18ELU26

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

BSc DEGREE EXAMINATION MAY 2022
(Sixth Semester)

Branch – **ELECTRONICS**

VLSI DESIGN

Time: Three Hours Maximum: 75 Marks

SECTION-A (10 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (10 x 1 = 10)

1. The n-type semiconductor have _____ as majority carriers.
   (i) Holes (ii) Negative ions
   (iii) Electrons (iv) Positive ions
2. The n-MOS invertor is better than BJT in terms of _____
   (i) Fast switching time (ii) Low power loss
   (iii) layout area (iv) All the mentioned
3. CMOS has high _____
   (i) noise margin (ii) packing density
   (iii) power dissipation (iv) high complexity
4. Oxidation process is carried out using _____
   (i) hydrogen (ii) low purity oxygen
   (iii) sulphur (iv) nitrogen
5. When NMOS is turned on in NMOS logic dynamic power is _____
   (i) increased (ii) decreased
   (iii) infinite (iv) doesn't change
6. The inputs in the PLD is given through _____
   (i) NAND gates (ii) OR gates
   (iii) NOR gates (iv) AND gates
7. After compiling VHDL code with any EDA tool, we get _____
   (i) Final device (ii) FPGA
   (iii) Optimized netlist (iv) Netlist
8. Which of the following can be the name of an architecture?
   (i) arch 1 (ii) 1arch
   (iii) arch_1 (iv) architecture
9. The most basic form of behavioural modelling in VHDL is _____statements.
   (i) IF (ii) Assignment
   (iii) Loop (iv) WAIT
10. Which of the following is not a way of partitioning a design?
    (i) Component (ii) Block statement
    (iii) Processes (iv) Generics

Cont...

SECTION - B (25 Marks)

Answer **ALL** questions
ALL questions carry **EQUAL** Marks (5 x 5 = 25)

11 a Compare MOS and CMOS.

OR

b Outline the process of design abstraction.

12 a Explain the photolithography process with diagram.

OR

b List out the CMOS design rules.

13 a Sketch the NMOS logic gates and explain it.

OR

b Compare the applications of CPLD and FPGA.

14 a Explain the introduction to VLSI.

OR

b Distinguish between the data types in VLSI.

15 a Compare the behavioural and structural modelling and list the similarities.

OR

b Narrate the steps involved in block statements of data flow modelling.

SECTION -C (40 Marks)

Answer **ALL** questions
ALL questions carry **EQUAL** Marks (5 x 8 = 40)

16 a Discuss the process of CMOS fabrication in steps.

OR

b Classify the behavioural, structural and physical domains and explain.

17 a Discuss about the well and channel formation in CMOS.

OR

b Summarise the points on passivation metrology.

18 a Highlight the important points on negative logic system.

OR

b Elucidate about the programmable array logic.

19 a Enumerate the capabilities of VHDL.

OR

b Classify the different types of operators used in VLSI.

20 a Distinguish between assignment statements of behavioural and dataflow modelling.

OR

b Identify the key points involved in component instantiation of structural modelling.

Z-Z-Z

END