(AUTONOMOUS)

MSc DEGREE EXAMINATION MAY 2026

(Second Semester)

Branch -**APPLIED ELECTRONICS**

CHIP DESING USING VERILOG / VERILOG

Time: Three Hours | Maximum: 75 Marks

SECTION-A (10 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** marks (10 × 1 = 10)

Module No.	Question No.	Question	K Level	CO
1	1	What is the basic building block of a Verilog design? (i) Function (ii) Module (iii) Task (iv) Block	K1	CO1
	2	Which data type is used to store binary values in Verilog? (i) integer (ii) real (iii) reg (iv) time	K2	CO1
2	3	Which of the following is a built-in primitive gate in Verilog? (i) nand (ii) module (iii) function (iv) always	K1	CO2
	4	Which switch is used for bidirectional signal flow? (i) nmos (ii) pmos (iii) tran (iv) bufif1	K2	CO2
3	5	Which keyword is used for continuous assignment in Verilog? (i) always (ii) wire (iii) initial (iv) assign	K1	CO3
	6	Which statement is used for multiple condition selection? (i) if (ii) case (iii) for (iv) while	K2	CO3
4	7	What is module instantiation? (i) Defining a module (ii) Writing a testbench (iii) Declaring a variable (iv) Calling a module inside another module	K1	CO4
	8	What is the purpose of a testbench? (i) Verify and simulate design (ii) Design hardware (iii) Store data (iv) Control power	K2	CO4
5	9	What does PLA stand for? (i) Programmable Logic Array (ii) Programmable Linear Array (iii) Parallel Logic Array (iv) Programmable Logic Application	K1	CO5
	10	What is ASIC? (i) General-purpose processor (ii) Analog circuit (iii) Application-Specific Integrated Circuit (iv) Memory device	K2	CO5

Cont...

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 × 7 = 35)

Module No.	Question No.	Question	K Level	CO
1	11.a.	Apply arithmetic and logical operators in Verilog with examples.	K1	CO1
		(OR)		
	11.b.	Differentiate between bitwise and reduction operators.		
2	12.a.	Illustrate tristate gates and pull gates.	K4	CO2
		(OR)		
	12.b.	Describe gate delays and their significance.		
3	13.a.	Explain continuous assignment in Verilog with examples.	K3	CO3
		(OR)		
	13.b.	Differentiate between dataflow and behavioral modeling.		
4	14.a.	Summarize module instantiation and port declaration.	K4	CO4
		(OR)		
	14.b.	Describe the disable statement and named events.		
5	15.a.	Organize the role of the logic synthesis and RT-level design.	K4	CO5
		(OR)		
	15.b.	Differentiate PLA and PAL Logic device families.		

SECTION -C (30 Marks)

Answer **ANY THREE** questions

ALL questions carry **EQUAL** Marks (3 × 10 = 30)

Module No.	Question No.	Question	K Level	CO
1	16	Describe in detail the structure of a Verilog module, including identifiers, keywords, and formatting rules.	K2	CO1
2	17	Identify the principles of sequential UDP model and analyze its behavior.	K4	CO2
3	18	Write and analyze a Verilog program using procedural constructs.	K3	CO3
4	19	Develop a complete testbench for a digital circuit including waveform generation.	K4	CO4
5	20	Compare and evaluate FPGA vs ASIC design methodologies.	K2	CO5

Z-Z-Z END