

**PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)**

**MSc DEGREE EXAMINATION MAY 2022
(Second Semester)**

Branch – APPLIED ELECTRONICS

ADVANCED DIGITAL SYSTEM DESIGN

Time: Three Hours

Maximum: 50 Marks

SECTION-A (5 Marks)

Answer ALL questions

ALL questions carry EQUAL marks $(5 \times 1 = 5)$

1. Who developed the Verilog?
(i) Moorby
(ii) Thomas
(iii) Russel and Ritchie
(iv) Moorby and Thomson
2. Which of the following models the components like resistors, capacitors etc?
(i) Resistor transfer Model
(ii) Layout Model
(iii) Circuit Level Model
(iv) Switched Level Model
3. What is the basic unit of behavioural description?
(i) Structure
(ii) Sequence
(iii) Data flow
(iv) Process
4. Which among the following process in data flow diagram at the most detailed level?
(i) Functional Primitive
(ii) Data Flows
(iii) Interface
(iv) Transfer description
5. Which type of device FPGA are?
(i) SLD
(ii) SRAM
(iii) EEPROM
(iv) PLD

SECTION - B (15 Marks)

Answer ALL Questions

ALL Questions Carry EQUAL Marks $(5 \times 3 = 15)$

6. (a) Classify the Module of Verilog.
(OR)
(b) Analyze the function of Data types.
7. (a) Explain the operation of Tristate Gates.
(OR)
(b) Elucidate the User Defined Primitives.
8. (a) Discuss about the Delays with example.
(OR)
(b) Analyze the function of Case Statement.
9. (a) Evaluate the external Ports of Structural Modeling.
(OR)
(b) Discuss the sharing task with function.
10. (a) Assess the Programming Logic device families.
(OR)
(b) Compare the function of mapping and Placement of FPGA.

Cont...

SECTION -C (30 Marks)

Answer ALL questions

ALL questions carry EQUAL Marks

(5 x 6 = 30)

11. (a) Evaluate the function of Operators.
(OR)
(b) Compare the function of Logical and Bitwise operators.
12. (a) Categorize the function of Bidirectional Switches.
(OR)
(b) Distinguish Combinational UDP and Sequential UDP.
13. (a) Discuss the function of Procedural Assignments.
(OR)
(b) Enumerate the function of Conditional Statement.
14. (a) Classify the system tasks.
(OR)
(b) Evaluate the operation of wave form generation.
15. (a) Illustrate the designing a Synchronous Sequential Circuit using PLA.
(OR)
(b) Discuss about the Controller Data Path Synthesis.

Z-Z-Z

END