PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)
MSc(SS) DEGREE EXAMINATION DECEMBER 2023
(Third Semester)

Branch - **SOFTWARE SYSTEMS (five year integrated)**

COMPUTER ORGANIZATION

Time: Three Hours   Maximum: 50 Marks

SECTION-A (5 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks   (5 x 1 = 5)

1 Which of the following is a type of computer architecture?
   (i) Microarchitecture   (ii) Harvard Architecture
   (iii) Von-Neumann Architecture   (iv) All of the mentioned

2 The stack is useful for_____.
   (i)   Storing the register status of the processor
   (ii) Temporary storage of data
   (iii) Storing contents of registers temporarily inside the CPU
   (iv) All of the mentioned

3 Which of the following is the fastest means of memory access for CPU?
   (i)   Registers   (ii) Cache
   (iii) Main memory   (iv) Virtual Memory

4 Which of the following devices provide a means of communication between a computer and outer world?
   (i) I/O   (ii) Storage
   (iii) Compact   (iv) Drivers

5 The interconnection topologies are implemented using _____ as a node.
   (i) control unit   (ii) microprocessor
   (iii) processing unit   (iv) microprocessor or processing unit

SECTION - B (15 Marks)
Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks   (5 x 3 = 15)

6 a) Convert the decimal number 41.6875 into binary.
                  OR
   b) Discuss about alphanumeric representation.

7 a) Explain in details about register stack.
                  OR
   b) Discuss about reverse polish notation.

8 a) Determine memory hierarchy with neat diagram.
                  OR
   b) Evaluate memory address map with proper diagram.

9 a) Explain DMA controller with neat diagram.
                  OR
   b) Discuss about CPU-IOP communications.

10 a) Evaluate characteristics of multiprocessors.

OR

b) Examine time shared common bus.

SECTION -C (30 Marks)
Answer ALL questions
ALL questions carry EQUAL Marks   (5 x 6 = 30)

11 a) Enumerate input output configuration.

OR

b) Elucidate input output instruction.

12 a) Determine three address instruction.

OR

b) Elucidate RISC instruction.

13 a) Enumerate read operation in memory organization.

OR

b) Determine hardware organization with neat diagram.

14 a) Explain in details about DMA transfer.

OR

b) Determine IBM 370 I/O channel.

15 a) Elucidate multistage switching network.

OR

b) Explain in details about hypercube interconnection.

Z-Z-Z   END