PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc(SS) DEGREE EXAMINATION DECEMBER 2023
(First Semester)

Branch – **SOFTWARE SYSTEMS** (Five years Intregrated)

ANALOG AND DIGITAL ELECTRONICS

Time: Three Hours Maximum: 50 Marks

SECTION-A (5 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (5 x 1 = 5)

1 The Decimal equivalent of 11100 is ____.
(i) 23 (ii) 31
(iii) 27 (iv) 28

2 ____ are the universal logic gates.
(i) NAND and NOR gates (ii) NOT and EX-OR gates
(iii) AND and NOT gates (iv) OR and EX-OR gates

3 Which of the following can be represented for Decoder?
(i) Sequential circuit (ii) Combinational circuit
(iii) Logical circuit (iv) None of the mentioned

4 In a 4 bit Johnson counter sequence, there are a total of how many states?
(i) 1 (ii) 3
(iii) 4 (iv) 8

5 The input applied to an inverting amplifier is _____.
(i) Equal to output (ii) Equal to inverted output
(iii) Not equal to output (iv) Output is equal to input

SECTION - B (15 Marks)
Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks (5 x 3 = 15)

6 a Convert 278_{10} and 56_{10} into binary number.
OR
b Give an account on Excess-3 code.

7 a Explain the operation of OR gate with truth table.
OR
b Reduce the Boolean expression Y= AB+ AC+ BD+ BC.

8 a Describe the operation of Full- Subtractor with circuit diagram.
OR
b Discuss about the working of Decoder with neat sketch.

Cont...

9 a With neat diagram and explain the operation of JK Flip Flop.

OR

b Write short note on Decade counter.

10 a Draw and explain the operation of Inverting amplifier.

OR

b Explain the operation of analysis of Integrator with diagram.

SECTION -C (30 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 x 6 = 30)

11 a Convert the Hexadecimal 2F58 to decimal equivalent.

OR

b Show the 8 bit Subtraction of these decimal numbers in 2's complement representation (i) +16, -38 (ii) -43, -78

12 a State and explain the De-Morgan's theorem.

OR

b Solve the following expression using K-map.
$F(A,B,C,D)= \sum_m (0,1,2,3,4,5,6,7,8,10,13)$

13 a Enumerate the operation of Half- subtractor circuit diagram with truth table.

OR

b Briefly explain the working of Demultiplexer with diagram.

14 a Describe the working of Serial In Parallel Out with neat diagram.

OR

b Elucidate the operation of Synchronous counter with neat sketch.

15 a Explain the operation of open loop and closed loop using op-amp with diagram.

OR

b Design a subtractor circuit using op-amp and drive an equation for its output voltage.

Z-Z-Z END