PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION MAY 2018
(Second Semester)

Branch - APPLIED ELECTRONICS

ADVANCED DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 75 Marks

SECTION -A (30 Marks!
Answer ALL questions
ALL questions carry EQUAL Marks ( 5 x 6 = 30)

1 a Define the entity declaration in VHDL.

OR

b Describe briefly about the structural modeling,

2 a Write a brief introduction to verilog.

OR

b Explain about the concatenation operators.

3 a Write short note on tri state gates.

OR

b Define the working of implicit nets.

4 a What is a net declaration assignment and explain its importance?

OR

b Describe about the loop statement with an example.

5 a Explain the working of PL A.

OR

b What is module instantiation and explain about it?

**SECTION -B (45 Marks)**
Answer any THREE questions
ALL questions carry EQUAL Marks ( 3 x 1 5 = 45)

6 Explain briefly about the package declaration with suitable diagrams.

7 Describe in detail about the (i) Relational operator and (ii) Equality operator.

8 Explain briefly about the combinational UDP and sequential UDP.

9 Discuss in detail about the procedural assignments with examples.

10 Explain briefly about the sharing task and functions.