PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION MAY 2019
(Second Semester)

Branch - APPLIED ELECTRONICS

ADVANCED DIGITAL SYSTEM DESIGN

Three Hours Maximum: 75 Marks

SECTION-A (10 Marks!
Answer **ALL** questions
ALL questions carry **EQUAL** marks (1 0 x 1 = 10)

1 Which one of the following is not used in modeling hardware in verilog HDL?
(i) logic-0 (ii) logic-1
(iii) known value (iv) high-impedance

2 How many kinds of constants are usedin verilog HDL?
(i) 2 (ii) 3
(iii) 4 (iv) 5

3 Indicate the combinational logic circuit.
(i) Flip Flop (ii) Register
(iii) Counter (iv) None

4 The variables read state, CPU Bus and Main Bus are used in modeling a
(i) Pull gate (ii) MOS switch
(iii) Tristate gate (iv) Bidirectional switch

5 Procedural assignments can appear only within____ statement.
(i) always (ii) if
(iii) loop (iv) case

6 Which one of the following loop statements is supported for synthesis?
(i) while-loop (ii) for-Ioop
(iii) forever-lop (iv) repeat-loop

7 A function call represents
(i) combinational logic
(ii) sequential logic
(iii) either combinational logic or sequential logic
(iv) both combinational and sequential logics

8 The functional mismatches are printed by
(i) a net list (ii) a test bench
(iii) a delay (iv) none

9 FPGA design includes
(i) Technology mapping (ii) Placement & routing
(iii) RTL synthesis (iv) all the above

FPGA stands for
(i) Flag Programmable Gate Assignment
(ii) Field Programmable Gate Arrays
(iii) Field Programmable Group Arrays
(iv) Flag Programmable Gate Arrangement

Cont...

SECTION - B (35 Marks)

Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks (5 x 7 = 35)

11 a Describe the identifiers used in Verilog HDL.

OR

b Discuss the Relational operators with an example.

12 a Explain the design of built-in primitive gates.

OR

b How will you define a UDP in Verilog HDL? Explain the sequential UDP.

13 a Design a combinational circuit from blocking and Non blocking procedural assignments.

OR

b Explain conditional and block statements with suitable examples.

14 a Describe tasks and functions.

OR

b How will you write a test bench? Explain.

15 a Explain the process of "Technology Mapping" in FPGA design.

OR

b Discuss with example, the register transfer logic synthesis.

SECTION - C (30 Marks)

Answer any **THREE** Questions
ALL Questions Carry **EQUAL** Marks (3 x 10 = 30)

16 Discuss the conditional and replication operators of Verilog HDL.

17 Explain the design of
(i) MOS Switches (ii) Tristate gates

18 Discuss the different kinds of case statements.

19 Explain the modules instantiation of
(i) User-built multipliers
(ii) User-specific flip-flops

20 Design a synchronous sequential circuit using PLA.

Z-Z-Z END

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