14ELP10

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION MAY 2019
(Second Semester)

Branch - **APPLIED ELECTRONICS**

ADVANCED DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 75 Marks

SECTION -A (30 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 x 6 = 30)

1 a With an example, explain the Entity - Architecture body of VHDL.

OR

b Write a VHDL program for Half Adder in behaviroral modeling Style.

2 a Brief the Module, Identifiers and Keywords of Verilog.

OR

b Write a Verilog program for Full Adder.

3 a Explain the functions of Tristate gates and Pull gates.

OR

b Discuss about the Gate delays.

4 a With example, explain the various procedural assignment statements.

OR

b With a Verilog program, explain the function of CASE statement.

5 a Brief the working of Disable Statement.

OR

b Explain how to read vectors from a text file.

SECTION -B (45 Marks)

Answer any **THREE** questions

ALL questions carry **EQUAL** Marks (3 x 1 5 = 45)

6 Write a VHDL program for Multiplexer and Demultiplexer.

7 Explain in detail about the various Data types and Operators in detail.

8 What is UDP ? Explain the Combinational UDP and Sequential UDP.

9 Discuss the Block, Conditional and Loop Statements with an example.

10 Write a Verilog program for ALU.

Z-Z-Z END