23ELU624N

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

BSc DEGREE EXAMINATION MAY 2026
(Sixth Semester)

Branch – **ELECTRONICS**

VLSI DESIGN

Time: Three Hours Maximum: 75 Marks

SECTION-A (10 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (10 × 1 = 10)

Module No.	Question No.	Question	K Level	CO
1	1	A junction between p-type and n-type silicon is called a _____ (i) FET (ii) Transistor (iii) SCR (iv) diode	K1	CO1
	2	Digital VLSI design is often partitioned into _____ levels of abstractions (i) 3 (ii) 2 (iii) 5 (iv) 6	K2	CO1
2	3	CMOS processing steps can be broadly divided into _____parts (i) Four (ii) Two (iii) Eight (iv) Three	K1	CO2
	4	The thick oxide used to be formed by a process called_____ (i) LOCOS (ii) LCOS (iii) LOCS (iv) LOOS	K2	CO2
3	5	PMOS transistors have the opposite behavior of _____transistors (i) NMOS (ii) CMOS (iii) MOS (iv) PMOS	K1	CO3
	6	A _____comprises multiple circuit blocks on a single chip (i) VHDL (ii) CPLD (iii) PAL (iv) PLA	K2	CO3
4	7	_____is used to describe a model for a digital hardware device (i) VLSI (ii) FPGA (iii) VHDL (iv) LSI	K1	CO4
	8	An identifier in VHDL is composed of a sequence of one or more _____ (i) image (ii) Digits (iii) Special Characters (iv) Characters	K2	CO4
5	9	An architecture body describes the _____view of an entity (i) internal (ii) external (iii) side (iv) top	K1	CO5
	10	The component instantiation is not connected to any _____ (i) noise (ii) signal (iii) spikes (iv) supplies	K2	CO5

Cont...

SECTION - B (35 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 × 7 = 35)

Module No.	Question No.	Question	K Level	CO
1	11.a.	Describe the nMOS and pMOS transistor in VLSI design with diagram.	K3	CO1
		(OR)		
	11.b.	Illustrate Behavioral, Structural and physical Domains using Y chart.		
2	12.a.	SiO2 manufacturing techniques What are common approaches follows, list it out?	K3	CO2
		(OR)		
	12.b.	Survey the construct of Metallization in CMOS Processing Technology? Write it.		
3	13.a.	How to Build a NOT Gate using NMOS? Discuss briefly.	K3	CO3
		(OR)		
	13.b.	How to Develop Programmable Array Logic (PAL) in Implementation Technology.		
4	14.a.	Show the major capabilities that the language provides in VHDL.	K2	CO4
		(OR)		
	14.b.	Illustrate the various types of Floating Point data used in VHDL.		
5	15.a.	Summarize the Case statement in Behavioral Modeling.	K1	CO5
		(OR)		
	15.b.	Draw and explain a 9-bit parity generator circuit for structural model.		

SECTION -C (30 Marks)

Answer **ANY THREE** questions

ALL questions carry **EQUAL** Marks (3 × 10 = 30)

Module No.	Question No.	Question	K Level	CC
1	16	Analyze how a D Flip-Flop performs in CMOS logic with a diagram.	K4	CO1
2	17	Criticize the Gate, Source and Drain Formations in CMOS technology.	K4	CO2
3	18	Discuss in detail about Field Programmable Gate Array (FPGA).	K5	CO3
4	19	Explain What is an entity in VHDL? Discuss any three types.	K2	CO4
5	20	Evaluate Block Statement in Dataflow Modeling.	K3	CO5

Z-Z-Z END