25PHP103

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION DECEMBER 2025
(First Semester)

Branch - **PHYSICS**

INTEGRATED ELECTRONICS

Time: Three Hours

Maximum: 75 Marks

SECTION-A (10 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (10 × 1 = 10)

Module No.	Question No.	Question	K Level	CO
1	1	The binary addition of $(1011)_2$ and $(1101)_2$ is _____ a) $(11000)_2$ b) $(10100)_2$ c) $(11100)_2$ d) (10010)	K1	CO1
	2	The 1's complement of $(101100)_2$ is _____ a) 101011 b) 010011 c) 110011 d) 010100	K2	CO1
2	3	The output of a NOT gate is _____ a) Always 0 b) Always 1 c) Same as input d) Complement of input	K1	CO2
	4	A 3-variable K-map contains how many cells? a) 4 b) 6 c) 8 d) 16	K2	CO2
3	5	A de-multiplexer can be used as _____ a) Data distributor b) Data selector c) Encoder d) Comparator	K1	CO3
	6	The invalid condition of an SR flip-flop occurs when ____ a) S = 0, R = 0 b) S = 1, R = 0 c) S = 1, R = 1 d) S = 0, R = 1	K2	CO3
4	7	The basic logic family that uses diodes and transistors is called _____ a) Transistor-Transistor Logic (TTL) b) Complementary Metal Oxide Semiconductor (CMOS) c) Emitter Coupled Logic (ECL) d) Resistor-Transistor Logic (RTL)	K1	CO4
	8	The propagation delay in transistor logic circuits is mainly caused by _____ a) Input voltage levels b) Transistor switching time c) Diode resistance d) Power supply voltage	K2	CO4
5	9	The input impedance of an ideal op-amp is____ a) Infinite b) Zero c) Very low d) Equal to output impedance	K1	CO5
	10	The common-mode rejection ratio (CMRR) of an ideal op-amp is _____ a) 0 b) 1 c) 100 d) Infinite	K2	CO5

Cont...

SECTION - B (35 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 × 7 = 35)

Module No.	Question No.	Question	K Level	CO
1	11.a.	Explain binary addition and subtraction with suitable examples.	K2	CO1
		(OR)		
	11.b.	Estimate the X value of the following: (i) $277_{10} = X_2$ (ii) $10110_2 = X_{10}$		
2	12.a.	Construct the truth table for a logic circuit having inputs A and B connected to an NAND gate. Draw the logic diagram and write the Boolean expression.	K3	CO2
		(OR)		
	12.b.	Use a Karnaugh map to simplify the logic expression $Y = A(B\overline{C}+\overline{B}\overline{C}) + A\overline{B}C$.		
3	13.a.	Examine 2-to-1 multiplexer with circuit representation, truth table and logic diagram.	K4	CO3
		(OR)		
	13.b.	Explain J-K Master-Slave flip flops with neat diagram.		
4	14.a.	Summarize any five characteristics of digital logic families.	K5	CO4
		(OR)		
	14.b.	Measure the Transistor-Transistor Logic (TTL) characteristics.		
5	15.a.	Evaluate the gain, input and output impedances of Non-inverting Operational Amplifier.	K5	CO5
		(OR)		
	15.b.	Explain Digital to Analog conversion system.		

SECTION -C (30 Marks)

Answer **ANY THREE** questions

ALL questions carry **EQUAL** Marks (3 × 10 = 30)

Module No.	Question No.	Question	K Level	CO
1	16	Explain the process of obtaining the 1's and 2's complement of a binary number with an examples.	K2	CO1
2	17	Apply Karnaugh map, to convert (i) $Y = \overline{B}\overline{C} + \overline{A}B + ABC$ into its product-of-sum (POS) equation. (ii) $Y = (A+B)(\overline{B}+C)$ into its sum-of-product (SOP) equation.	K3	CO2
3	18	Illustrate the four-bit ring counter and shift counter with timing waveforms.	K4	CO3
4	19	Interpret the performance characteristics of various logic families.	K5	CO4
5	20	Evaluate the waveforms of OP-AMP Astable multivibrator and determine its frequency.	K5	CO5

Z-Z-Z END