PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

BSc DEGREE EXAMINATION DECEMBER 2025
(Sixth Semester)

Branch – **ELECTRONICS**

VLSI DESIGN

Time: Three Hours

Maximum: 50 Marks

SECTION-A (5 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (5 x 1 = 5)

1 Name the insulating material used between the gate and channel of a MOS transistor
(i) Metal (ii) Semiconductor
(iii) Oxide (iv) Silicon

2 Choose the role of photoresist in the photo lithography step of CMOS fabrication
(i) To remove impurities (ii) To protect the silicon wafer
(iii) To anneal the Silicon (iv) To create a pattern on the wafer

3 What is an FPGA
(i) Field program gate array (ii) First program gate array
(iii)Field programmable gate array (iv) First programmable gate array

4 Which of the following is a hardware description language used for digital systems
(i) Python (ii) HTML
(iii) VHDL (iv) SOL

5 Identify the VHDL modelling style which describes a system by its internal structure and components
(i) Behavioral (ii) Structural
(iii) Data flow (iv)Functional

SECTION - B (15 Marks)
Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks (5 x 3 = 15)

6 a Explain the history and evolution of MOS transistor technology.
OR
b State and explain the basic components of a CMOS inverter.

7 a Analyze the role of photolithography in CMOS processing.
OR
b Explain the function of well formation in CMOS technology and how it impacts the device performance?

8 a Bring out the important applications of CPLDs and FPGAs.
OR
b Show the difference between NMOS logic gates and CMOS logic gates.

Cont...

9 a Explain the role of identifiers in VHDL.

OR

b State and explain the difference between the Entity Declaration and Architecture Body in VHDL.

10 a Explain the difference between the signal assignment and variable assignment in behavioral modelling.

OR

b Explain the purpose of the process statement in VHDL.

SECTION -C (30 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 x 6 = 30)

11 a Summarize the CMOS fabrication process step by step with neat diagrams.

OR

b Discuss the different levels of design abstraction in CMOS design partitioning and their significance in design verification.

12 a Discuss the CMOS process flow from wafer formation to passivation, highlighting the major steps involved.

OR

b Summarize the layout design rules in CMOS processing technology.

13 a Classify various types of programmable logic devices.

OR

b Compare and explain the working of Programmable Logic Array (PLA) and Programmable Array Logic (PAL).

14 a Categorize the functions of data types in VHDL with examples.

OR

b Discuss about various operators in VHDL with examples.

15 a Discuss the data flow modelling style with suitable examples.

OR

b Compare the conditional signal assignment statement and block statement in Data flow modelling.

Z-Z-Z END