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22CMU102N

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

BSc DEGREE EXAMINATION DECEMBER 2025
(First Semester)

Branch – **COMPUTER SCIENCE**

FUNDAMENTALS OF DIGITAL COMPUTERS

Time: Three Hours Maximum: 75 Marks

SECTION-A (10 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** marks (10 × 1 = 10)

Module No.	Question No.	Question	K Level	CO
1	1	What is the binary equivalent of the decimal number 25? a) 11011 b) 11001 c) 10110 d) 10011	K1	CO1
	2	Identify the law which is represented by A + AB = A. a) Absorption Law b) Distributive Law c) Associative Law d) Idempotent Law	K2	CO1
2	3	Find the flip-flop that commonly used in counters. a) SR Flip-Flop b) D Flip-Flop c) T Flip-Flop d) JK Flip-Flop	K1	CO2
	4	How many inputs and outputs do a half adder requires? a) 2 inputs and 2 outputs b) 1 input and 1 output c) 2 inputs and 1 output d) 3 inputs and 2 outputs	K2	CO2
3	5	In register transfer notation, the statement R1 <- R2 indicates that a) Data is transferred from R1 to R2 b) Data is transferred from R2 to R1 c) Data is swapped between R1 and R2 d) Data is added from R1 and R2	K1	CO3
	6	_____ microoperation is used to transfer data from one register to another without modification. a) Increment b) Decrement c) Complement d) Transfer	K2	CO3
4	7	The number of bits in an instruction format is determined by _____. a) The word length of the CPU b) The number of registers c) The size of the memory d) The number of operations the CPU can perform	K2	CO4
	8	In which addressing mode the operand is directly specified in the instruction? a) Direct addressing b) Immediate addressing c) Indirect addressing d) Register addressing	K1	CO4
5	9	The component that coordinates the DMA transfer is ___. a) CPU b) Memory Management Unit c) DMA Controller d) Cache Controller	K2	CO5
	10	What is Cache memory? a) Slower than main memory but faster than registers b) Faster than main memory but slower than registers c) The same speed as main memory d) The same speed as secondary storage	K1	CO5

Cont...

SECTION - B (35 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 × 7 = 35)

Module No.	Question No.	Question	K Level	CO
1	11.a.	Convert the F3A7C2 hexadecimal number to binary and octal.	K3	CO1
		(OR)		
	11.b.	Determine by means of a truth table the validity of DeMorgan's theorem for three variables: (ABC)' = A' + B' + C'.		
2	12.a.	Solve the following Boolean functions using three-variable k-map. F(A,B,C) = Σ (0,2,3,4,6).	K6	CO2
		(OR)		
	12.b.	Design a full adder circuit using basic logic gates and explain it.		
3	13.a.	With a neat labeled sketch the data transfer between two registers with a control signal.	K3	CO3
		(OR)		
	13.b.	Demonstrate how memory write operation is performed using a system bus.		
4	14.a.	How the stack organization works in a typical computer system? Discuss it.	K2	CO4
		(OR)		
	14.b.	Utilize two-address instructions to evaluate X = (A + B) * (C + D).		
5	15.a.	Compare and contrast the roles of CPU and I/O processors in data transfer tasks.	K4	CO5
		(OR)		
	15.b.	Inspect the relation between address and memory space in a virtual memory system.		

SECTION -C (30 Marks)

Answer **ANY THREE** questions

ALL questions carry **EQUAL** Marks (3 × 10 = 30)

Module No.	Question No.	Question	K Level	CO
1	16	Draw and explain the basic logic gates in digital circuits.	K3	CO1
2	17	Simplify the following expressions in sum-of-products and product-of-sums form. x'z' + y'z' + yz' + xy	K4	CO2
3	18	Elaborate the 4-bit arithmetic circuit along with its Function table.	K6	CO3
4	19	Classify the different types of addressing modes. In that explain any five of them.	K2	CO4
5	20	Explain how the associative mapping technique works in cache memory.	K2	CO5

Z-Z-Z END