PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION DECEMBER 2025
(First Semester)

Branch – **APPLIED ELECTRONICS**

ANALOG AND DIGITAL CIRCUIT DESIGN

Time: Three Hours Maximum: 75 Marks

SECTION-A (10 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** marks (10 × 1 = 10)

Module No.	Question No.	Question	K Level	CO
1	1	An ideal op-amp requires infinite bandwidth because _____ a) Signals can be amplified without attenuation b) Output common-mode noise voltage is zero c) Output voltage occurs simultaneously with input voltage changes d) Output can drive infinite number of device	K2	CO1
	2	The formula for output offset voltage of an op-amp due to input bias current is _____ a) $V_{OIB} = R_F * I_B$ b) $V_{OIB} = (R_F+R_1)/I_B$ c) $V_{OIB} = (1+R_F)*I_B$ d) $V_{OIB} = [1+(R_F/R_1)]*I_B$	K2	CO1
2	3	Which of the following circuit is not made of digital ICs? a) Shift registers b) Multipliers c) Demultiplexers d) Counters	K2	CO1
	4	Filters are classified as _____ a) Analog or digital b) Passive or active c) Audio or radio frequency d) All of the mentioned	K2	CO1
3	5	In which one of the following amplifier, the voltage gain is always greater than one? a) Idea inverting b) Ideal non inverting c) Both a and b d) None of the above	K4	CO2
	6	What is term used for the change in the op-amp's offset voltage caused by variations in supply voltage ? a)Large signal-voltage gain b)Common-Mode Rejection Ratio c)Common-mode voltage gain d)Power Supply Rejection Ratio	K4	CO2
4	7	What is the indication of a short to ground in the output of a driving gate? a) Only the output of the defective gate is affected b) There is a signal loss to all load gates c) The node may be stuck in either the HIGH or the LOW state d) The affected node will be stuck in the HIGH state	K6	CO3
	8	One that is not the outcome of magnitude comparator is_____ a) a > b b) a – b c) a < b d) a = b	K6	CO3
5	9	What type of flip-flop is commonly used for building finite state machines? a) S-R Flip-Flop b) D Flip-Flop c) T Flip-Flop d) JK Flip-Flop	K6	CO5
	10	What is the primary purpose of a finite state machine in digital logic design? a) To generate random sequences b) To synchronize data transfer c) To model sequential logic behavior d) To perform arithmetic operations	K6	CO5

Cont...

SECTION - B (35 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 × 7 = 35)

Module No.	Question No.	Question	K Level	CO
1	11.a.	Describe the operations of the Op-amp using a equivalent circuit.	K2	CO1
		(OR)		
	11.b.	Explain the current input bias and offset.		
2	12.a.	Identify the amplifier for the instrumentation.	K4	CO2
		(OR)		
	12.b.	Describe the features of LDO Regulators.		
3	13.a.	Describe the Schmitt Trigger characteristics.	K6	CO3
		(OR)		
	13.b.	Describe the generator of triangular waves and sawtooth waves.		
4	14.a.	Discuss about the Design Procedure of CLC.	K4	CO4
		(OR)		
	14.b.	Differentiate between encoders and decoders.		
5	15.a.	Categorize State Assignment and State Table Reduction.	K6	CO5
		(OR)		
	15.b.	What is the purpose of the synchronous counter design.		

SECTION -C (30 Marks)

Answer **ANY THREE** questions

ALL questions carry **EQUAL** Marks (3 × 10 = 30)

Module No.	Question No.	Question	K Level	CO
1	16	Describe the Op-amp's operations using a circuit schematic.	K2	CO1
2	17	Give an explanation of voltage regulators.	K4	CO2
3	18	Discuss about the Clippers and Clampers with applications.	K6	CO3
4	19	Describe the Demultiplexers and Multiplexers in details.	K4	CO4
5	20	Examine the SLC Design Process using the circuit.	K6	CO5

Z-Z-Z END