TOTAL PAGES: 2

22ELP208N

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION MAY 2025
(Second Semester)

Branch – **APPLIED ELECTRONICS**

VERILOG

Time: Three Hours Maximum: 75 Marks

SECTION-A (10 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (10 × 1 = 10)

Module No.	Question No.	Question	K Level	CO
1	1	Which versions of the Verilog are known as System Verilog? a) Verilog version 3.0 b) Verilog version 1.0 c) Verilog version 1.5 d) Verilog version 4.0	K1	CO1
	2	What is the result of the following Verilog relational operators expression: (5 < 3) ? a) 1 b) 0 c) x d) z	K2	CO1
2	3	Which Verilog data type can store multiple logic values (0, 1, x, z)? a) wire b) reg c) int d) logic	K1	CO2
	4	Which gate delays are modeled in Verilog to represent propagation delays? a) Setup and hold delays b) Inertial and transport delays c) Rise, fall, and turn-off delays d) Structural delays	K2	CO2
3	5	What is the primary construct used for dataflow modeling in Verilog system? a) always block b) initial block c) Continuous assignment d) Case statement	K1	CO3
	6	Which of the following is not a type of timing control used in behavioral modeling? a) Delay control b) Event control c) Level control d) Wait statement	K2	CO3
4	7	What is required when instantiating a module in Verilog? a) A continuous assignment b) Ports and parameters c) Sensitivity list d) Always block	K1	CO4
	8	Which of the following correctly differentiates between a task and a function in Verilog? a) A task must return a value, while a function cannot. b) A function can contain timing control, while a task cannot. c) A task can contain delay or wait statements, but a function cannot. d) A task can be called within a continuous assignment, but a function	K2	CO4
5	9	Which of the following is a programmable logic device used in digital design? a) ROM b) PLA c) RAM d) Register	K1	CO5
	10	What does "RT" stand for in FPGA design? a) Real-Time b) Register Transfer c) Route Transfer d) Reconfigurable Technology	K2	CO5

Cont...

SECTION - B (35 Marks)

Answer **ALL** questions
ALL questions carry **EQUAL** Marks (5 × 7 = 35)

Module No.	Question No.	Question	K Level	CO
1	11.a.	Describe the 1-bit full-adder circuit using the data flow style.	K4	CO1
		(OR)		
	11.b.	Discuss the role of Verilog data types and usage of three types of operators with examples.		
2	12.a.	Explain the syntax of tristate gates model with truth table.	K4	CO2
		(OR)		
	12.b.	Discuss the effect of gate delays. Give details about rise, fall and turn off delay with example values.		
3	13.a.	Give an example of how turn off delay is used in a continuous assignment in Verilog.	K5	CO3
		(OR)		
	13.b.	Examine the role of delays in dataflow modeling. Explain the effect of net delay.		
4	14.a.	Explain the functions of modules and ports in structural modeling with a simple example.	K3	CO4
		(OR)		
	14.b.	Draw a structural model for a 2-bit adder using module instantiation.		
5	15.a.	Compare PLA and PAL.	K3	CO5
		(OR)		
	15.b.	Explain the role of RT/Logic synthesis in FPGA programming.		

SECTION -C (30 Marks)

Answer **ANY THREE** questions
ALL questions carry **EQUAL** Marks (3 × 10 = 30)

Module No.	Question No.	Question	K Level	CO
1	16	Explain about Concatenation and Replication operators with example.	K5	CO1
2	17	Analyze the multiple inputs and multiple outputs of built- in primitive gates in Verilog HDL. Provide examples.	K4	CO2
3	18	Develop a Verilog model using procedural constructs to implement a counter with timing control and loop statements.	K5	CO3
4	19	Analyze the process of writing a test bench with waveform generation and display of results using system tasks.	K4	CO4
5	20	Evaluate the role of technology mapping and routing in FPGA design. How these phases impact the performance, power consumption of an FPGA-based system?	K4	CO5

Z-Z-Z END