PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

BSc DEGREE EXAMINATION MAY 2025
(Sixth Semester)

Branch – **ELECTRONICS**

VLSI DESIGN

Time: Three Hours | Maximum: 50 Marks

SECTION-A (5 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (5 x 1 = 5)

1 Which among the following is a used in CMOS fabrication?
(i) P well (ii) N well
(iii) Twin tub (iv) All of the above

2 Design rules are based on_____
(i) λ (ii) A
(iii) Θ (iv) Ψ

3 FPGA can be expanded a_____
(i) Finite Programmable Gate Array (ii) Field Programmable Grounded Assay
(iii) Finite Programmable Grounded Assay (iv) Field Programmable Gate Array

4 _____is a VHDL term, for a parameter that passes information to an entity.
(i) Attribute (ii) Configuration
(iii) Generic (iv) Process

5 Which statement provides internal and transport delay?
(i) Signal (ii) Block
(iii) Generate (iv) Driver

SECTION - B (15 Marks)
Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks (5 x 3 = 15)

6 a Draw the cross section of CMOS and explain its operation.
OR
b Summarize the design verification sequence in VLSI design.

7 a Describe the Photolithography process.
OR
b Articulate the contact rules in CMOS Technology.

8 a Discuss the operation of MOS transistor as switch.
OR
b Differentiate: PAL and PLA.

Cont...

9 a Discuss about the data types in VHDL.

OR

b Write a VHDL code to test the functionality of OR gate.

10 a Write a behavioral model VHDL code to implement Full Adder.

OR

b Compare: Data flow and behavioral modeling in VHDL programming.

SECTION -C (30 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 x 6 = 30)

11 a Draw and explain the operation of CMOS NAND and NOR Logic Gates.

OR

b Draw and evaluate the design procedures for N-Well CMOS fabrication steps.

12 a Elaborate the CMOS Lambda based design rules.

OR

b Summarize the steps involved in CMOS processing technology.

13 a Draw the NMOS Basic Logic Gates and summarize the functionality.

OR

b Appraise the applications of CPLDs and FPGAs.

14 a With an example, explain the structure of VHDL program.

OR

b Analyze the operators in VHDL.

15 a Write a structural modeling VHDL code to implement 4:1 Multiplexer.

OR

b With an example, explain the looping statements of VHDL.

Z-Z-Z END