18ELP09

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION DECEMBER 2022
(Second Semester)

Branch – **APPLIED ELECTRONICS**

ADVANCED DIGITAL SYSTEM DESIGN

Time: Three Hours Maximum: 50 Marks

SECTION-A (5 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (5 x 1 = 5)

1 Which of the following is not an assignment operator?
(i) <= (ii) :=
(iii) => (iv) =

2 By how many modeling styles, the gates in VHDL can be implemented?
(i) 1 (ii) 2
(iii) 3 (iv) 4

3 The most basic form of behavioral modeling in VHDL is _____
(i) IF statements (ii) Assignment statements
(iii) Loop statements (iv) WAIT statements

4 What is the basic unit of structural modeling?
(i) Process (ii) Component declaration
(iii) Component instantiation (iv) Block

5 How many total bits can be stored in these arrays?
(i) 16 (ii) 9
(iii) 64 (iv) 27

SECTION - B (15 Marks)
Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks (5 x 3 = 15)

6. a. What is the difference between VHDL and Verilog?
OR
b. What are the main usages of VHDL?

7. a. Explain hardware modeling verilog primitives.
OR
b. Discuss about pull gates.

8. a. Compare the combinational behavior and sequential behavior of user defined primitives.
OR
b. Explain the verilog model for net delay and module paths and delays.

9. a. Define external ports.
OR
b. Discuss the sharing task.

10. a. Compare the speed performance of ACT 1,2,3.
OR
b. Write a program for synthesis of case and conditional.

Cont...

SECTION -C (30 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 x 6 = 30)

11 a. What are the main differences between task and function in Verilog?

OR

b. Briefly explain the verilog data types.

12 a. Implement NAND, AND, OR gates using MOS switch test it with a suitable test bench.

OR

b. Design and verify a switch level model at the four channel MOS transistor.

13 a. Write short notes on non-blocking assignments and what are the sequences takes place at each positive edge of clock for the non-blocking assignments.

OR

b. Explain behavioral models of finite state machines.

14 a. Briefly explain the mixing structure with behaviour.

OR

b. What is synthesis of priority structures give one example with program?

15 a. Explain about the state assignment for FPGA.

OR

b. Explain in detail about designing a synchronous sequential circuit using PLA.

Z-Z-Z END