22ELP208

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION DECEMBER 2023
(Second Semester)

Branch – **APPLIED ELECTRONICS**

VERILOG

Time: Three Hours Maximum: 50 Marks

SECTION-A (5 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (5 x 1 = 5)

1. Who developed the Verilog?
   (i) Moorby (ii) Thomas
   (iii) Russell and Ritchie (iv) Moorby and Thomson

2. _____ Gate have only one input and one or more inputs.
   (i) Multiple-Input Gate (ii) Multiple –output Gate
   (iii) Tristate Gate (iv) Pull Gates

3. What is the purpose of the "case" statement in Verilog?
   (i) To define a new module (ii) To specify simulation time
   (iii) To declare variables (iv) To implement conditional logic

4. Which keyword is used to specify a Verilog task?
   (i) task (ii) function
   (iii) sub-module (iv) block

5. PAL stands for_____.
   (i) Programmable Array Logic (ii) Programmable Logic Array
   (iii) Programmable Array Loaded (iv) None of the these

SECTION - B (15 Marks)
Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks (5 x 3 = 15)

6 a. Explain the Identifiers.
OR
b. Discuss the Relational Operators.

7 a. Discuss the Multiple-Input gates.
OR
b. Explain the MOS Switches.

8 a. Explain the Procedural Constructs.
OR
b. Illustrate Case statement.

9 a. Write short note on Module instantiation.
OR
b. Discuss the waveform generation.

10 a. Give application of PLAs.
OR
b. Explain the Routing.

Cont...

SECTION -C (30 Marks)

Answer **ALL** questions
ALL questions carry **EQUAL** Marks (5 x 6 = 30)

11 a. Discuss the Data types.

OR

b. Explain the Arithmetic and Logical operators with example.

12 a. Explain the Tristate gates.

OR

b. Discuss the Combinational UDP.

13 a. Discuss the Continuous assignment and Net-Declaration assignment.

OR

b. Explain the following statement
(i) Conditional statement (ii) Loop statement.

14 a. Describe the system tasks and function.

OR

b. Explain the Reading vectors from a text file.

15 a. Discuss the PAL.

OR

b. Draw the basic architecture of data path controller and explain.

Z-Z-Z END