18ELU26

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

BSc DEGREE EXAMINATION MAY 2024
(Sixth Semester)

Branch – **ELECTRONICS**

VLSI DESIGN

Time: Three Hours Maximum: 50 Marks

SECTION-A (5 Marks)
Answer **ALL** questions
ALL questions carry **EQUAL** marks (5 x 1 = 5)

1 Which oxide layer is formed in the MOSFET?
(i) Metal oxide (ii) silicon dioxide
(iii) Polysilicon oxide (iv) oxides of non metals

2 Identify CMOS fabrication when the photo resist layer is exposed to___.
(i) Visible light (ii) ultra violet
(iii) Infrared light (iv) fluorescent

3 Which of the following is full form of a FPGA?
(i) Field program gate array (ii) First program gate array
(iii) Field programmable gate array (iv) First programmable gate array

4 Mention a package in VHDL consists of _____.
(i) Commonly used architectures
(ii) Commonly used tools
(ii) Commonly used data type And subroutines
(iv) Commonly used Syntax and variables

5 Find the most basic form of behavioral modeling in VHDL is _____.
(i) If statement (ii) Assignment statement
(iii) Loop statement (iv) Wait statement

SECTION - B (15 Marks)
Answer **ALL** Questions
ALL Questions Carry **EQUAL** Marks (5 x 3 = 15)

6 a Define CMOS logic.
OR
b State design abstraction.

7 a Develop the process of wafer formation.
OR
b Analyze the concept of passivation.

8 a Summarize the working of CMOS logic gates.
OR
b Bring out the application of CPLDS.

9 a Show the history of VHDL.
OR
b Bring out the function of Identifiers.

10 a Explain the function of variable assignment statement.
OR
b Describe the component Instantiation of modeling styles.

Cont...

SECTION -C (30 Marks)

Answer **ALL** questions

ALL questions carry **EQUAL** Marks (5 x 6 = 30)

11 a Enumerate the operation of MOS Transistors.

OR

b Discuss about behavioral and structural Domains.

12 a Outline the concept of well and channel formation.

OR

b Elucidate the CMOS Design rules.

13 a Analyze the working of NMOS logic gates.

OR

b Summarize the X points on FPGA.

14 a Point out the Basic Terminology in VHDL.

OR

b Categorize the function of data types in VHDL.

15 a Explain the function of Architecture body in behavioral modeling.

OR

b Highlight the function of concurrent signal assignment statement.

Z-Z-Z END