18CAP03

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MCA DEGREE EXAMINATION DECEMBER 2018
(First Semester)

Branch - COMPUTER APPLICATIONS

COMPUTER SYSTEM ARCHITECTURE

Time: Three Hours Maximum: 75 Marks

SECTION-A (10 Marks!
Answer **ALL** questions
ALL questions carry **EQUAL** marks (10 x 1 = 10)

1 In computers, subtraction is generally carried out by
(i) l'scomplement (ii) 2'scomplement
(iii) 9's complement (iv) 10's complement

2 The circuit used to store one bit of data is known as
(i) decoder (ii) encoder
(iii) Flip flop (iv) register

3 Floating point representation is used to store
(i) Boolean values (ii) Whole numbers
(iii) Real integers (iv) Integers

4 Stack-organised computer uses instruction of
(i) zero address (ii) two address
(iii) indirect addressing (iv) index addressing

5 A machine language instruction format consists of
(i) operand field (ii) operation code field
(iii) operation code field and operand field (iv) none of the above

6 The instruction form 'register to register' has a length of
(i) 1 byte (ii) 2 bytes
(iii) 3 bytes (iv) 4 bytes

7 In Reversh Polish notation, expression A *B + C * B is written as
(i) AB*CD*+ (ii) A * BCD * +
(iii) AB * CD + * (iv) A * B * CD +

8 The addressing mode used in an instruction of the form ADD XY, is
(i) absolute (ii) indirect
(iii) index (iv) none of the above

9 Which of the following is lowest in memory hierarchy?
(i) cache memory (ii) secondary memory
(iii) Registers (iv) RAM

10 The fastest data access is provided using
(i) Caches (ii) DRAM's
(iii) SRAM's (iv) Registers

SECTION - B (25 Marks!
Answer **ALL** questions
ALL questions carry **EQUAL** Marks (5 x 5 = 25)

11 a Explain logic gates with truth table and algebraic function

12 a Discuss logic microoperations with example.

OR

b Convert the following binary numbers to decimal :
(i) 101110 9ii) 110110100

13 a Explain the instruction format.

OR

b Explain the phases of instruction cycle.

14 a Draw and discuss the block diagram of DMA controller.

OR

b Explain parallel priority Interrupt.

15 a Explain the hardware organization of associative memory.

OR

b Discuss the characteristics of multiprocessors.

SECTION -C (40 Marks!

Answer **ALL** questions
ALL questions carry **EQUAL** Marks (5 x 8 = 40)
Question no. 16 is compulsory

16 Simplify the following Boolean function and draw the logic diagram with
(i) AND - OR gates (ii) NAND gates
F (A, B, C, D) = £ (0, 2, 8, ***9,\0,*** 11, 14, 15)

17 a List all arithmetic micro operations with example.

OR

b Elucidate the arithmetic logic shift unit with diagram and function table.

18a Write an assembly language program to subtract two numbers and explain.

OR

b Discuss the major tasks performed by the assembler during the translation process.

19 a Explain addressing modes with example.

OR

b How data transfers to and from peripherals are handled? Explain.

20 a Explain associative and direct mapping cache organization with relevant example.

OR

b Discuss Interprocess synchronization and mutual exclusion with semaphore.

Z-Z-Z END