I4KLP10

PSG COLLEGE OF ARTS & SCIENCE
(AUTONOMOUS)

MSc DEGREE EXAMINATION DECEMBER 2018
(Second Semester)

Branch - **APPLIED ELECTRONICS**

ADVANCED DIGITAL SYSTEM DESIGN

Fime : Three Hours Maximum : 75 Marks

SECTION -A (30 Marks)

Answer ALL questions

ALL questions carry **EQUAL** Marks (5 x 6 " 3 0)

1 a Explain the structural description styles of system hardware with the verilog I IDE .

OR

b Mention any four types of operators in v erilog UDE code.

2 a Illustrate the initialization of sequential primitives with relevant examples.

OR

b Explain the verilog model, for net delay, module paths & delays.

a Write the program in verilog for 4 to 1 multiplex using gate level modeling.

OR

b To compare sequential UDP & combinational UDP.

4 a What are the advantages & disadvantages of net declaration method assignment?

OR

b Explain the case statement syntax with example for it.

5 a With the help of the flow chart describe the system task for digital system design.

OR

b Write a notes on reducing vectors from a text file in verilog with examples.

SECTION -B (45 Marks)

Answer any **THREE** questions

ALL questions cany[7] **EQUAL** Marks (3 x15 45)

6 Explain the different types of test bench in VI IDE for simulating a module.

7 Discuss about verilog HDC data types with suitable example^.

8 Implement NAND, AND, OR gates using MOS switch test with its suitable test bench.

9 Describe the loop statement in verilog with suitable diagram.

10 Detail about sharing task & it’s functions.

END