Indian Institute of Science

Design of Photovoltaic Systems

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NPTEL Online Certification Course

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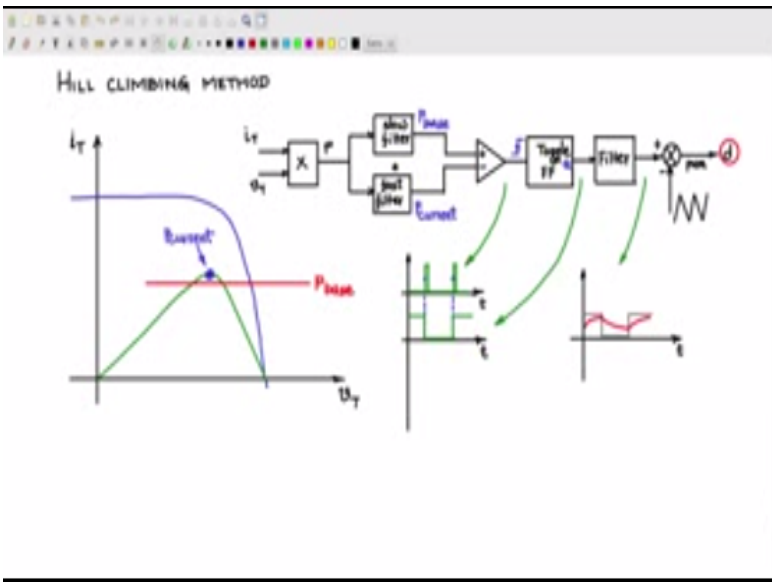

We shall now look at this spice simulation of the hill climbing method of maximum power point tracking. We will use this algorithm, we will use all these blocks, we will measure the current, measure the voltage, calculate the power, pass it through a slow filter and a fast filter, comparator, toggle flip flop filter, and then PWM and giving it to the duty cycle input of a DC-DC convertor.

The DC-DC convertor where we will choose is the buck boost converter, because it is able to operate on the entire IV characteristic. So let us go to spice and see how we will be able to simulate all these block and integrate it with the operation of the buck boost converter interface with the PV source.

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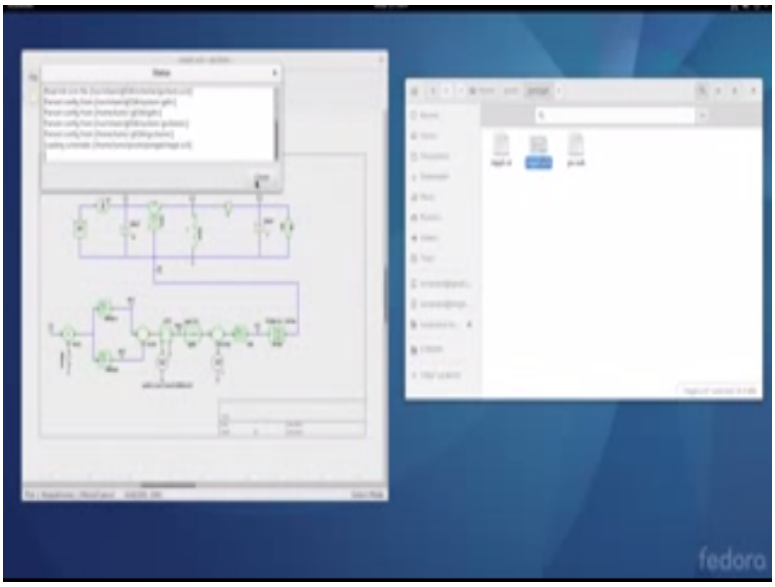

So in the simulation folder I have one folder call PV MPPT, within that folder you will see that there is a MPPT is schematic, the sub circuit PV sub circuit file with added components, I will show you what the added components are, and then of course the MPPT.AR file.

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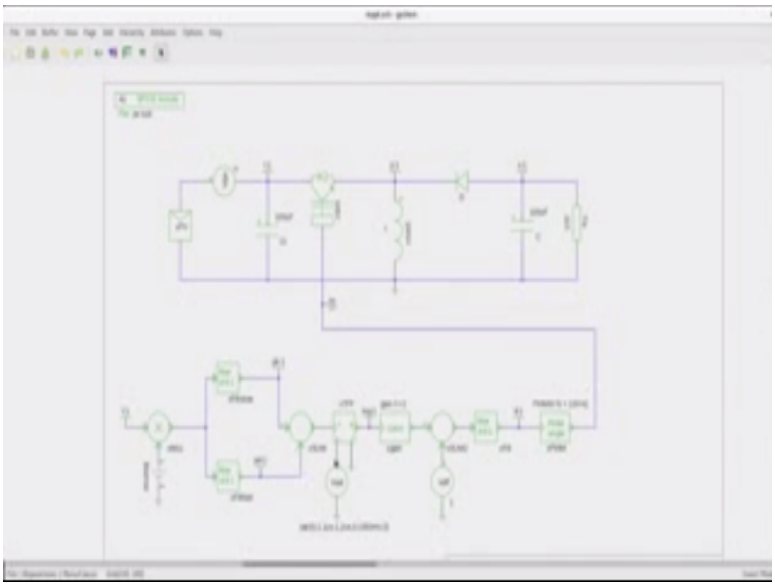

Let us open schematic file and let me zoom in observe here that this schematic is linked to PV. Sub circuit. Now this schematic here, we are familiar with this is the PV source, this is the power semiconductor switch L and the diode. This is a buck boost converter which is having V0=Vin or VT(D/1-D). The difference here is in these blocks which are ultimately generating the proper duty cycle signal for switching this IGPT.

Now how are these blocks functioning and do they agree with what we had discussed earlier. So let me put up the set of block diagram that we had discussed while discussing the hill climbing algorithm and let us compare and try to understand this.

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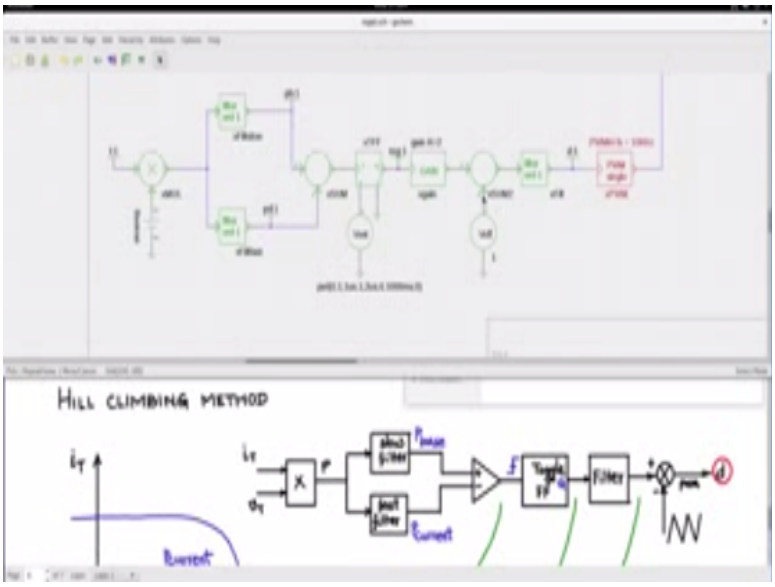

So here at the bottom part of the screen we see the block diagram that we drew while discussing the hill climbing method, and on the top part of this screen I am having the GSM, GDS GSMs schematic editor in which I have included these set of block diagram to generate the duty cycle for the buck boost convertor which is interfacing the PV source. Observe here in the block diagram that we discuss IT and VT are measured sensed and passed to a multiplier to obtain P.

Here also the voltage of this node T at VT is the terminal voltage of the PV source and V sense is sensing the current of the PV source which is the current flowing through the VIPV source which is set to a value zero. So V sense is basically a sense where it is giving an output voltage proportional to VIPV. So it is basically giving a voltage proportional to the current flowing through the PV cell or the PV module.

I am using a multiplier here. Now this multiplier multiplies VT and IPV and gives with the power output of the panel. It is multiplier block is on new block you see that NG spice integrates very nicely with the inserter and X spice. X spice inserter tools, inserter libraries or also integrated well within NG spice. These set of blocks here or analog behavioural modelling blocks and they are obtained from the X spice library. It is available in NG spice. It is well integrated and available in NG spice, I will tell you how this can be made, how this half circuit for this is.

And I will share with you the symbols on the sub circuits. So output of the multiplier gives the power. Now the power is pass through two filters, one is called the slow filter and another called the fast filter, to obtain P base and P current. Now here also I am going to pass

it through to first order filters, power is passed through a first order filter. I will call that one is slow filter and you will get PB to represent P base.

And this N power is pass through another first order filter the different N constant call it fast filter and I will say PD p dynamic. So within the filter if you see the value here it is calling the sub circuit felt underscore order underscore one is a first order. K gain of the filter is one and A which is the time constant. It is of the form one by AS +1 where A is the time constant. I am setting it at 100 milliseconds.

So this is the slow filter. The fast filter is much faster with the very low time constant. So I am setting the time constant value to one millisecond. So therefore, this is the fast filter. So output of this slow and fast filters go through a comparator + - and output of that goes through a toggle flip flop. Here also in the schematic you have + - goes through a sigma block, the output of the sigma block is analog in nature.

But I will not put a comparator here. Because the toggle flip flop here inside the input is containing Schmitt comparator. Therefore I can directly give analog signal to that. The output of the toggle flip flop, I will tell you why this is later output of the toggle flip flop goes through gain block, assuming block and then filter. In this block diagram, we are giving the output of the toggle flip flop to a filter and then to a PWM.

See in the PWM that we are using the triangle carrier is swinging from -1 to +1. Therefore, the voltage here shows to swing from -1 to +1. -1 showed to represent zero and +1 showed to represent 1 and therefore, this gain block remember, that the toggle flip flop is going to give an output from zero to one. I multiplied by a gain of two, the output of this has valued from zero to two.

I am now subtracting one from this, so it becomes -1 to +1. That is what it is given to the input the filter. The output that filter can swing from at most -1 to +1 limits which goes the PWM and goes to the duty cycle input of the buck boost convertor. Now we set here why have I given this V set, this is given to the SNR a sink that imports the toggle flip flop. At the time of switch on we do not know what will be the output state of the toggle flip flop.

In order to be consistent it is normal to give to the set import has small mono shot which will give a high hear momentarily set this and then from there on the tracking continues. So that is basically what I have done. I have given a very small, so mono shot type of signal used a piece wise linear at zero it is one after one microseconds it is one, after two microseconds it is zero and after 1000 milli seconds, one second it is still continue to zero.

So it is a very small pulse which I give to initially set Q to a high state and from there on the close loop will take over. So that is why this portion is come into picture and we offset here of one view, I just explain to you in order to get here + and - limits for the PWM signal input. So here you see that there are so many new blocks on the multiplier I already told you, this first order filter this is also new block.

These one two and three all first order filters have the same sub circuit. There is a sigma block, summer block + and - there is a toggle flip flop how do we do a toggle flip flop, there is a game block if this PWM block we have already seen earlier. So these are all based on analog behavioural modelling and they can be easily included at sub circuits in NG spice.

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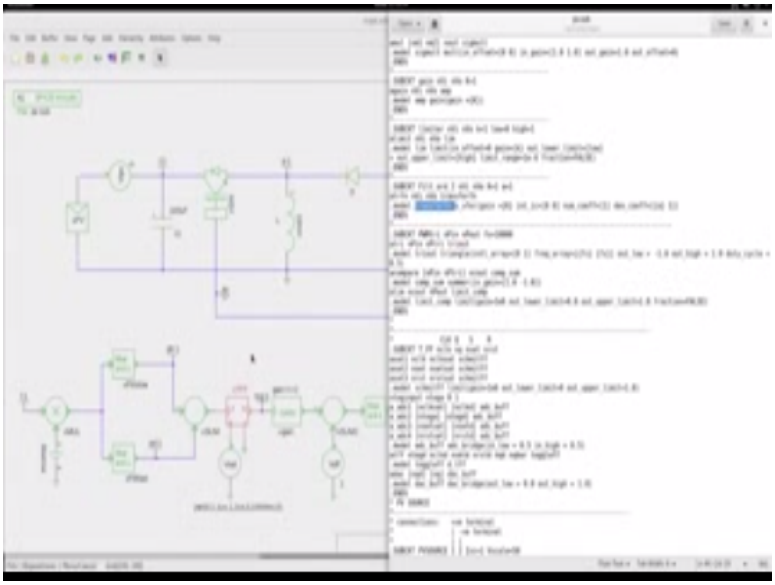

Now I will open this PV. Sub file and let us have a look at the sub circuit inside it. Let me keep it to one side okay. Now look at this multiplier block here, so this multiplier block is given here sub circuit multiplier block node one, node two, output node. So that is what this is. And all analog behavioural modelling starts with letter A okay, and I am giving the inputs as a vector output.

And then I am giving a model name and in the model I have the multiplier model which will come in. You can refer to the NG spice manual to get the ideas of this index of this. So I have the multiplier model here, I have the gain model you see that I have use gain, I have the gain model here. The flip flop I have the summer block the model of the summer block is here.

Flip flop block the model for flip flop is given here. See sub circuit toggle flip flop, the inputs clock, then Q, output AC could not set, AC could not reset. So you see there is a schmitt all the inputs are pass through schmitt comparator. The schmitt comparator model is kept here and after passing through the schmitt comparator they are pass through an analog buffer.

It is an ADC bridge every analog signal has to be passed through an ADC bridge before it is put into the digital domain. So in any mixed mode simulation keep this very important thing in mind. Any analog signal pass it through an ADC bridge taken into the digital domain and do the digital domain operation here model of the toggle flip flop is D_TFF look into NG spice manual for syntax.

And then after doing the digital you bring it out into the analog well by using a dam buffer and a dam bridge. So analog to digital conversion is by the ADC bridge and all the digital work is done and then it is brought back into the analog world by the dam bridge. These two operations are very important in any mixed mode signal analysis in spice okay. So you have the toggle flip flop and we can also have a look at the filter, you see this filter 1,2 and 3 filters are here.

I have a first order filter, it is very simple in implementation sub circuit first order, filter order 1 input node, output node, gain of one and A time constant default one. So this is the module of the filter S_X FER gain the integral initial conditions zero, zero numerator coefficient 1, denominator coefficient A and 1, so it is 1/AS + 1. This is basically from the right increasing order of the powers of S, S^0, S^1 like. So in this way the first order filter is done and the symbols for the like before, I have already done that and kept and then called it from within the symbols files.

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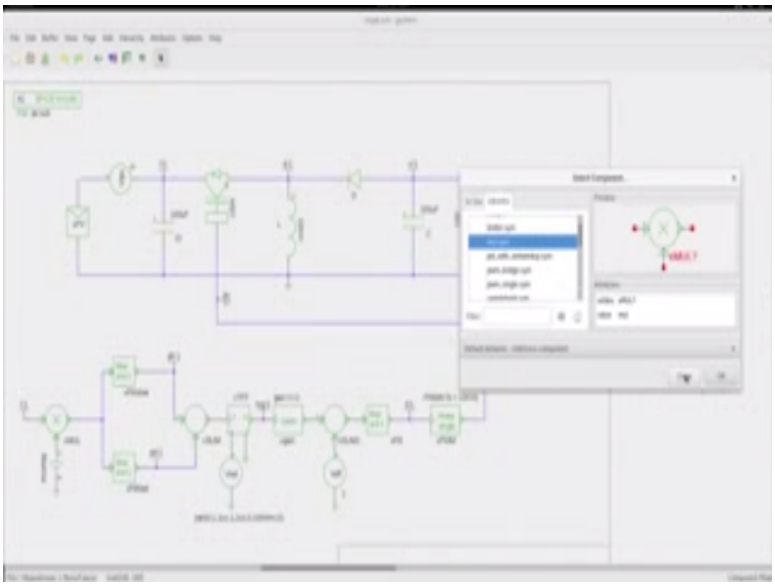

So you will see that when I open this block in the A block directory, I have see the filter symbol. I have the symbol for toggle flip flop, the symbol for summing, and symbol for multiplying. So like that the symbol I made the symbol and placed it the proper place. I will share them with you, so that you can also work on it, and then make the simulation work.

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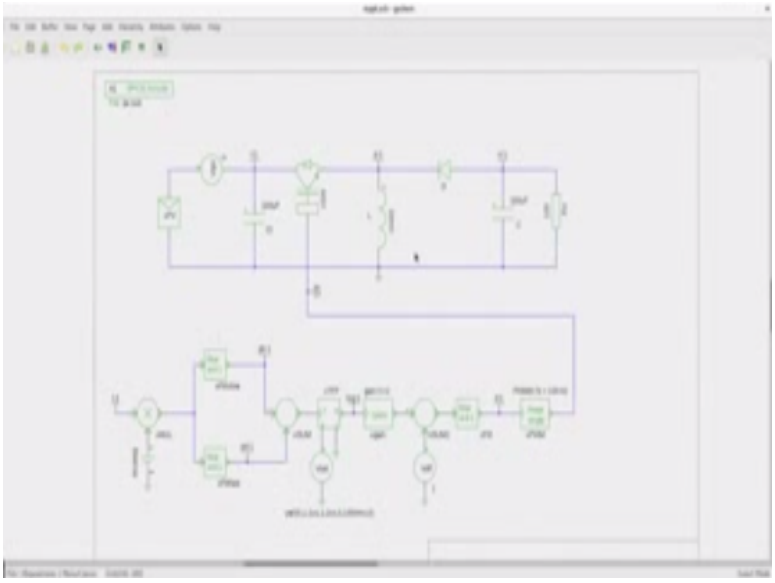

So now we will go to performing this simulation. So what is it this is existing which we are done before up to this point, we have done before. We are now going to give this in a close look fair sensing the voltage and the current. And we except that whatever may be R0, this will always go and adjust the value of the duty cycle in such a way that maximum power is drawn from the PV source.

Now that is what we want to see. So first we will say this an 100 ohms, and see that it will go and settle at some duty cycle providing maximum power, and then we will change R0 and then see that will settle at the new value of duty cycle also providing the same maximum power, now that would complete our experiment.

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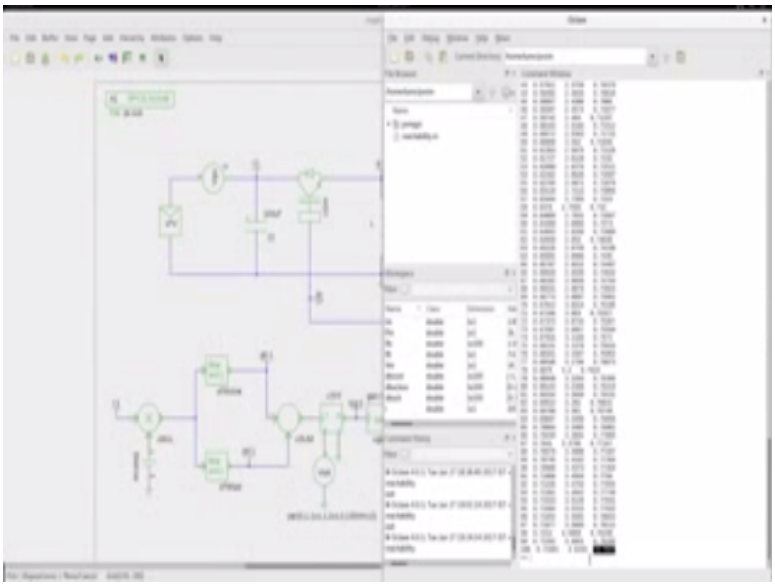

In the octave environment, I have run this reachability.M file again. So that recall that our PV source as a big power of 26.1 I have not change the ISC value and the V scale value. VM of 14.1, IM of 1.8, RTM of 7.6 ohms, and we have to look at this buck boost converter column, this last column here. Now we have put R0 of 100 ohms and therefore, you can see that the last column the duty cycle is 0.7837.

So 0.78 will work out to 0.78 x 2-1 which is around 0.56. So we expect the final duty cycle to settle down at 0.56 and deliver the maximum power point.

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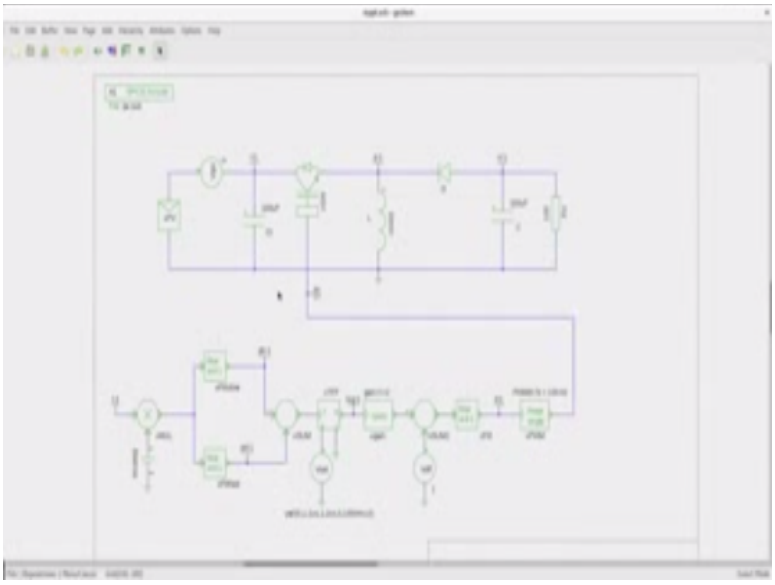

Now you should remember that this is a close loop operation now. This filter time constant, this filter time constant, this filter time constant need to be properly tuned, if you have to get good results. I have just done a draft tuning is a rough tuning and you will see that the MPPT is tracking, but I will leave it to you to do a fine tuning and see if you can get better results. Now let us go back to the terminal and simulate an NG spice.

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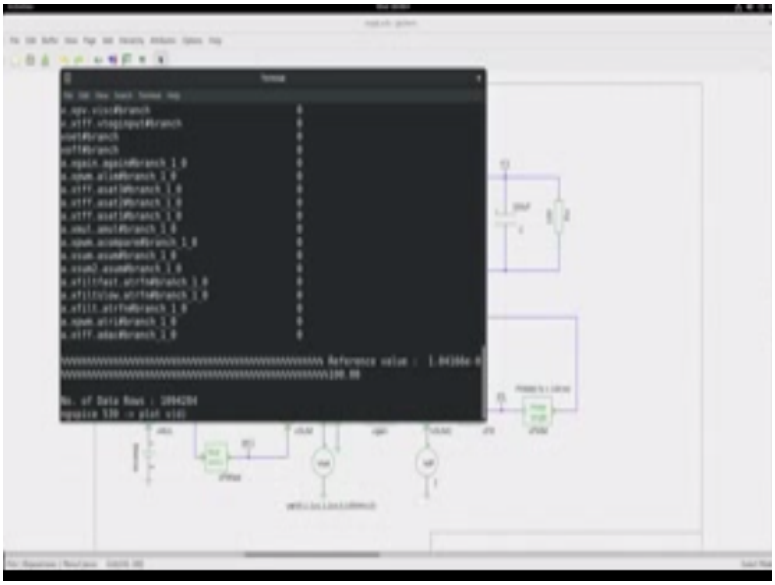

So I will use gnetlist generate MPPT.Net from the schematic we will do that. So the net 5 is generated and now I will type NG spice MPPT.cir. I have given 1000 milliseconds as a total time, and it will take some time, but we will run this. So it will run for some time few minutes, let me comeback in a few minutes. So the simulation is now about to complete and it has completed.

Now we can plot and see what is the duty cycle value here. The node for that is VG, we can plot VG and C. That would be switch pulses; instead I will plot VD here which is the DC input to the PWM. So plot V(d).

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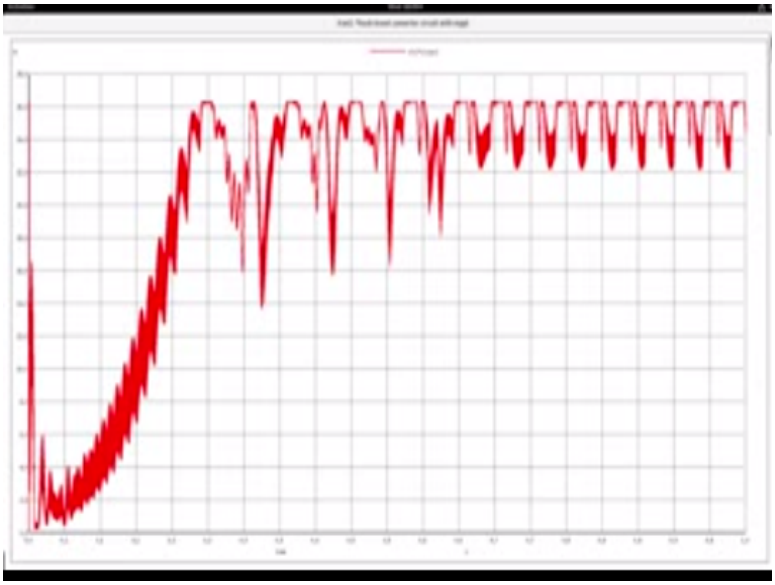

So if I expand that, so observe that the duty cycles starts from zero and then picks up and tries to oscillate and stabilize around the maximum power point operating point. So you see that I said that it should settle at around 0.56 or so. So this is settling it around that value. So you see that maximum power point tracking is happening. It is tracking the max power. We could also sense plot VT, we will now plot terminal voltage into PV current VIPV.

So this is the power that is drawn from the PV panel. So you see here again that the power gradually forwards and then finally settles at around the 26 vat value which is the peak power point of the PV source. So you see that the maximum power point tracking is happening by this algorithm by this hill climbing algorithm.

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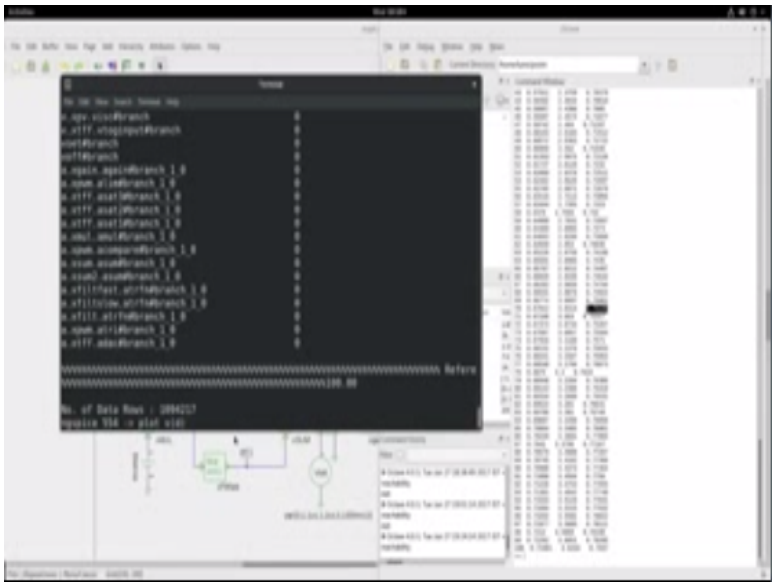

What we shall now do is change the value of R0 from 100 to some other value. Let us choose now R0 of 70. So far R0 of 70 the corresponding duty cycle is 0.75 which will work out to be 0.75 x 2-1 around 0.5 will be the value of the voltage input to the PWM carrier. So let us see if we change alter the R0 value to 70 and then re-simulate the duty cycle will settle down with new value yet still giving peek power drawing, power from the PV source.

So alter R0 to 70, now let us run, the simulation will run for some time I will come back after sometime the simulation is about to complete, it is completed. So now let me plot VD again here and see what is happened to the duty cycle.

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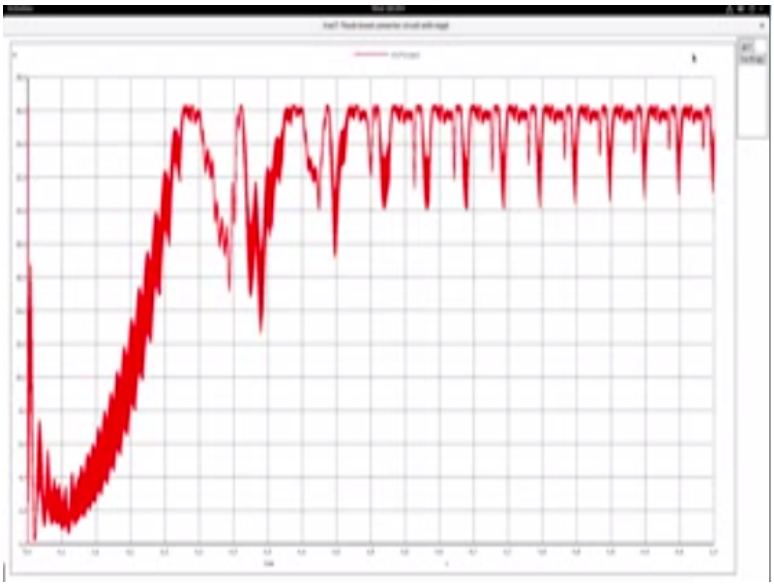

So you see that the duty cycle voltage given to the PWM block. Now it has settled to a slightly lower value, it is settle to around 0.5, and if you look at the plot of VT into current through the PV source, the power it is still over around the 26 vat level there are these disturbances here we should get adjusted if you tune the filters properly.

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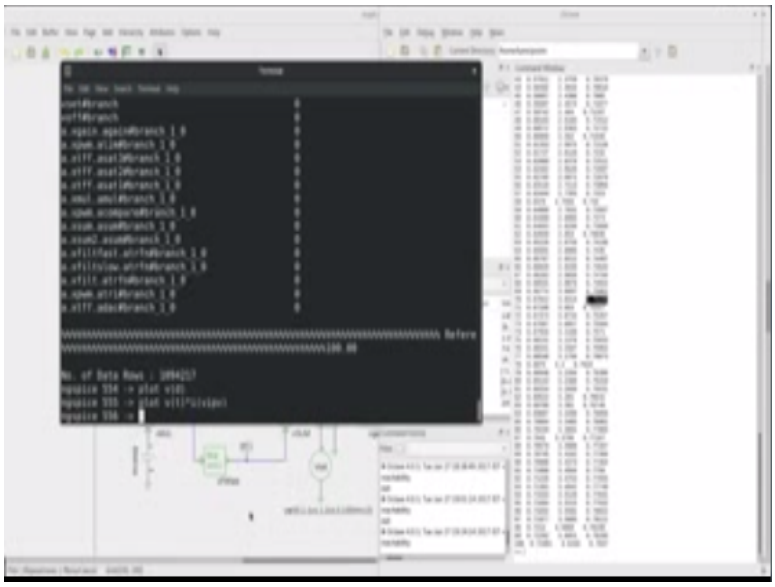

So you see that the hill climbing algorithm we have implemented, the next step we would be for you to practically implement them in hardware and try to validate the theory that we have understood and simulated.

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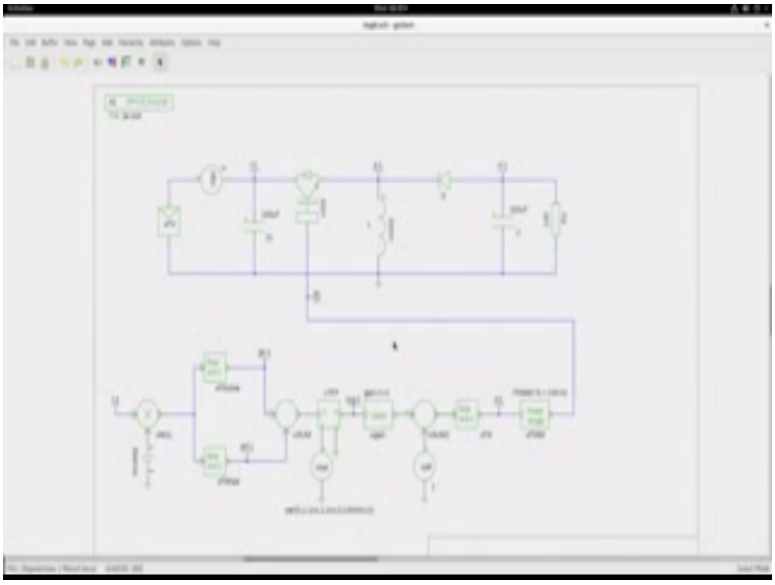

I will now leave it to you for you to explore the circuit in NG spice and try to gain more inside into maximum power point tracking.