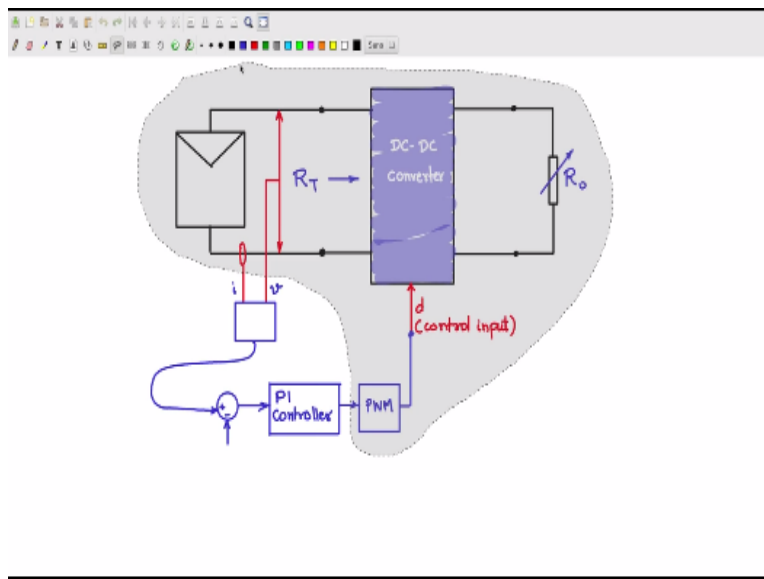**Indian Institute of Science**

**Design of Photovoltaic Systems**

**Prof. L Umanand**
**Department of Electronic Systems Engineering**
**Indian Institute of Science, Bangalore**

**NPTEL Online Certification Course**

(Refer slide Time: 00:17)



Let us see how we can simulate the dc-dc converter interfacing the PV source and the load. Earlier we saw how to make the PV source, the symbol, and the sub circuit. And we will use the that PV source to power up the dc-dc converter and deliver power to the load or not. We shall simulate the PV source dc-dc converter in open loop we just have a PWM, we shall not close the loop which we will come to later after having discuss the MBPT tracking algorithms.

So what we can take up for simulation is the PV source, we can have an PWM and the dc-dc converter this shaded region we will simulate in the spice.

(Refer Slide Time: 01:21)
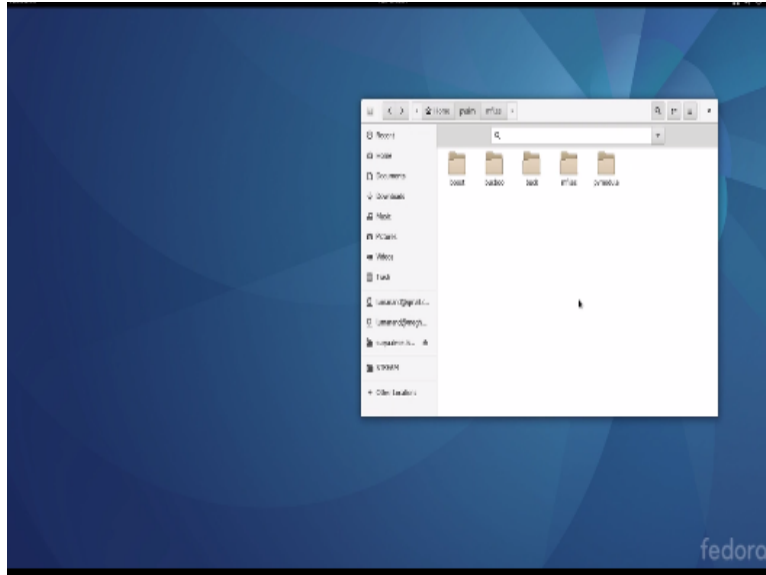
In the simulation folder I have created four more folders the boost folder for simulating the boost converter interface to the pv module, baa boost converter interface to the PV module, the baa converter and there is an M file here in this folder which will check for reach ability of the duty cycle for any given converter.

(Refer Slide Time: 02:02)
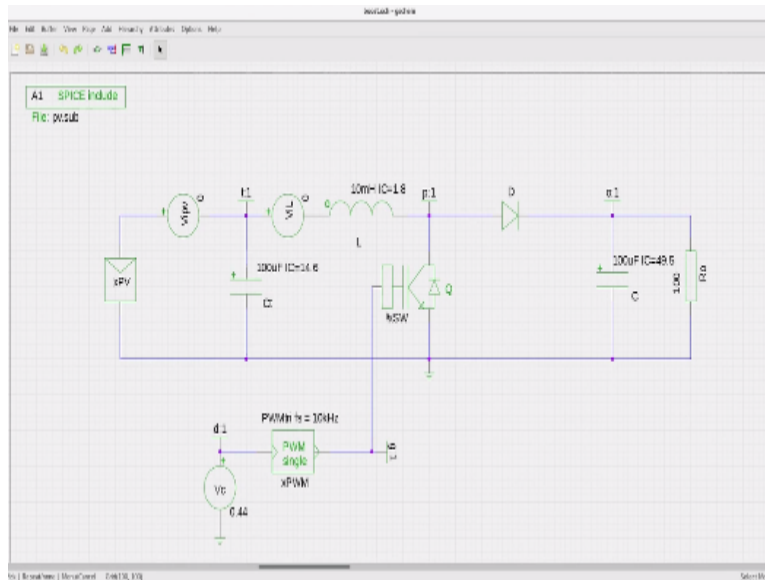
Let us look at the boost converter 1ˢᵗ I have here the schematic file let me zoom that yeah. Now we will see that this is schematic of the boost converter, inductor, switch, diode, capacitor, load. So this portion is the boost converter, I have capacitor here across the terminal of the pv to improve the repo input repo, this is the PV source, module, the model of which we design earlier. Pv.sub is the sub circuit file which contains the sub circuit model of these and few others it also contains the model for these power switch it also contains the model for these PWM.

I have here a voltage source which is set to a value 0, voltage source set to a value 0 can be used for sensing the current through that branch. So we ITV sensing actually the PV current IPV and VIL is actually sensing the inductor current. This is also a current sense voltage source value set to 0, I have put some initial condition values on the energy storage element capacitance, I have this initial conditions, inductance I have the initial conditions 1.8 amps and capacitors also I have put these initial condition 49.5 volts at the output.

So that the simulations will be smooth and fast you will not see lot of oscillation during the turn on process. So for the R0 of 100 ohms, I have calculated that the VC value should be 0.44 to give duty cycle of 0.72. What is the relationship between the duty cycle and the VC voltage, let me just show you.

(Refer Slide Time: 04:13)
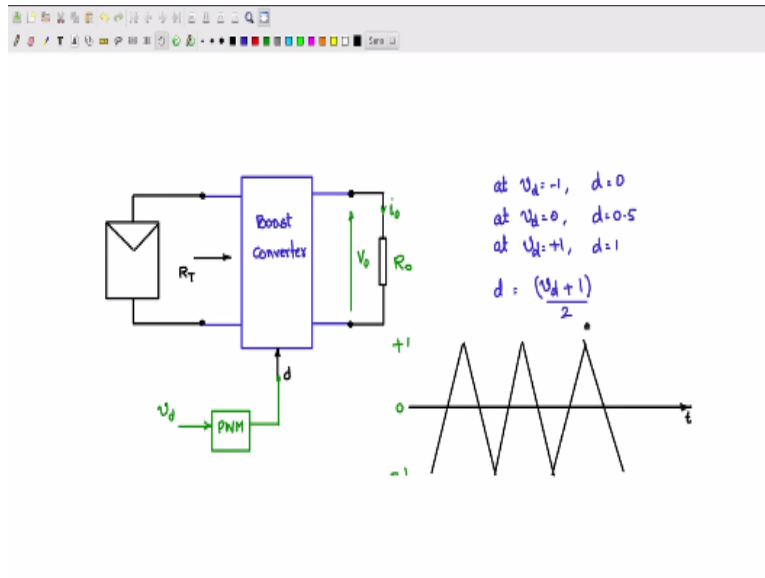
Boost converter and the PWM block here, now VD setting actual the duty cycle. So inside the PWM block there is an triangle carrier something like this so let us say the triangle carrier is going + - in this passion, this is -1 this is 0 this is +1. So your VD value is at -1 then duty cycle is 0 at VD here in between 0 and the duty cycle is ½ which is 0.5, and at VD =+1 longer tip D=1. So therefore we get the relationship we D duty cycle is VD+1/2.
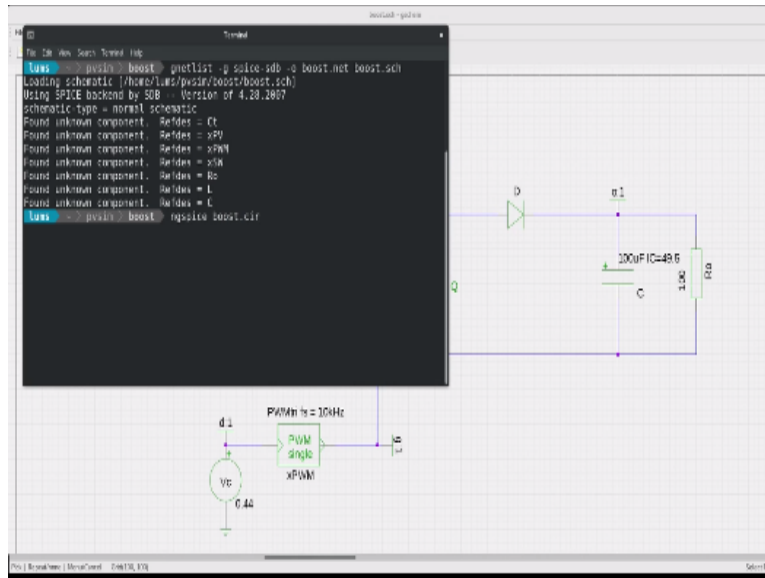
(Refer Slide Time: 05:19)
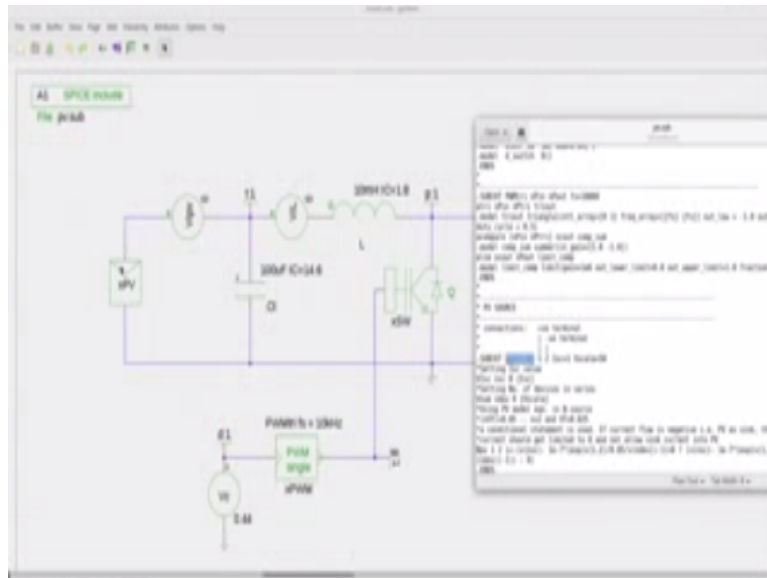
The PV source we know what is the value of the short circuit current and the voltage scale value, and we have simulated the PV source and seeing the IV characteristics. So you know the short circuit current value and the open circuit current value and also the peak power point value. So using those values we can calculate what should be the value of T.

In the PV sub file, sub circuit file we have power _SW these is the sub circuit for the power semi conductor switch. So the power _SW is the sub circuit for the semi conductor switch, this PWM tri, triangular PWM is the sub circuit for these block PWM single face where we have as parameter, the carrier frequency, and then we go for the down you have the PV source the sub circuit PV source is the one we made earlier and that is for these XPV the PV source. Now let us go to the terminal and simulate the circuit
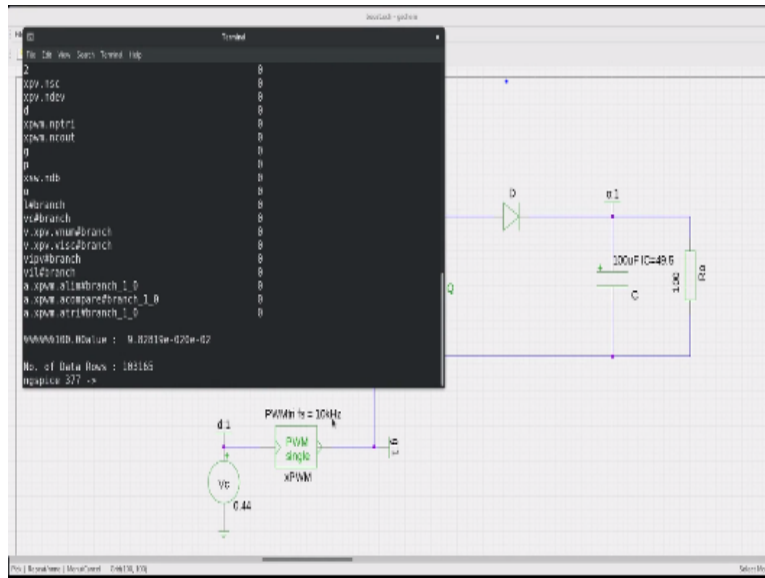
(Refer Slide Time: 07:34)

I have open the terminal let may go to the folder boost , I will generate the net list boost.net using G net list execute that, now going to NG spices boost.cir.
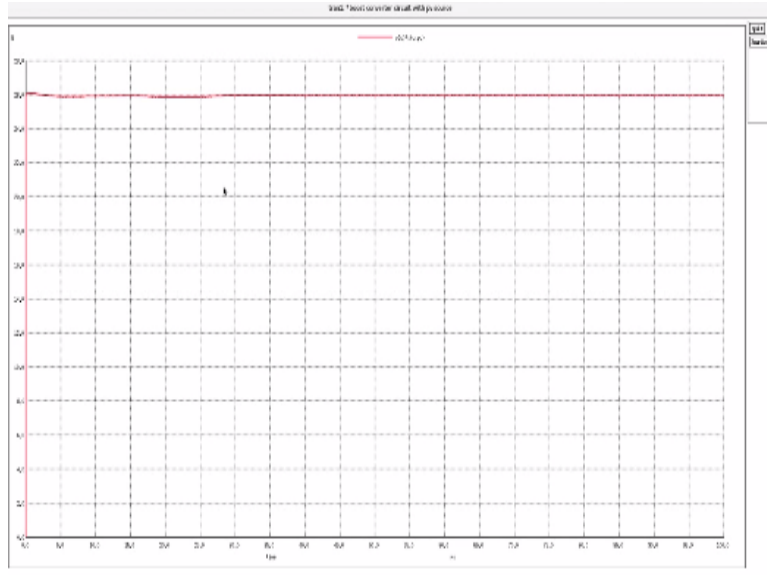
(Refer Slide Time: 07:35)
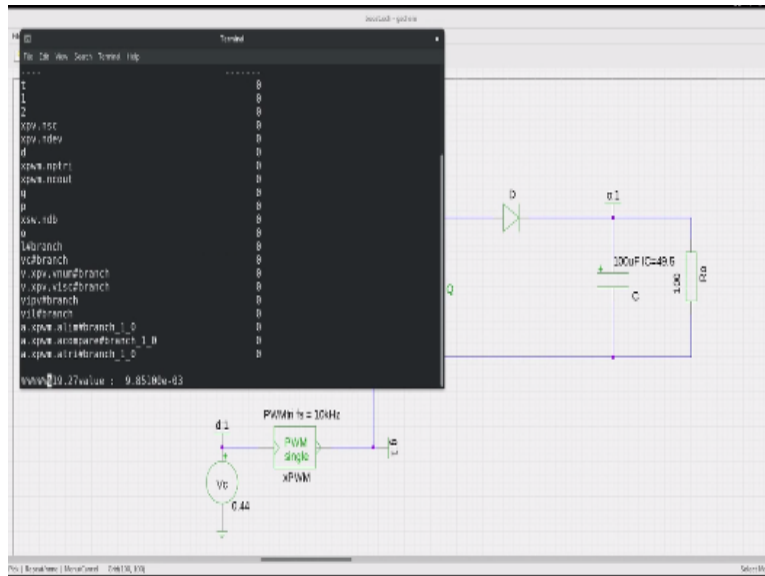
So it will perform the simulation and then we have the, so on. Now let us plot what do you want o plot I could plot the input current VIPV into the voltage terminal that will give the power.
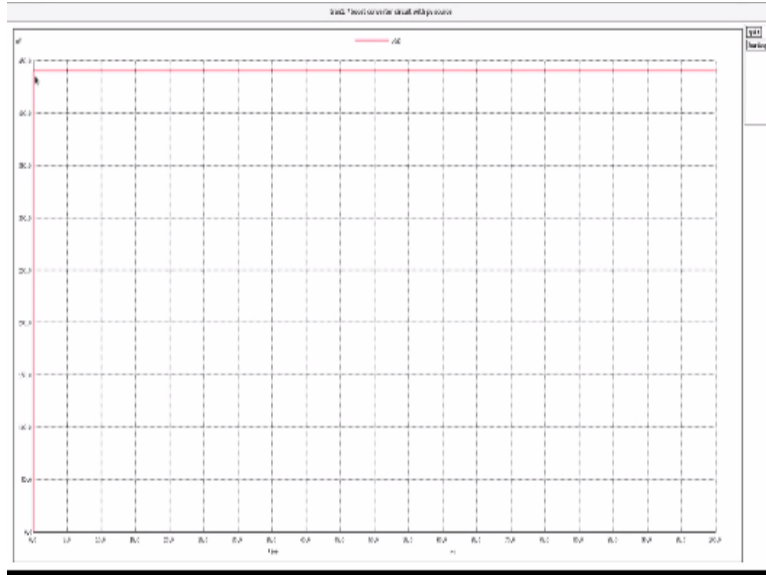
(Refer Slide Time: 08:02)

So let us plot VT terminal voltage into current through the VIPV source the IPV sensor.

(Refer Slide Time: 08:23)

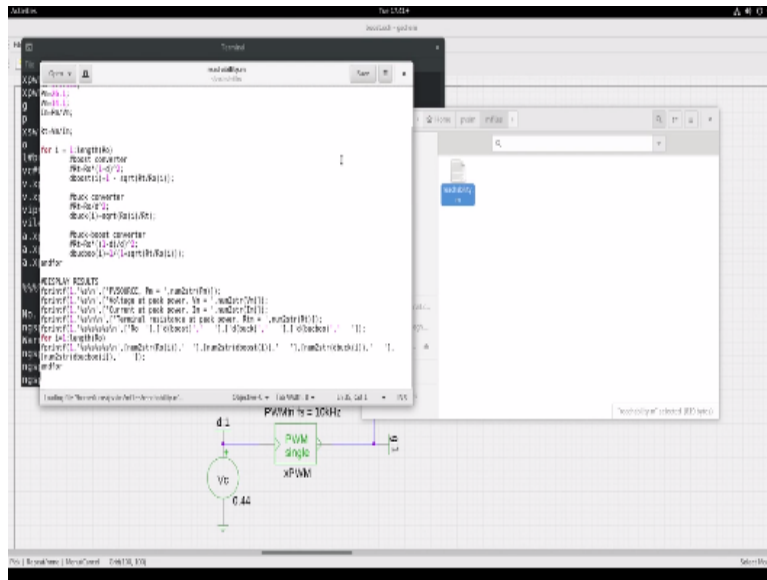So you will see that the input power is hovering around 26 vats, you saw earlier that this PV module that we used had a peak power of around 26 vats. So at these particular duty cycle it is presenting an optimum or T value terminal resistance as seen from the PV module such that max power gets transferred.

(Refer Slide Time: 08:56)

We shall observe the way form here at the input PWM to see that.

(Refer Slide Time: 09:05)

It is 0.44 or 440 mv that we have said. And at this value the duty cycle is 0.72, how did we get this duty cycle 0.72, again from the relationship let me show you how.

(Refer Slide Time: 09:29)

Let me go into the M file I will open the regionability.M file, you know a script file.

(Refer Slide Time: 09:38)

So you see here, I am making the R0 vary from 1 to 100, and this is the characteristic of the PV module that we are used is 26 vat panel 14 vm voltage at peak power IM is calculated PM/VM RTIS VM/I, the terminal resistance. Then for every value of R0 we excaudate this what we find out, we find what is the duty cycle for the boost converter using that relationship $RT=RNOT1-D^2$ find that the duty cycle $1-\sqrt{RT/RNOT}$ like that you can do converter for the boost converter also.

And I will present the results on to the octave works space, so let us open octave and run these so let us see what happens.

(Refer Slide Time: 10:47)
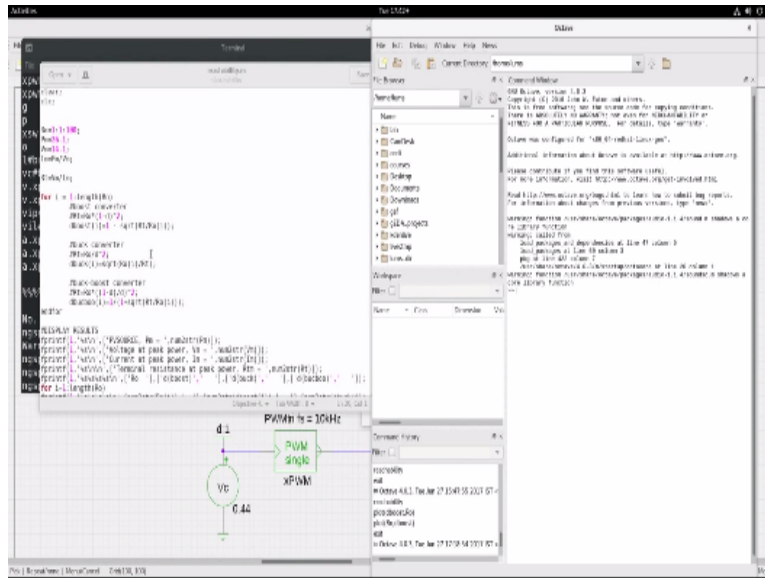
Let me have octave, let me go to the M file where you have reachability.M and let me clear this work space screen and type in reachability. So you see here that we have the PV source details listed here Voltage at $p^{14}$ current at $p^{1.8}$ terminal resistance $p^{7.6}$ ohms. Now here first consider column 1 only R0 this is R0 for every value of R0 load resistance we have some value of duty cycle for the boost. You see these are not valid duty cycles.

Now let us see for R0 of 100 we will see that the value of duty cycle is 0.72 to achieve peak power operation according to this equation at peak power point. So 0.72 duty cycle would mean VC of 0.44 using the relationship that we saw for the BWM triangle which is going from -1 to +1. So that is why we had kept the VC value at 0.44.

(Refer Slide Time: 12:29)
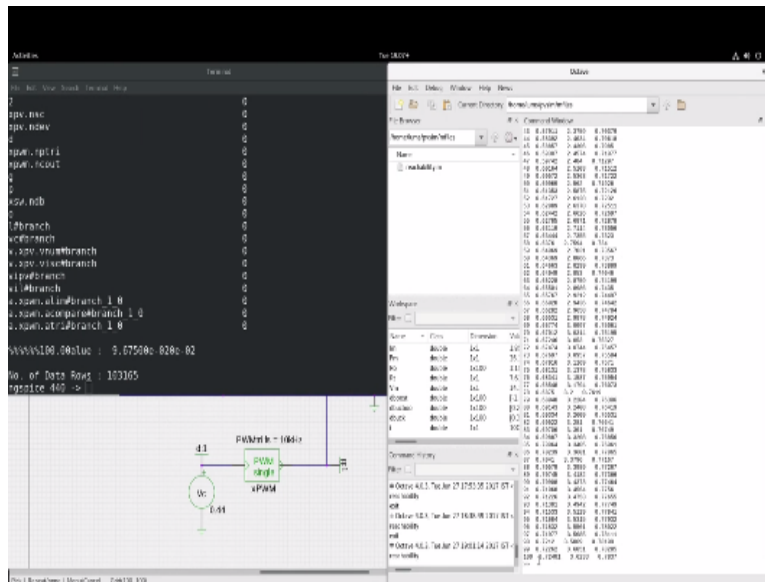
Let me now change the R0 value from 100 to something lower let us say 70. At 70 the duty cycle is 0.67 that corresponds to 0.67 x 2-1 which is 0.34, so instead of 0.44 we can change it to 0.34. But first let us change the R0 value from 100 to 70. So let me alter the value of R0 to 70 and let me run the simulation. After running the simulation I expect now that the input power coming out of the PV panel will not be peak power, so it will be less than that, so let us view that.
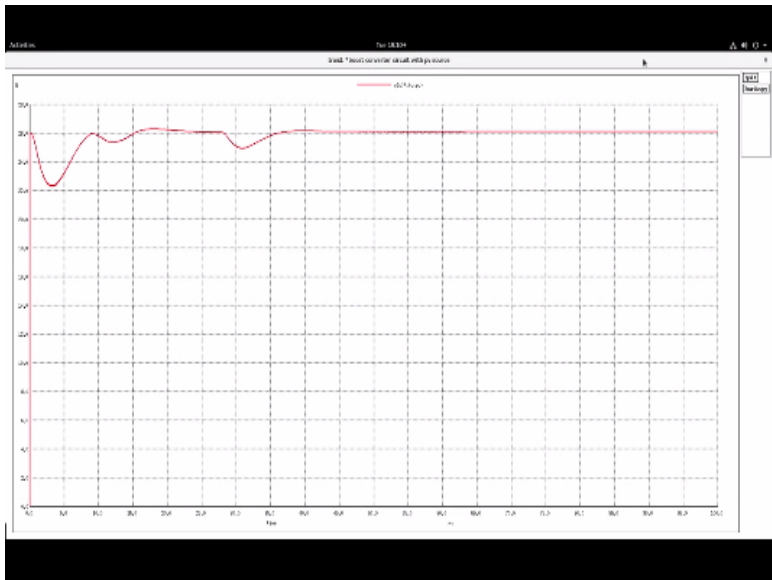
(Refer Slide Time: 13:25)
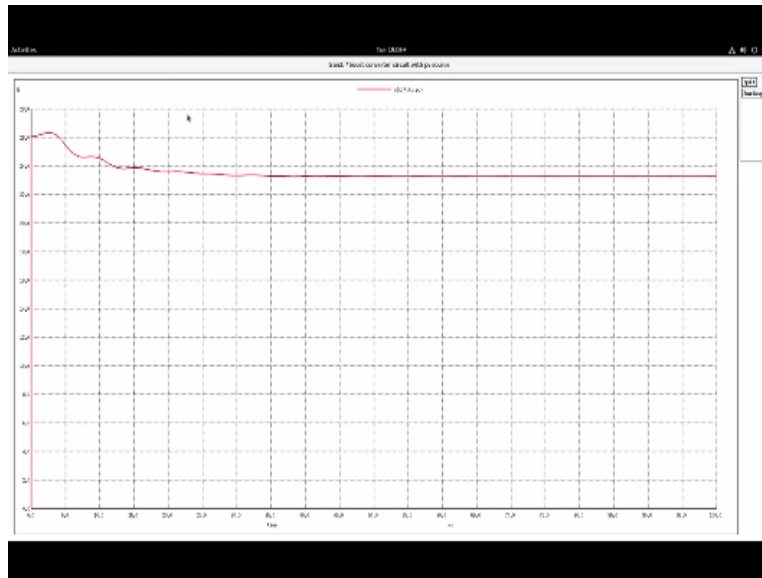
You will see that the peak power was at 26 vats. Now it is lower somewhere around 23 vats. Now let us say if we give the matching duty cycle of 0.67 then will the power come back again to the peak power operating. So let me alter VC to 0.34, this corresponds to duty cycle of 0.67. So let me change that, and let me now run the simulation again.

So now the duty cycle is matching with the R0 and therefore the RT presented to the PV panel would be optimum that is at peak power operating point. So we expect the power drawn from the PV panel to be at the peak power point. So you see here that the panel is now back to supplying 26 vats.
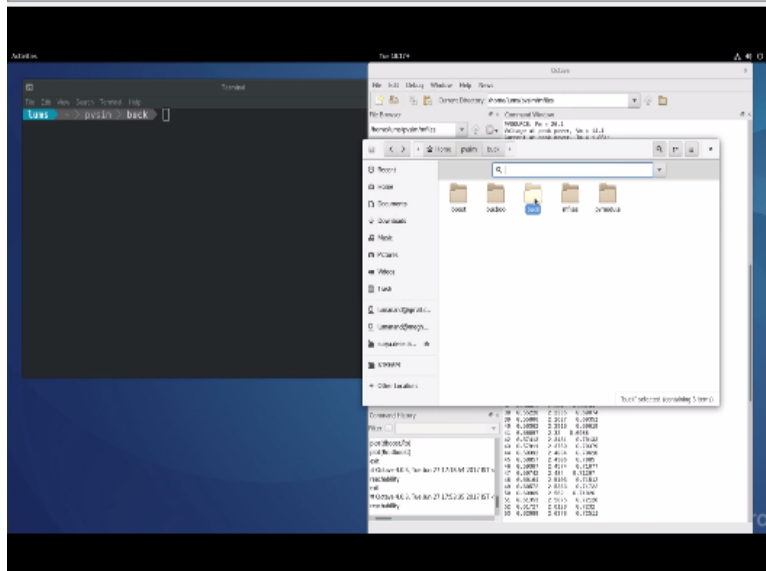
(Refer Slide Time: 14:39)

(Refer Slide Time: 14:46)
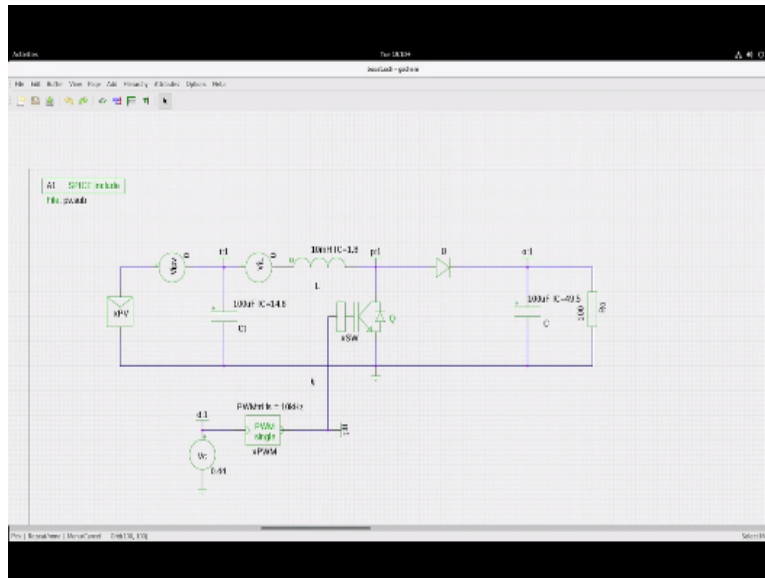
So in this way you can try to understand the various aspects of the circuit, try to observe the various currents and the voltages of this boost converter interface to the PV panel, and try to get a much insight as possible. I will leave it to you to workout with as much detail as possible and as much variation as possible for this xxx for this boost converter circuit that I will also be sharing with you in the resources section.

(Refer Slide Time: 15:19)

Let me now go into the bug folder and open the bug.schematic file and let us zoom this.

(Refer Slide Time: 15:26)
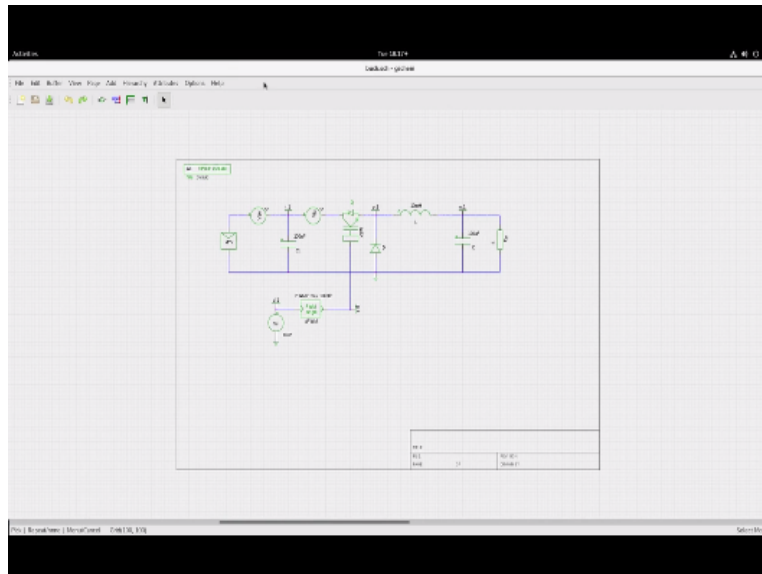
And you see it is similar to what we discussed in the boost converter only now it is the bug converter you have the switch here, the inductor and the L with the freewheeling diode in this fashion you have the same BWM and you have the VC control voltage, you have the xPV this is the PV source, it is the same PV source ISA 2 V scale 20. So now therefore let us simulate this, what should be the duty cycle I have 48.62 for an R0 of 5 ohms.

How do we fine the value of this duty cycle let us run the reachability check and then find out the values. So you see here for the value of r0 5 ohms, the duty converter for the bug converter is 0.81, for the boost converter it is an invalid duty cycle cannot use it, for the case the bug converter it is 0.81, so that will work out to the 0.62, 0.81 x 2-1 which is 0.62 .

(Refer Slide Time: 16:57)
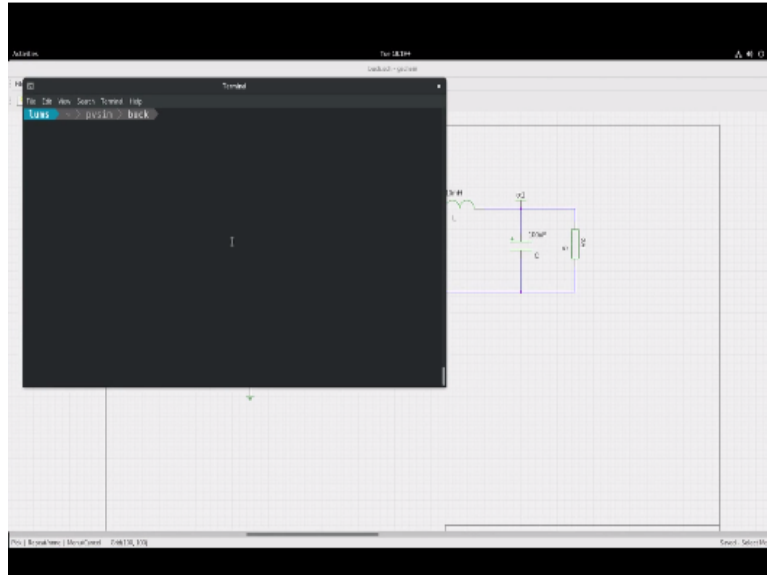
So given this let us save, go to terminal and let us simulate the circuit. First let me generate the net list using the G net list and then ngspicebuk.cir.

(Refer Slide Time: 17:13)
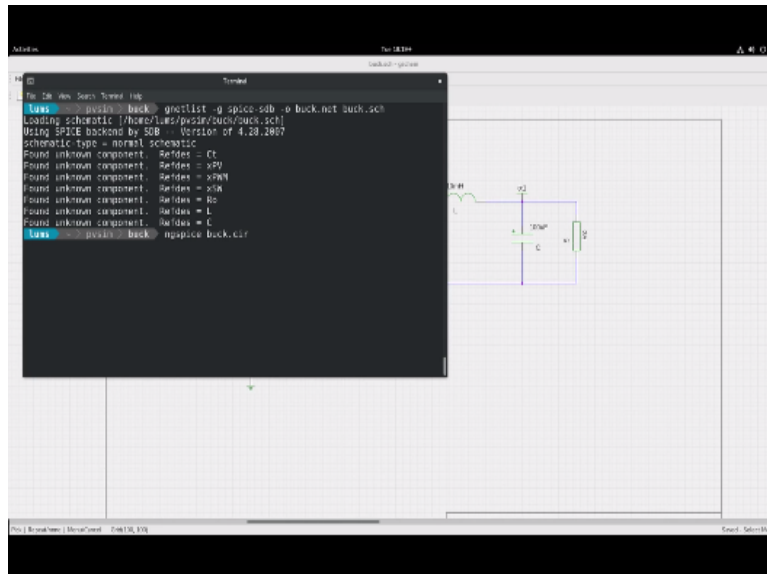
So the simulation goes through and we would like to observe the input power, the power out of the PV panel.
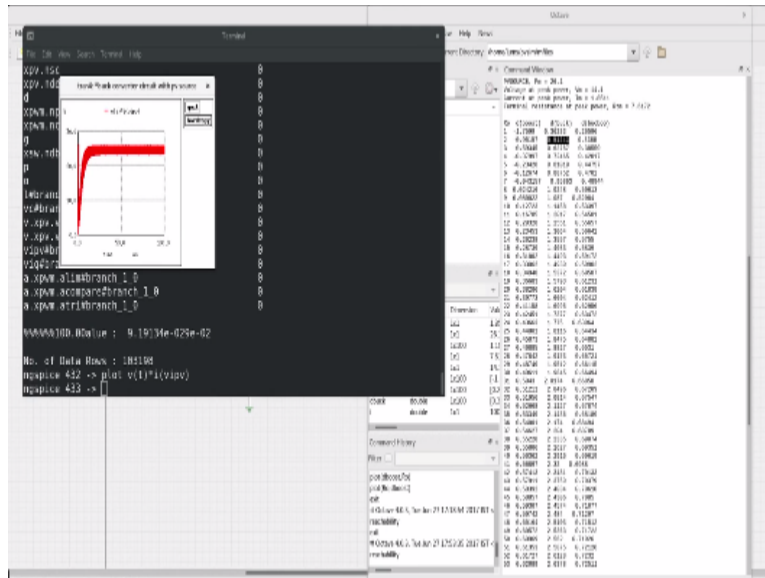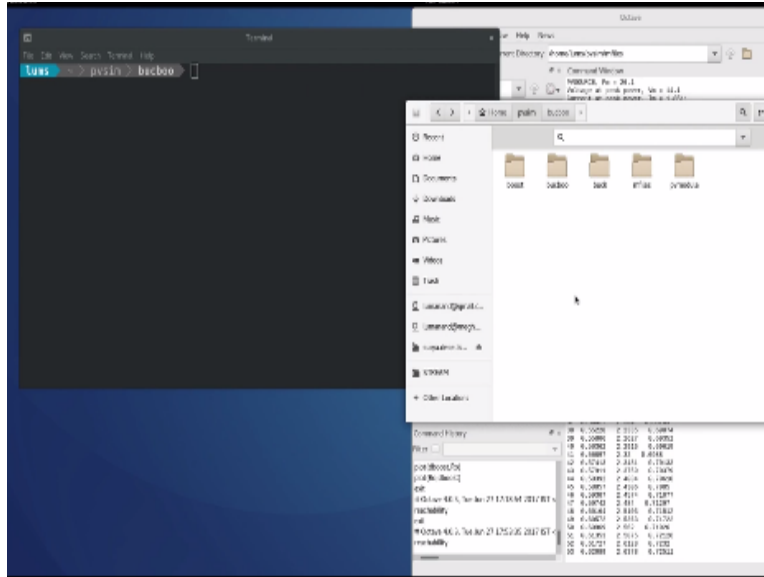
(Refer Slide Time: 17:31)
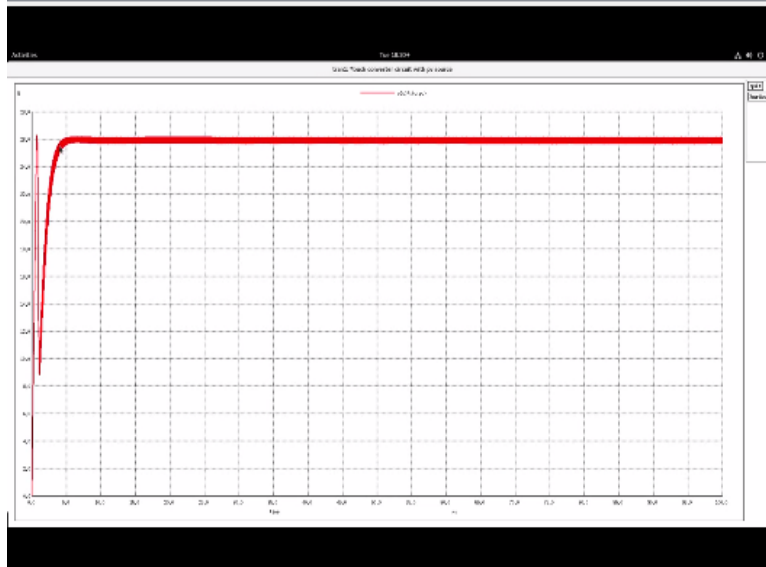
So let us check that out you see that it is now hovering at around 26 vats which is the peak power point.

(Refer Slide Time: 17:38)

You can cross check plot the voltage of the control voltage it is at 0.62, what happens if I set R0 to 20 ohms? At 20 ohms the duty cycle record is 1.62 for the bug converter which is an invalid value, the duty cycle should be between 0 and 1. And therefore you will not, if R0 is 20 ohms you will never be able to achieve the peak power. However at the given same value duty cycle, if you put R0 as 20 the power lawn will be vey less.

For example, alter R0 to 20 and the duty cycle control voltage VC is till 0.62 run, and you will see VD is same 0.62, and let me plot the input power, you see the input power is not below 10 vats which is really poor. On the other hand let me change R0 to 2 ohms, 2 ohms where the duty cycle for the bug converter is 0.51. So let us say I change alter R0 to 2 ohms run the simulation, you see that it is much lesser than the peak power point.

However, if I change the duty cycle to 0.51, see let us say 0.5, 0.5 corresponds to 0 volt VC, so let us say 0 volt VC and we run the simulation, alter VC to 0 run, and again if I look at the power.

(Refer Slide Time: 19:58)

You see that it is back again to delivering peak power. So you can always match the duty cycle with the load, and by trying to match the duty cycle with the load such that RT the terminal impendence seen at the terminals of the PV module is such that it is placed at an operating point which will give maximum power. I will leave it to you to the further explore this bug converter circuit and try to get more insight out of it.

(Refer Slide Time: 20:34)

Let us now look at the bug boost converter interfacing the PV panel to the load. So let us go this one an open the schematic of the bug boost converter and let me zoom it like this.

(Refer Slide Time: 20:45)
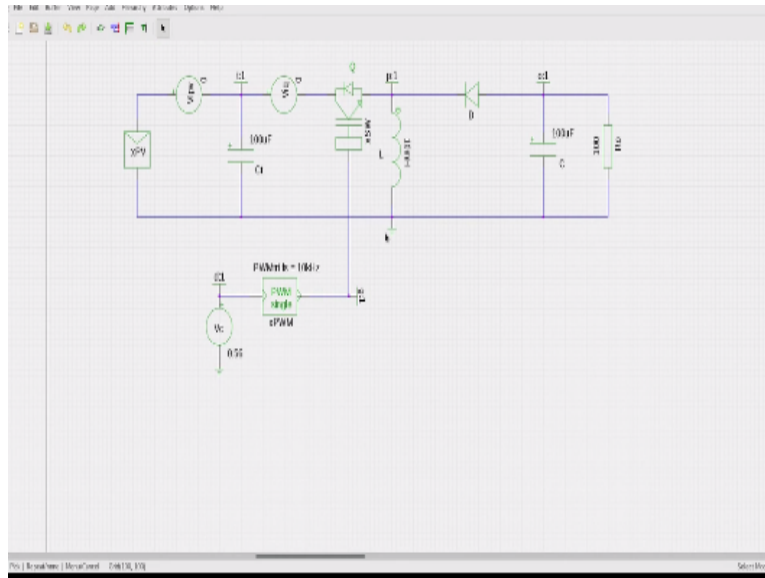
So this is the bug book converter observe that there is a switch here in line with the import , you have the inductor and the diode in this polarity you see that the inductor free wheel through the diode in the fashion, the voltage across the capacitor is negative. Now same PV source we have used, so this is ISA at 2 amps we scale 20. Same as before rest of the circuit similar have CT here, the terminal capacitance acting as the energy storage buffer BWM 10 kilo hertz and the VC control voltage is deciding the duty cycle.

I have set it at 0.56 again from the relationship reachability relationship. One advantage with the bug boost is that, for the bug boost the entire range of the IV curve is reachable and you will see that all are valid duty cycles. Now take for example, The octave output see that here is last column here is the duty cycle or the bug boost, and if you go through you will see that all the duty cycle values are valid values which means every duty cycle value is reachable.

Now for the 100 ohms, 100 ohms load are not that we have put the value of the duty cycle for the bug boost is 0.78. So 0.78 x 2 - 1 =0.56, so therefore we have set the VC value at 0.56 to give the peak power point. So this is like before a sub circuit power _SW the power switch and we have the PWM triangle. Now let us simulate the circuit the for 100 ohm R0 and the VC value set in such a way that duty cycle is 0.78.

(Refer Slide Time: 23:23)
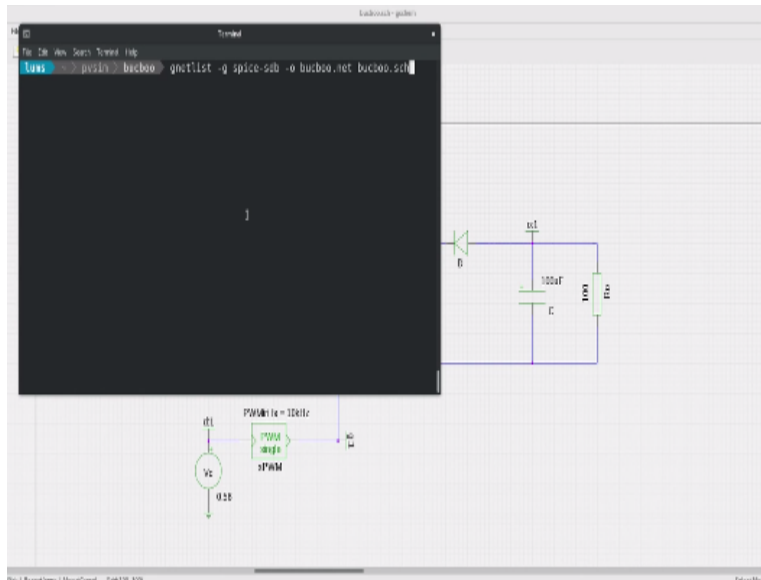
So let me open the terminal and I will use G net list to generate the net list for the bug boost schematic. So you do that, and then I will use ngspice bugboost.ar, so it will now simulate and after that is over I would like to observe the input power so you will see the input power you see here hovering.

(Refer Slide Time: 23:59)
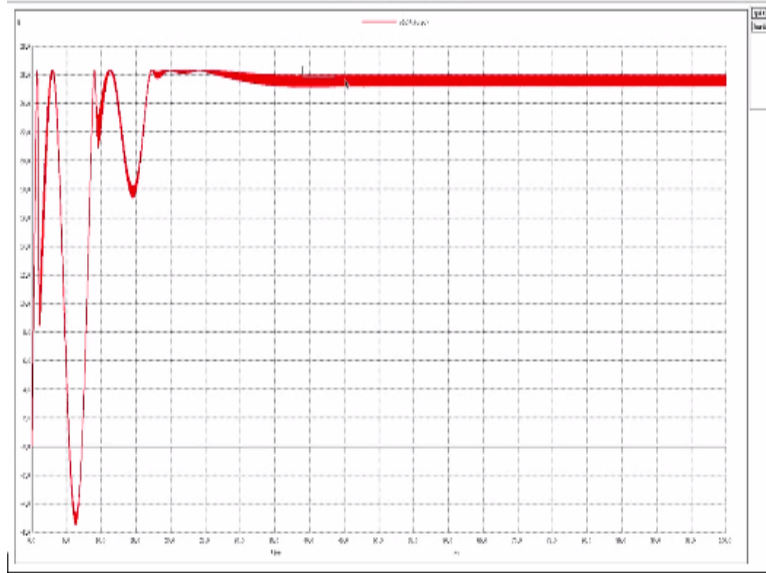
4.26 vat which is the peak power point of the panel. So you will see that there is lot of repel in the current, this is basically because of charging, discharging of the capacitance.

(Refer Slide Time: 24:22)
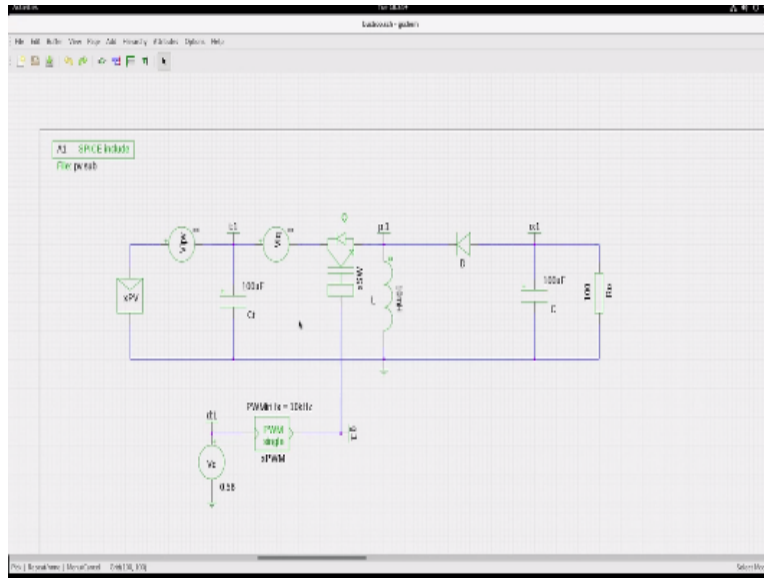
You see that there is this input capacitance storage capacitance that we have put one may have to adjust its value to lesser repel or higher repel. So that is why this repel is present here, now let us say that I go right down in or not let us say will take this R0 of 8 ohms, for R0 of 8 ohms in the case of bug boost you have 0.50 as the duty cycle when you express it for the VC it will be 0. So let me first alter the value of R0 to 8 ohms from 100 ohms. And then run the simulation, and then after running the simulation let us observe the input power.

(Refer Slide Time: 25:19)
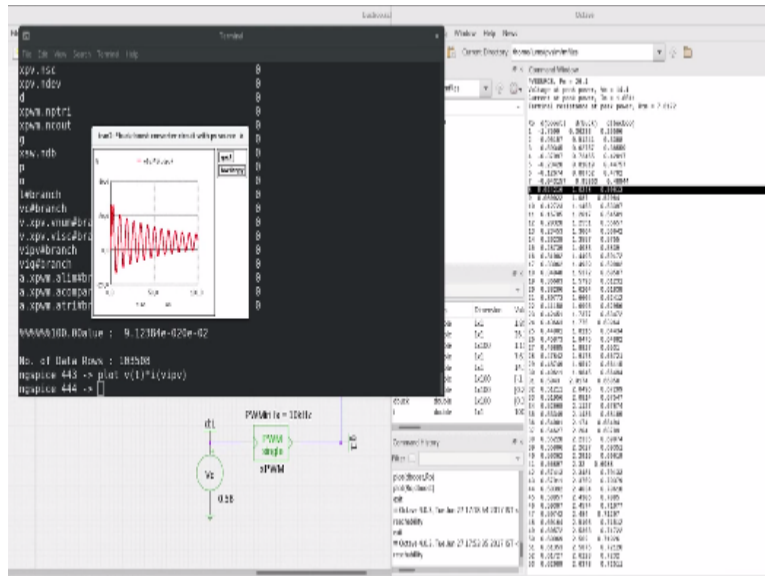
The input power is way below the maximum value it is settling down somewhere to a very low value even bellow 10. So let me now observe that the duty cycle voltage is at around 0.56 or 560 million as the value control voltage value. Let me adjust it to this value what is supposed to be 0.5 duty cycle which means VC (0). So I will alter VC to 0, and then run the simulation, and you should see that the input power is brought back to the peak power point value, because now we are given matching duty cycle.

(Refer Slide Time: 26:16)
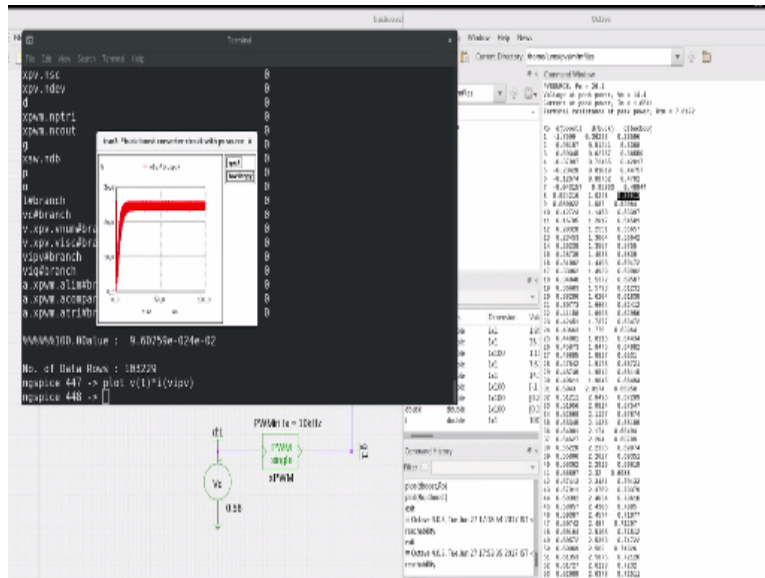
Such that RT is at appropriate load line angel slope. Now you see that the power is back again close to the peak power point. So I will leave it to you to explore this circuit also and try out various things and try to visualize the way forms and try to understand the circuit with the PV source being the input source with IV characteristics as given.

(Refer Slide Time: 26:54)
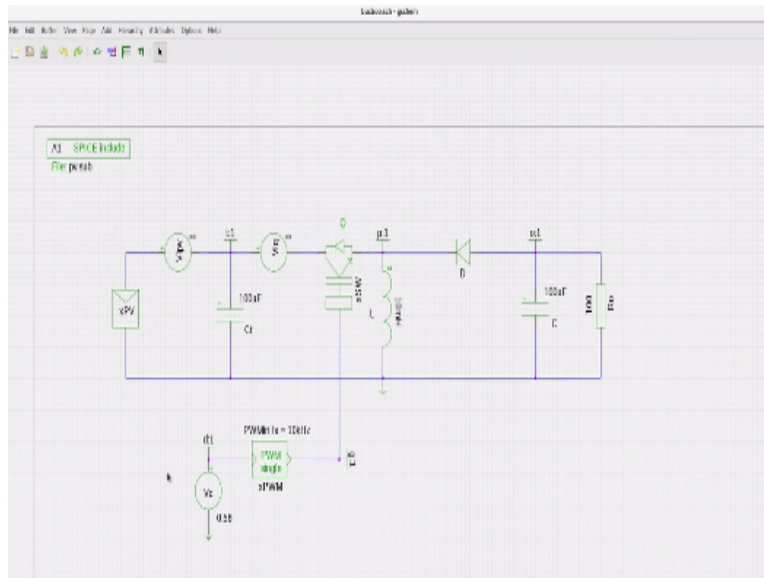
You can also explore with the different values of short circuit current and the voltage scale values and try to see what happens. This will give you more inside into interfacing the PV panels to the load by means of as switch DC-DC converter. Right now we have done the simulation of this entire PV panel DC-DC converter load combination system using a PWM block, and it is in open loop VC is just fixed value it is not closed the loop is not closed. So this is just to ensure that in under open loop or is the system okay, well designed and working as per our expectations.