Design and Simulation of DC-DC converters using open source tools

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Lecture – 04
Simulation walk-through: Rectifier C-filter example

In this video capsule, we shall take a walk through the simulation process. We shall draw a schematic and we will take the full bridge rectifier capacitor filter circuit. As an example, generate the net list and use n g spice to simulate it, see the way form, plot the way forms and try to get some inside of the circuit. One thing that you have got to understand is that simulation is for mature people, the values of the simulation or the results of the simulation is as good as the models that we put in.

So, remember that many a times we will put kind of idealized model for dilutes or the transistor or various components and expect the simulation to the way forms, which you would get or the oscilloscope of frail system. How where there will be considerable difference because there are many non-idealities and many of the uncertainties, which we will not be taking care in the simulation; keep in mind that simulation is to give you good insight on the concept or the operation of the system. It can be used for design the rating of the various components, but the real test is when you put them into the hardware; physical hardware and realize the actual way forms and results on the real hardware. So, use the simulation and simulation results with the pinch of salt and use it for understanding and design purposes.

So, with this kind of limitation you try to go ahead with the simulation. So, let us now begin this simulation work using GDA for generating the schematics and n g spice for simulating. Let us begin the simulation process by opening the GDA schematic. Last time we had used the terminal to open, but we could also go into the show applications menu. There is the GDA schematic start up, click a icon, click on that one, you will have GDA open up, we have light background GDA as we have started, set it up last time, use the mouse wheel to zoom in and how dynamically. So, first let us save it as file that we can name it as a rectifier dot schematic. So, what we can do is go into file, we do a save as I have this PC DC here. I have up PC DC, there is nothing else we can name it as rectifier dot h c s. So, it can be located in that place.

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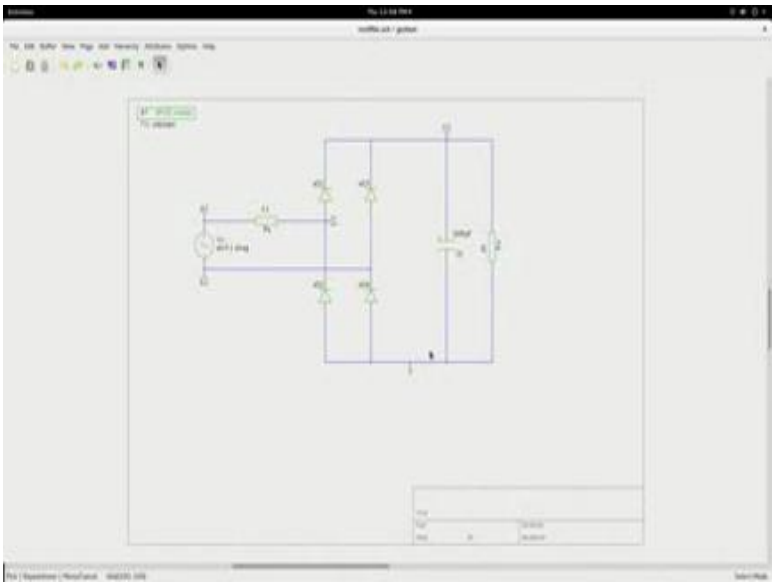

Next, we go to the components and try to draw the components from the libraries. So, first let us go and draw the circuit components which is the diode the sources and the capacitors load, them comes folder library which we had installed; yes in the last section contains the generic components. You can use it for the most of the simulation because they are generic models. Let us pick the capacitance, we need that we need a diode, a power diode, we need 4 of them. So, let us install core I am using ER to rotate the devices and I will rotate this device too, then we will need load resistance. We will put one resistance here and I will also need another resistance to put that as shunt resistance, otherwise you will land up in convergence problems. So, I will place that here you will see, we will correct it into the circuit then we need to take grow resources.

So, the resource you can take from the spice simulation elements, library resource is a sin source. We will pick a sin source, we also need to pick one more item here there is spice include directory. We need to include a file which contains the library of models customer then we would be creating. So, we will give a pointer to the file that that would be our library; our custom library. Next, we need to take from the power library the generic; this is a generic, marking the symbol which can pick out the potentials of any points of circuit. We will keep on the many a ground symbol, this is important without a ground symbol spice will not work.

So, I think we have most of them in place. So, let us position these elements. So, let me put the source here, let me have a series imperance, this will be very small imperance. Let us position the diodes some in the form of rich nature, just position them and then you can adjust it later on like this. Then one more diode, then we can have the capacitance position like this. Now, I will rotate this load register and position it like this here, this we will live it for now. Let us draw the wires.

The wires can be drawn using this add nets. So, click on that, now you are in add net mode, you see it searches and links to this net. Now, I will start putting a wires, click right click now, I will go here click right click, click, click, right click, click, click, click, click, right click and completing the wiring by right clicking click, click, right click, click, right click and so on. You make the connection for the diodes too, the diodes the subset with model that is why we have an x mark, x at the beginning all subsets tools will have x at the beginning than resources connected to the central proportional bridge and we have the circuit in place change over the cursor.

Now, the ground we could probably see ground is a virtual concept, it is just a recurrence or the 0 node with respect with the voltage hazard measured. If you keep the ground here then when you measure this node you will get directly the output voltage, we give the ground here then you will have to get the output, voltage will have to take voltage of this minus the voltage of this node that is something which you already know circuit analysis.

Now, let us place these labels here placing this labels are important because when you run the simulation in spice, the net list are generated according to the labels that you would provide. If you do not provide the labels then it will assign sub number list and when it will be difficult for you to keep track of the circuit node points. If you consciously assign labels then you will be able to get more insight analysis and know, understand the net list much better.

So, let me call this as node ‘a’ and I will copy this paste it, I will rotate it and I will call this node ‘b’ by this what I have done I have given a conscious label to this node. Now, when I want to refer to the input source I will say V a minus V b which will give me the value of the result of that way form, then we could give a node number here and let us say we call this as and we could give a node for this point will call this as, we will call

this as ‘c’. We can give one more node here I would like to place attracting here to introduce on later on.

So, for now I will just not give this label, I will give this I will remove this label and denote this label as ‘o’. So, that we know it is an output label. So, we have the labels, we have the ground, we have the components and players. We have wire dead, we have to give the component names. So, you double click on those, we will call this as R S series resistance and it should have a value and let us not give 100, it is too much of a series resistance, 0.1 ohm, sorry this double value to take care of the track.

We will come to the source later, we will give names for this diodes x, d 1 will can that d 1 will call this d 2, d 4, d 3 and the diodes are labelled then after that. Let us label this capacitance we will call it as filter capacitance C f, we will call this as load resistance. I will call it as R naught. So, we will give some value we put keep this later on 20 ohms, where you see some amount of current, we will put 1000 micro hertz capacitance like what we saw yesterday, the capacitance value and now the source we need to give some value let us first give it name V.

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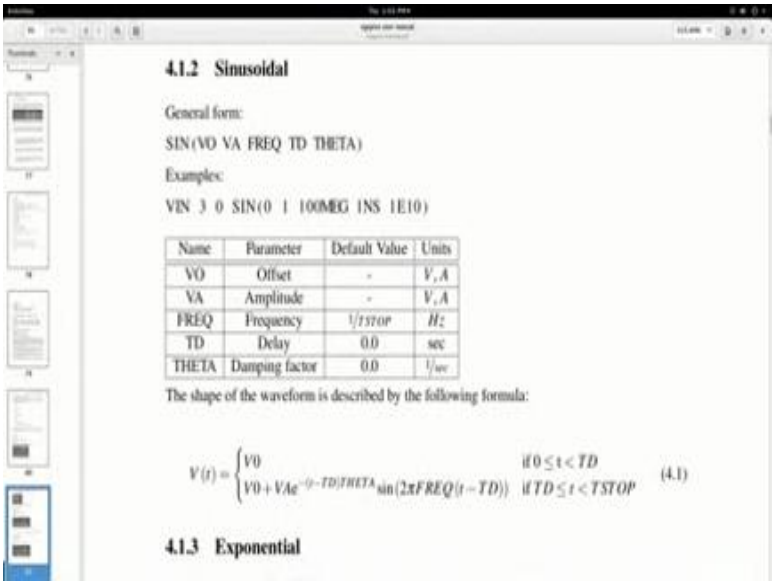

4.1.2 Sinusoidal

General form:

SIN(VO VA FREQ TD THETA)

Examples:

VIN 3 0 SIN(0 1 100MEG 1NS 1E10)

Name	Parameter	Default Value	Units
VO	Offset	-	V, A
VA	Amplitude	-	V, A
FREQ	Frequency	1/TSTOP	Hz
TD	Delay	0.0	sec
THETA	Damping factor	0.0	1/sec

The shape of the waveform is described by the following formula:

$$V(t) = \begin{cases} V0 & \text{if } 0 \le t < TD \\ V0 + VA e^{-(t-TD)*THETA} \sin(2\pi FREQ(t-TD)) & \text{if } TD \le t < TSTOP \end{cases} \quad (4.1)$$

4.1.3 Exponential

So, we have the name V in and we need to provide the parameter for the sin attribute. So, here we will have to give the sin wave parameter, any doubt you can always refer to the manual, I had recommended in the last session that it is a good practice to download the n g spice manual and keep it by your side, just to look at the parameter of the sin wave or

let me go to the manual these the n g spice manual, you see the general syntax sin V offset V amplitude frequency delay and the damping factor.

So, you can give a damped sin wave also, this is an example of the sin. You have the V in between the positive node and the other node sin, the 0 offset 1 amplitude 100 meg frequency, what we need to give is 0 offset 3 V m root 2 or 325 230 root 2 or 325 volts amplitude 50 hertz 0, 0. So, that is what we will do. So, we shall make it as sin spice case incentive 0, 320 volts is what we have given 50 hertz what we want no delay and no damping. So, that is said that is source is set now to the input directory directive you make as value 1 and the file. So, right now I will write in a file e d t 0 1 or s u e d t is a electronic design technology 0 1 dot s u d you can have your own name whichever is convenient and goes. So, it will reflect here and this is a file that will get included when you generate the net list.

So, good time to save the file let us close the circuit this schematic and now you see that in the DC-DC folder we have rectifier dot s c h. So, we have now the schematic ready, but we have to add 2 more files; 1 file we will save as into the DC-DC, I will name it as rectifier dot C i R always keep the same name as that was schematic file name and only the extension you change it to C i R save that and here first line is always a comment. So, start from the second line.

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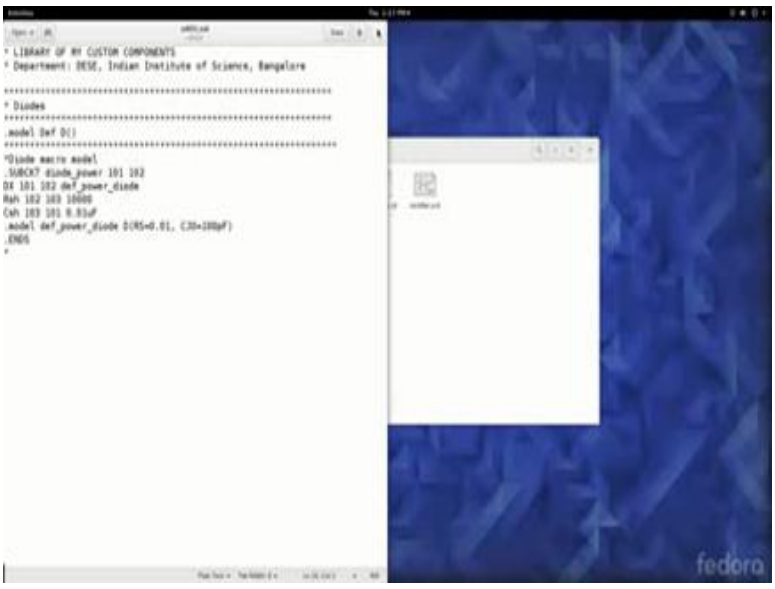

We would like you to, sorry we would like to have a transient analysis performed step time of 50 microsecond up to 100 millisecond using the initial conditions also include the rectifier dot net rectifier for dot net is not yet generated, but we will shortly generate that I will let you know how to do that. So, these 2 control statements for simulation include it in a separate file never include it into the net file. It is better if you do it in this kind of an organized way.

So, that later on for modification complex simulations it would be very easy save that and close this file. So, now, you have rectifier dot C i R also, here 1 more file we will include you remember that we had e d d 0 1 dot sub file which is suppose to contain the models. So, let me save this in the same directory and this time e d d 0 1 dot and save that. So, this we have linked in as an include directive and what should this contain this would a library of my custom components.

So, you could have Indian Institute of Science, Bangalore can have your own thing, what we say that we need to a model, we use the diode there and it was a power diode. Let us have a model for that to the power diode this consisting of 2 parts a model for the diode a default diode and the model sub circuit model for the power diode. So, I will just write this, I think you know how to use spice how to make sub circuits. So, I will not write now teach about how to go about making sub circuits because it is outside the scope of this course. So, I assume that you know spice modelling model I will give a named f now this is a default diode model of a default diode.

Now, let me model the power diode. Now, it is a micro model, it is useful to have this micro model sub circuit model because there are lot of non idealities, which you will not take care in the default ideal diode which you can take care in the sub circuit model and it will the convergence numerical convergence will be much better. So, dot sub circuits I just put that in cap caps just to recognize that over spice case in sensitive. So, let me write down the model first and diode let me take a normal ideal diode, I will say a default power diode can view some descriptive names.

I have put between 102 and 103 and some high value 10000 nodes and 103, 101 0.01 micro dot model default power diode d which has R S series 0.01 junction capacitance of 100 p f dot end s end the sub circuits. So, this is the sub circuits save that. So, I think you recognize this you have the diode between 101 and 102 and you have a resistance shunt

resistance then again in series with a shunt capacitance. So, R shunt and R C shunt or in series and across the diode d x. So, this can be closed and we have the required files this is referred already in the schematic this rectifier dot C i R gives you what is the type of analysis that you want to perform and we need now to generate the net list.

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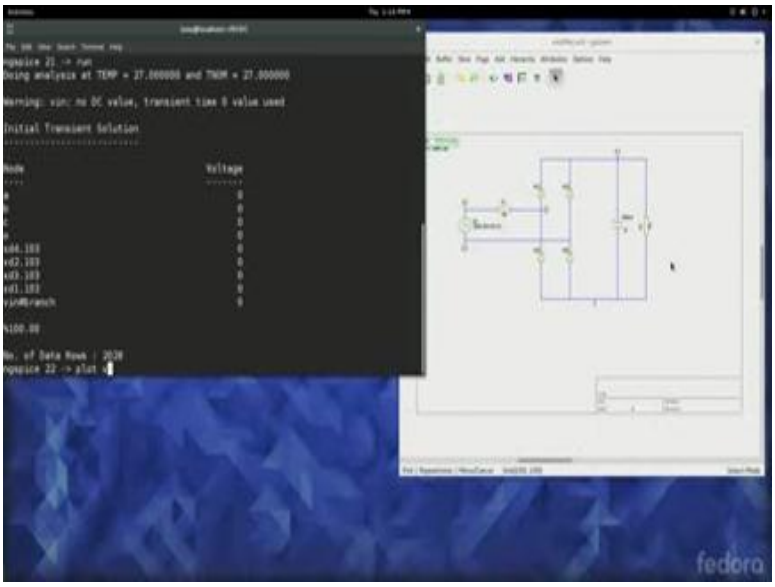

So, generating the net list pretty simple open a terminal and we will go into that folder to the terminal to see that all these files are there. So, let us generate the net list from the schematic like this G net list slash g spice s d b rectifier dot net. We want the output to rectifier dot net from rectifier dot s c h schematic. So, when you run this it will generate the net list. So, if you look there is a rectifier dot net generated, now these 3 files are the ones that will go into n g spice or simulation. So, if you look at the net you see the generated net list the models taken from the e d d sub because of the includitity dot s u d, you see the V in between a and b, we have apply the labels and it has take the label names for the nodes R s R naught the power diodes and the capacitance now we just have to simulate.

So, let us go through the simulation process you are already in the DC-DC folder, you have to call n g spice. So, you say n g spice rectifier dot C i R, you call rectifier dot C i R because within C i R you already have said include rectifier dot net. So, it will appropriately take the net list from here. So, now, you go into the n g spice environment. So, the n g spice environment has the circuits taken into its memory space work space

run type the command run, it will run the circuit and these are the nodes part vectors that you will have.

What we have to do next is plot let us plot V naught or V output you can always open the schematic for reference keep it by your side here, and let us say we want to plot this plot V naught plot V naught you will see the plot comma, you can double click on that and then you see the capacitance charging from the start up and then the labels has be had discussed in theory close that you want to probably see this resource correct here.

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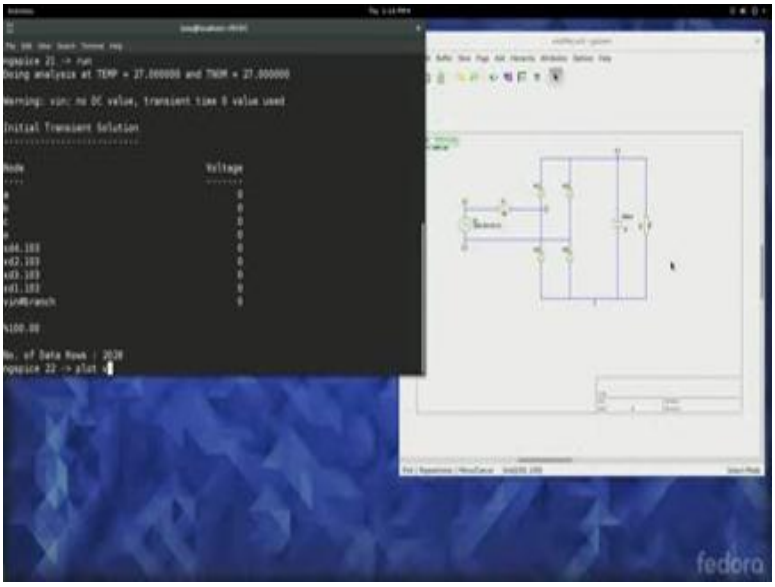

So, let us say plot V naught and also I would like to plot the current of which branch V in branch V in branch here and then you will see that you see the current. Now, the current through the resource is always considered in the opposite direction. Therefore, you see that it is shown minus, but actually the current is in flow in this direction. So, whenever you take the resource branch you can give minus of that by, for example, you can say plot V naught minus i, V in sorry plot V naught 0 minus i in, this was the proper direction of the current you see that initial starter current is higher than the normal steady state current as we had discussed in the last session, after this quit and you are out. So, this completes the one simulation process there are few points and tips that I would like to mention at this point which I will do.

Now, in the case of the simulation after generating the net list using n g spice, one issue with the n g spice plot n g spice rectifier dot and let me once, see that plot I have take

some example V naught though the plot is of a good quality and you can expand it comprehensive and you see that you can also zoom it to the particular part. You will get in expanded you also of that all these are possible the only way you can take this for documentation is by making a screen capture shot of that. So, which can be pretty high a memory when you are making the document and when you make the document, you will get this black background and higher is only for directly taking it as a print out

Therefore, for the purposes of documentation, this n g spice plot is not very comfortable manner you say. So, you can do some documentation with that, that is one issue with and the other issue that we saw is at the time when we where generating this net list. So, when we generated the net list from the schematic, we use the command like this g net list dash g spice dash s d V so on. But every time typing is every time you make a change in the schematic, you have to type this out and then generate the net list dot net file. What you can do is put this into a script file and then keeps calling it in a generic way for any such simulation.

So, combining these 2 problems and making a step such that these 2 problems are solved using octave. We have generate, we have made a script file and that is what you had initially copied and put into the win directory here. So, in the win directory the last section, we had copied 6 files and put it into this folder from resource you see that where free circuits in and then there is.

Now, that q sim is an octave script which takes care of the issue of this net list command generating net list command and also to show you the way forms using octave or MATLAB type of commands and also to put an output in the form of pdf file q sim, what it will do is, it will take the net list do the spice simulation and then put the results of the simulation into the raw file and the raw file is passed as a parameter to the spice as spice a read file dot m file. This is a open source tool function available from n g spice which can downloaded, but I have included it in the resource you can use it.

So, it will read this raw file and then the octaves g n u plot is used for plotting g n u plot is very powerful and you can have different types of output or s b g output from that part. So, that is what we do and this is a small script file written by it is there are there is lot of scope for improvement in this it is just a sample type of script file which proofs to show what you can do and there is lots that you can do, n g sim is actually are also similar to q

sim only that it also generates the rectifier dot C i R file, but many times we forget what you want to write or you know it is the step size ending time when you are a c, but if it is a a c analysis or if it is bias point analysis.

So, many other analysis which are there you may forget, so that where n g sim helps you to do that part. So, I will leave you to go through that and the said if you see that it is comfortable I will just one small example with we are in the DC-DC folder, I will run through same slash h for l. So, let know what to do. So, you have to give it in this form slash h will give you particular screen q sim file name without the extension. So, q sim rectifier without the dot s c just say q sim rectifier it will appropriately take the appropriate files generate the net file and then the n g spice or output file which will be used by octaves g n u plot. It will be read by the spice read file m dot m and then a q plot dot m will be used to plot their outputs.

So, these are some of the syntax which you do not need to use this two syntax because the g n u plot itself will give you an output for whatever for. So, let me just run q sim rectifier now you do not need to a generated the net file. So, what we will do I will just delete this net file to show that was not needed immediately after you do the schematics you have this you should have this and of course, edit 0 1 dot sim q sim rectifier we generate the net list we generate a raw file output which contains all the results of a simulation.

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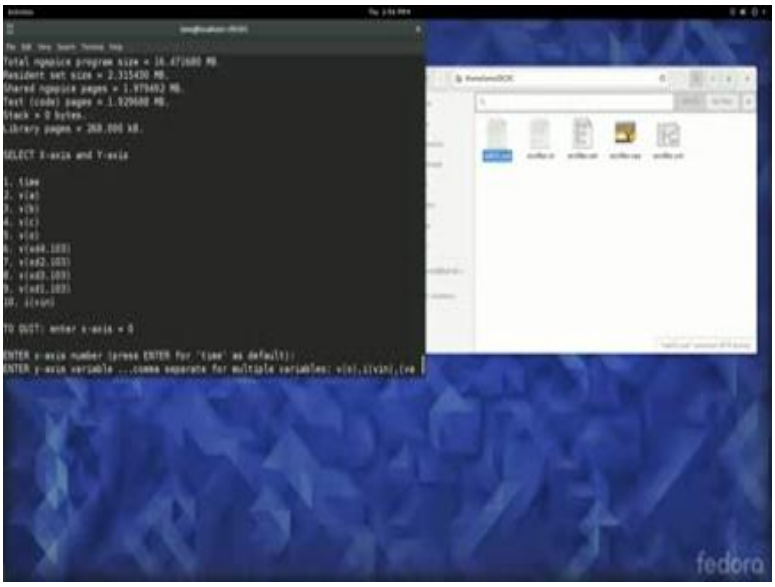

Now, the default time, I can give it as V naught now, here I have to put comma separation I can say current through V in inside that I can also give V a minus V b, all this you trying to see.

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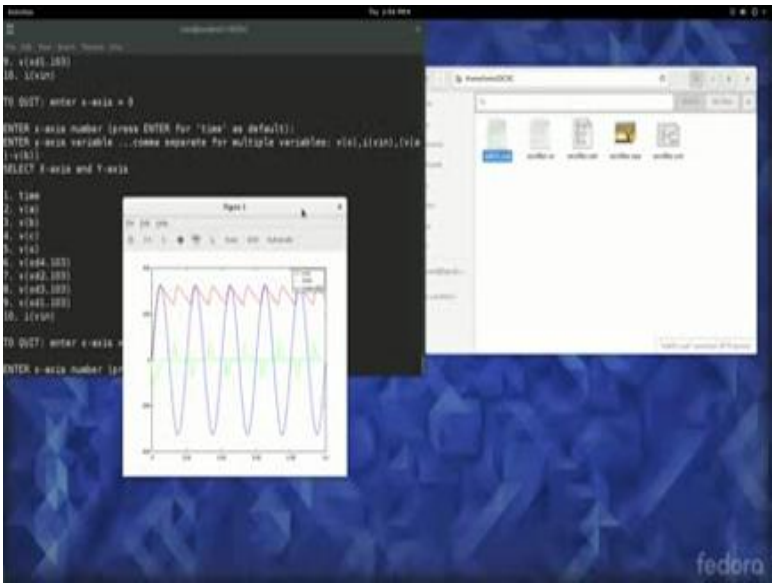

So, you will see it something like this then you output and you see here, you will have, you can save it into a file. Now, let us say I will save as text or s b g saves and then I will come out of. So, here you will the start s b g which can which can be taken into any of the graphic package like that graphic package like in scale for any similar packages, then you can do further editing and then put into the documentation. So, this is how we go about doing a complete simulation starting from schematics an n g spice and the plot outs.