Nanoelectronics: Devices and Materials
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Lecture - 08
Gate oxide scaling and reliability

So, today we will discuss issues in scaling gate oxide.

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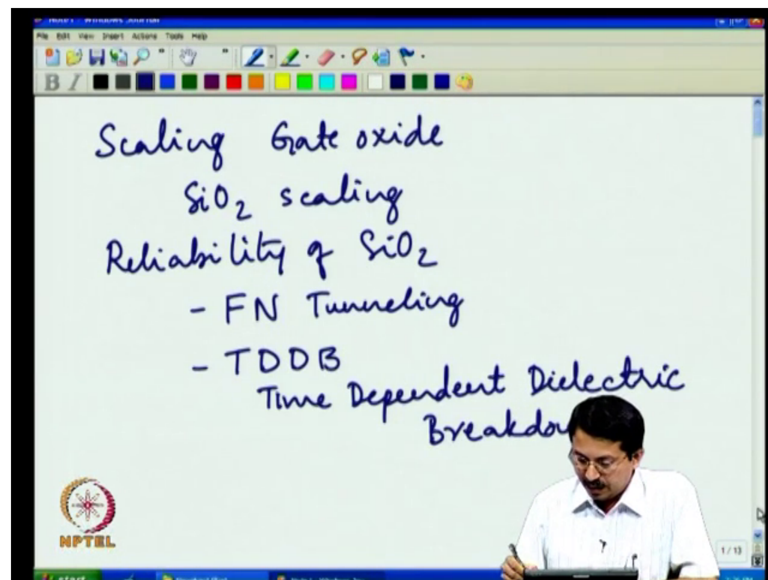

Now first we will address SiO 2 scaling, will see that you know silicon oxide has been fairly good insulator on silicon probably the best insulator semiconducting combination that one can find in the nature, but we see that there are now issues in using silicon oxide in transistor structure, right.

We will take a look at that in we will also talk about the reliability issues of gate oxide, in particular we will look at two concepts one what we call F N tunneling, that is to say if you start flying higher and higher voltage is on silicon oxide that is start increase in the electric field at some point we will start conducting through the silicon oxide and that phenomenon is called F N tunneling, which is essentially in abbreviation called Fowler-Nordheim tunneling we will look at that, and we will also study what is meant by TDDB which stands for Time Dependent Dielectric Breakdown ok.

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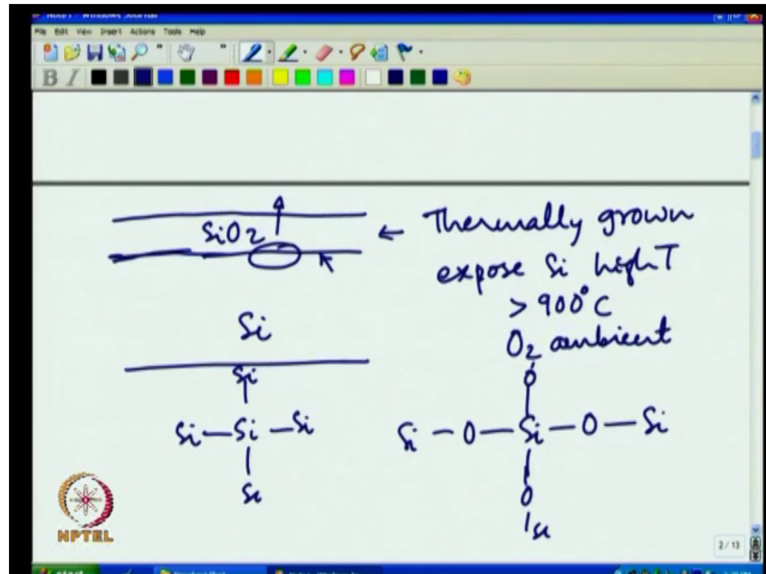

So, then let us get started with you know understanding the silicon oxide and you know what issues are we talking about here and you know when we look at silicon and silicon oxide, this SiO 2 we say is thermally grown what it means essentially is that you know you subject this silicon wafer expose the silicon wafer to high temperature, such as you know greater than let say 900 degree centigrade, and expose it to oxygen ambient and this would result in conversion of silicon into silicon oxide in that is what we call growth of silicon oxide as suppose to depositing something on top of silicon oxide right we actually convert silicon into silicon oxide.

As you could well imagine at this interface there is a transition, what we have in silicon is that we have a nice covalent bond structure, it is a crystalline semiconductor as you know and silicon oxide is an amorphous material and essentially you know what you have a in silicon oxide is essentially silicon bonding to oxygen right.

So, you know you have Si is essentially bonded to oxygen, and this will essentially continue on right. In other words you know this there will be another o and silicon and o and silicon and so on and so forth right. So, that is what you have. In other words an oxygen atom is shared between two silicon atom, right. So, that satisfies the balance and hence a silicon atom is bonded with four half oxygen atoms which is essentially SiO 2 you see, but this is not crystalline you know this is really you know very regular right it would not be looking like that, but the point is that every silicon oxygen atom will bond to an oxygen atom and this is how you have a structure in silicon oxide.

In bulk silicon oxide that is, that is when I start growing oxide on top of silicon as I go deeper and deeper up thickness is increasing, essentially you see a very ideal silicon oxide structure where you know silicon is bonded to oxygen, which is in turn bonded to silicon and you have this mesh. But at this interface we see you have a transition right your transitioning from one material to an another material right and this is what is extremely crucial in the context of field effect transistor and the issue at this interface is that you know you have two important aspect here, one is what is called interface traps and the other one is what is called oxide charges.

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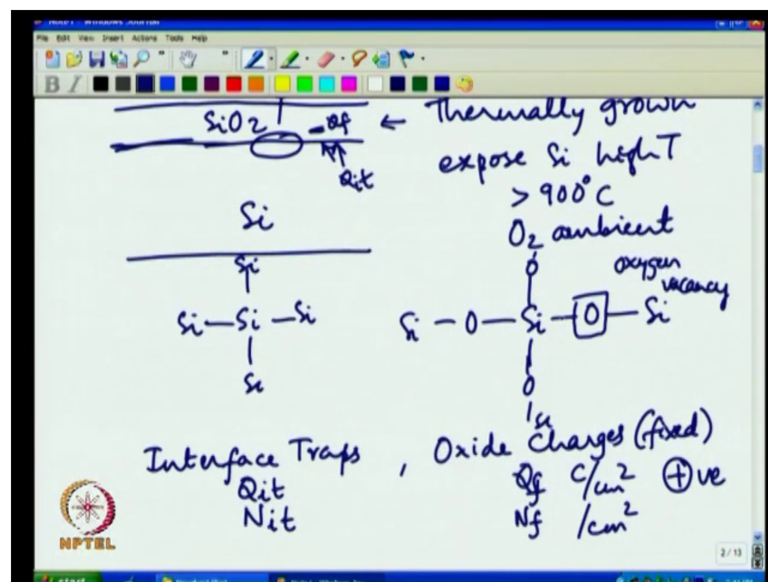

Sometime they are also called fixed oxide charges you know there sort of denoted has Qf to say this some charge which is fixed it does not change and you have what is called interface traps and typically the interface when I say Qf the typical unit that we are talking is you know coolum per centimeter square you know mostly we talk of per unit area, and we also sometimes referred to the number of traps fixed traps in the oxide which is essentially number per centimeter square and when your multiply this with q you get q were that is essentially transition from number to the charge ok.

Now, similarly you have interface traps, interface traps are typically denoted as the interface trap charge is denoted as Qit the traps themselves are denoted as Nit, which is exactly at this interface whereas, these oxide charges are little bit away from the interface right this is where you will find Qf and this is where you will find Qit. Qit is exactly at

the interface and that is the distinction essentially and as you start going away then the oxide is fairly ideal you know there no charges in insulator you know all that is fine and Qit as a postfix charge can be either negative positive right and that depends on whether your populating holes in the channel or electrons in the channel ok.

Whereas Qf is always fixed it does not change and in a silicon oxide system which is charge inside the silicon oxide Qf is always positive and it is conjectured that Qf arises at this interface because when you go little away from interface, because you still do not have an a regular oxide structure, in other words more importantly it is conjectured that you have a mix missing oxygen atom in that region. So, this is also called oxygen vacancy.

Because this is transitioning from silicon to silicon oxide, it is not quiet SiO 2 it is SiOx where that x is less than 2 right in some places you have missing oxygen and it turns out such a defect what it does is that it loses an electron right because now there is no oxygen there is one electron here and one electron here it loses one electron.

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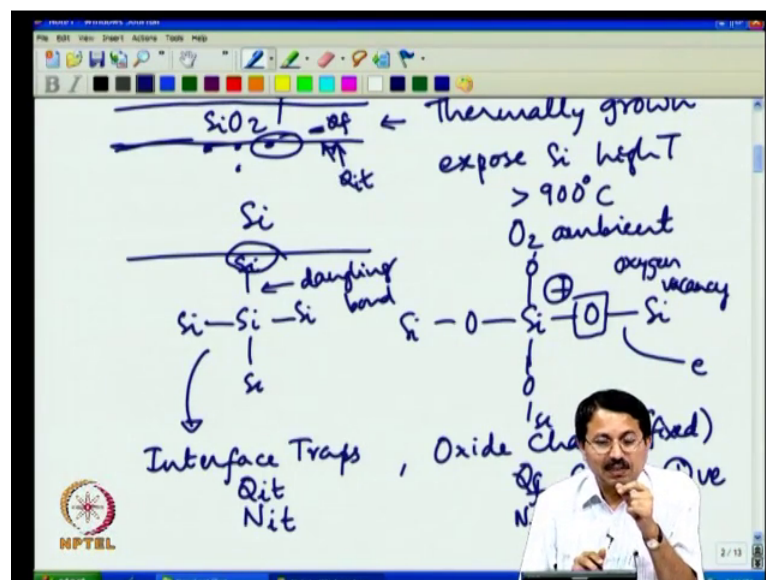

Out and it gets positively charge and this is what is suppose to give rise to all the positive charge that we see in silicon oxide at very close to this interface, and this is fixed because this is little bit away from the interface what you do in the channel has no bearing on changing this because you cannot have this carriers go in and change its state that is why is called fixed.

On the other hand at the interface what happens interface state is presumed because at the interface let say there is the silicon atom sitting here, this silicon atom is bonding to a silicon atom here a silicon atom here as a shown, a silicon atom inside down here, but there is a missing silicon here and in fact, this is what we call dangling bond ok.

If the silicon were to continue up, you will have another silicon atom sitting there and you know it is a perfect covalent bonding mechanism, but here you know you will have lot of these missing silicon atoms exactly at the interface where this silicon is sitting at this interface, but it has failed to find another silicon atom here, because its oxygen ridge it silicon oxide right and hence that gives rise to interface stay this interface traps and oxide charges they can make or break your device. If you have very large amount of interface traps and oxide charge there is no way you can build a field effect transistor, this is the precise reason why even though we had known about field effect transistor theory way back in 1930s a field effect transistor on silicon was only formed in 1960s because it was very difficult to create an oxide which has very low fix charge very low interface texture.

The technology was not mature at that time that is why the first semiconductor transistor was a bipolar junction transistor right it was 1947, but then has the technology progress we came up with lot of techniques to make sure that the oxide which is grown on top of silicon is very high quality oxide, which has as low missing oxygen as possible. So, very low oxide charge and as few dangling bonds as possible hence very few interface steps ok.

Today you know. In fact, in the state of the art Simon’s technology, the numbers that we talk about for Nit is less than 10 power 10 per centimeter square and similarly for Nf number per centimeter square is again less than 10 to the 10 per centimeter square.

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You see this the number does not make much sense unless you put this in a perspective, what is that perspective? Let us recall that the silicon atomic density right it is about 5 into 10 power 22 per centimeter cube, that is per centimeter cube of silicon you takes start counting the atoms you will count so many atoms right that is the atomic density of silicon.

Now, just zeroth order calculation for you if this is my silicon, silicon if it were infinite in all dimensions then everywhere you go you have this atomic density volume density. But when I cut silicon when I make a silicon wafer at the surface, you see this is a silicon surface this is where I am going to grow oxide build devices here we do not talk of volume density, here instead we talk of aerial density correct because now it is a plain because there is nothing else on top of it to talk of volume density ok.

So, just zeroth order way of getting the aerial density from a volume density is essentially take this number 5 into 10 to the 22, two-thirds of it is your aerial density, you can go back and think about how it is two thirds, but you know take it for granted from you know it is a 2 d we are looking at instead of 3 d and hence its two thirds of that number. So, if you do this math what you get is 5 this is now per centimeter square correct ok.

So, this is approximately 10 to the 15 per centimeter square, now you put things in perspective what is it telling you if you had this silicon surface which is a silicon wafer.

At the surface you will have so many silicon atoms and obviously, we will have so many traps because all these have dangling bonds because they are failed to get a silicon on top. So, this is yours surface trap density and you could bring this 5 into 10 to the 15 to 10 power 10 per centimeter square, that is 5 orders of magnitude decrease is possible because we put silicon oxide on top of silicon, that is why even though it is not silicon on top of that surface we say silicon oxide is an excellent passivation layer.

What it means is that, when I grow silicon oxide the silicon oxide silicon chemistry the interface chemistry if you will is so, nice that silicon oxide can saturate so, many dangling bonds and really bring down the volume density I mean the surface trap density by at least 5 orders of magnitude in today's devices. So, that is the kind of you know achievement that we have, but this is just simply not possible if you look at other semiconductors like gallium arsenide. You put an insulator on gallium arsenide you will struggle to get anywhere close to 10 power 10, it could be 10 power 12, 10 power 13 you know depending on what kind of insulator you have same with germanium oxide if you want use germanium for making field effect transistor right and the worst thing about germanium oxide is germanium oxide is water soluble ok.

Let alone be strong in resisting various chemicals that we use during semiconductor processing after growing germanium oxide even if you wash your germanium wafer it just dissolve germanium oxide right the key then for a insulator in FET structure.

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FET insulator that is gate insulator is that it should withstand first of all harsh processing, because after putting oxide as we have already seen in a Simons flow we have so many processes, it should withstand all those process conditions and give very good interface property and this can be done with silicon silicon oxide and it is just impossible to do it with any other you know means and that is why and again you know we take lot of care in really achieving that right.

For example silicon wafer has to be cleaned it has to be clean using various chemicals, we have now a cleaning procedure called RCA cleaning. It is a very well established chemical cleaning procedure, where in silicon wafer is put in acidic and alkaline solutions to get rid of all kinds of contaminants, middle contaminants, organic contaminants and so on and so forth right cleaning is extremely important and then oxidation at high temperature is important.

You know during oxidation you need to really have a very clean ambient, you need to have a very high quality quartz furnace in which you can actually do this oxidation. So, oxidation at high temperature and in clean condition and then of course, you know you have to immediately put the gate electrode and then we have also figured out immediately after oxidation it always helps if you also anneal it in inert ambient like nitrogen, you know if you anneal it at high temperature it improves the quality of the interface and then once you make all your mos capacitor put the gate we also do what is called forming gas anneal.

Forming gas is essentially a mixture of nitrogen plus hydrogen, about 90 percent hydrogen and 10 percent nitrogen and 10 percent hydrogen. The idea here is that you know you all these dangling bonds most of them are passivated by oxygen of silicon oxide, but there still could be some remnant dangling bonds, if you expose it to this kind of an ambient hydrogen is a very light material and very reactive material it can actually come in diffuse in and if there are any dangling bonds which look like this, hydrogen can come and terminate that and that is the idea of you know doing this forming gas anneal, right.

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Way back in 60s or even before that we did not know all this tricks it took a while to really come up with all these process development technology development and today we have very standard recipes. You use this recipes your guaranty to get oxide charges less than 10 power 10 per centimeter square, if you have those kind of charges you will have very little effect on threshold voltage.

Your threshold voltage will not deviate from what ideal theory would predict, otherwise these oxide charges themselves will influence your threshold voltage very drastically. So, this is why we started using silicon oxide, but a lot of things have happened in silicon oxide, you know in terms of our very early MOSFET way back in 1960s which were still large channel MOSFET like 10 micron, 20 micron kind of MOSFET.

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They used to operate at 10 volt and there typical gate oxide thickness of the order of 100 nanometer and today we talk of one volt supply voltage, but oxide thicknesses of the order of one nanometer. You see something interesting here this is exactly what I had said in the context of scaling theory also constant electrics scaling feel theory says you keep electric field constant, but if you see the history electric fields have increased over generations and that is very evident, voltage has decreased by 10 x whereas, thickness of the oxide has decreased by 100 x ok.

If you were to say the electric field is approximately V g by T o x, which is V g here 10 volte you do 10 volt by 100 nanometer, you got an electric field which we typically represent in megavolt per centimeter one megavolt per centimeter, that is the electric field and today if you talk a 1 volt across one nanometer the electric fields are 10 times large 10 megavolt per centimeter. This is precisely the reason for you know concerns today on silicon oxide and of course, the breakdown strength of good quality silicon oxide breakdown strength meaning at this voltage instantaneously it will breakdown you know is of the order of 18 megavolt per centimeter, you know this is still much higher than 10 megavolt per centimeter, but as we will see little later.

There is a phenomenon called time dependent dielectric breakdown under which even if you have lower electric field below the breakdown. So, called breakdown strength you can still have a oxide breakdown over long time, that is why it is called time dependent

breakdown not instantaneously. Whereas, 18 megavolt instantaneously you have a breakdown we will talk about that in a while ok.

So, you see first of all you know in terms of computing electric field across the oxide, this is an approximate expression you see really the electric field should be given by as you can very well understand V g minus V F B, remember V F B is like a built in voltage there is already that built in voltage due to the fact that the gate work function and substrate work function are not necessarily the same that gives rise to this built in potential which we call here V F B minus V silicon, what is V silicon its essentially psi s the band bending because remember I already talked about this simple model that is your Cox, C silicon and you apply V G.

This V G drop across C o x which is called V o x and drops of the silicon which is called v silicon, in a series circuit as you can see total V g is equal to V o x plus v silicon. So, your electric field across the oxide is V ox by T ox correct. So, here V o x in turn is V G minus V silicon by T ox, but because there is this built in potential as I was telling you there is a V F B term also right.

So, this is the exact expression that you should always use whenever you are ask to compute the electric field. So, the key here is that it turns out this electric field is very important. As you start increasing the electric field something interesting starts happening. In fact, you can starts seeing significant current through the oxide, oxide is suppose to be an insulator which is true when you have low electric field, but at high electric field just as you have a lightening and air is a insulator suppose to be, but you can have the current passing through this medium, which is supposedly insulator because you have a very high field generator.

And so is a case with silicon oxide also under low field electric condition it is indeed an insulator, but beyond certain electric field it can start conducting. And let us look at that particular aspect and understand; how does silicon oxide conduct.

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Let us take for instance case, where you know I have a it is true whether it is n type or p type. So, let us take a anyone of these conditions let us take a n type and I have this SiO 2 and I have gate, gate electrode right it could be let say poly silicon n plus or p plus if it is a p channel transistor that you are going to build you will put a p plus silicon or you could also have a metal gate it does not matter some conductor is there on the gate.

Now, let us look at this system and let us consider a case when I apply a positive voltage, I mean just for simplicity let say I just take a metal electrode right here put aluminum electrode it does not matter what electrode is just let us take that condition.

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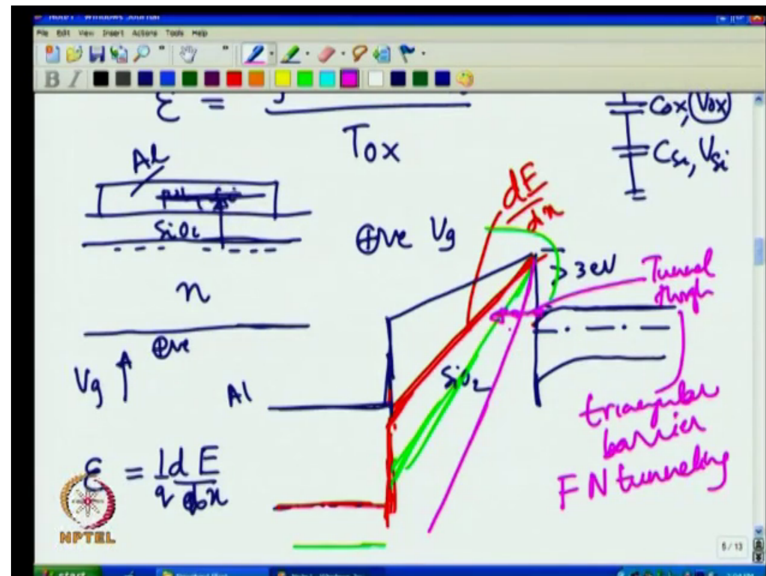

So, what happens when you start applying positive voltage as you can see here positive voltage will start accumulating the more and more electrons here correct that is a accumulation condition.

A negative voltage will dry over electron and it will create a inversion condition. Let us now consider a positive V g condition. So, if you look at the band diagram under this condition what you will see is the following right you have an insulator this is SiO 2 and this is your gate, this is gate that is a aluminum gate and this is your SiO 2 and here this is n type it is accumulating here more electrons at the surface because I have applied positive voltage and accordingly the Fermi level on the gate is lower than the Fermi level on the substrate, that is indicative of that this voltage is positive with respect to this voltage.

So, the band bending will essentially look like this correct there are lot of electrons here in the channel which is here as you can see, but these electrons cannot go in because oxide as you know is an insulator what does it mean? There is a huge barrier here which we have computed earlier which is greater than 3 electron volt that is a large barrier. So, oxide you know this a carriers will not tunnel through and hence you have zero current.

Let us now consider a case when V g starts increasing more and more positive what happens when you start applying more and more positive voltage? Essentially what you have is that you know these two Fermi level starts separately, that is in the difference

between this Fermi level and this Fermi level is the applied voltage and larger voltage will also setup larger electric field which is not difficult to understand and if you recall our discussion may be first or second lecture electric field is always related to gradient in band diagram. Remember this right and more precisely 1 over q dE by dx, right.

So, what does it mean what is a gradient in band diagram? This is a gradient in band diagram correct dE by dx. If I go to larger voltage larger electric field should setup in other words my band bending now will look like this, this is the condition for larger electric field what will happen now correct this is how the band diagram will look, this is the difference between this point and this point which is same as this, this is the difference between this point and this point which is same as this.

What has happened in the processes is I have separated this Fermi level from this Fermi level by a larger voltage and there is a larger gradient this is dE by dx which is your electric field right more electric field, increase it further you will have even more electric field something like this. How is something very interesting happening? If you can see here, earlier these electrons had to surmount this barrier to come into the oxide to conduct current. Now if you continue to increase this further and further let say you have this kind of a situation very large electric field.

Now, you see something interesting here, there is an electron sitting here and its sees an allowed energy state here which is separated by an extremely small distance what is this distance that this distance is governed by electric field; larger the electric field I have more very sever band bending and smaller is this distance and when this distance comes to of the order of nanometers, then you can have large tunneling current electrons need not go over the barrier, electrons can easily tunnel through this so called triangular barrier right.

So, if you increase it further electric field, this distance decreases tunneling distance increases it turns out that tunneling current is an exponential function of a tunneling distance. If you decrease a tunneling distance by a small amount there will be an exponential increase in tunneling current right then you will see that your tunneling current starts going up exponentially with applied electric field or applied voltage, and this is exactly what is called FN tunneling.

For example when will this tunneling distance be one nanometer just to tell you this which is not very hard to understand right you know this let say this barrier is 3 volt, 3 electron volt then you should have an electric field which is three volt per nanometer. If you have a electric field which is three volt per nanometer you will reach this point which is in line with this point over a distance of one nanometer.

So, those are the kinds of field that we are talking about, that is when the tunneling will start right. Typically it turns out you will start tunneling even before you reach 1 nanometer, 4 nanometer 5 nanometer you know you easily will start seeing significant tunneling current and we typically say that.

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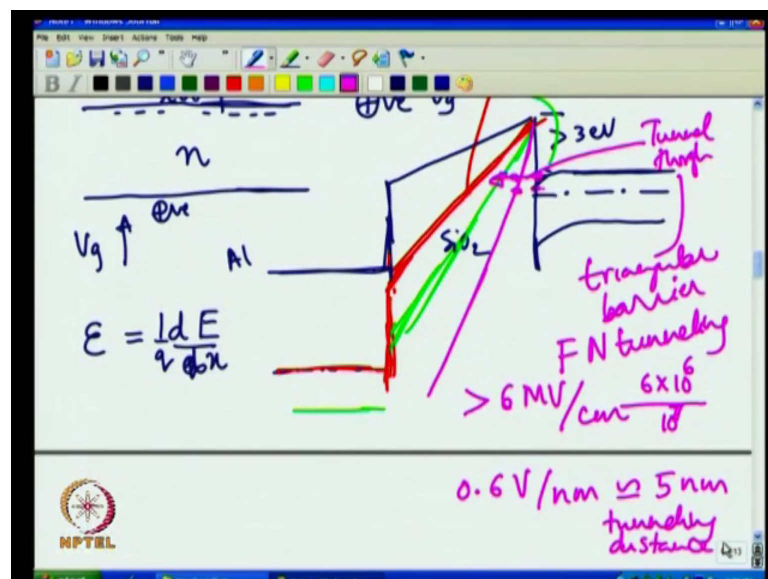

If the electric fields are more than you know of the order of 5 to 6 megavolt per centimeter, then you will certainly start seeing you know significant tunneling current.

So, what is this electric field? This is 6 into 10 to the 6 mega right m here and centimeter which is how many nanometer right 10 to the 7 right 10 to the 9 nanometer is a meter and 10 to the 7 is essentially you know this. So in fact, you can see here that right its essentially 6 by 10 which is 0.6 volt per nanometer, right.

So, even when you reach 0.6 volt per nanometer what is 0.6 volt per nanometer? For 3 volt barrier to be aligned here you have a tunneling distance of 5 nanometer you see 0.6

times 5. So, typically when your tunneling distance is of the order of 5 nanometer, you will start seeing tunneling current, ok.

So, this 6 megavolt per centimeter really corresponds to 0.6 volt per nanometer which approximately corresponds to a tunneling distance of 5 nanometer tunneling distance approximately and this is what you see.

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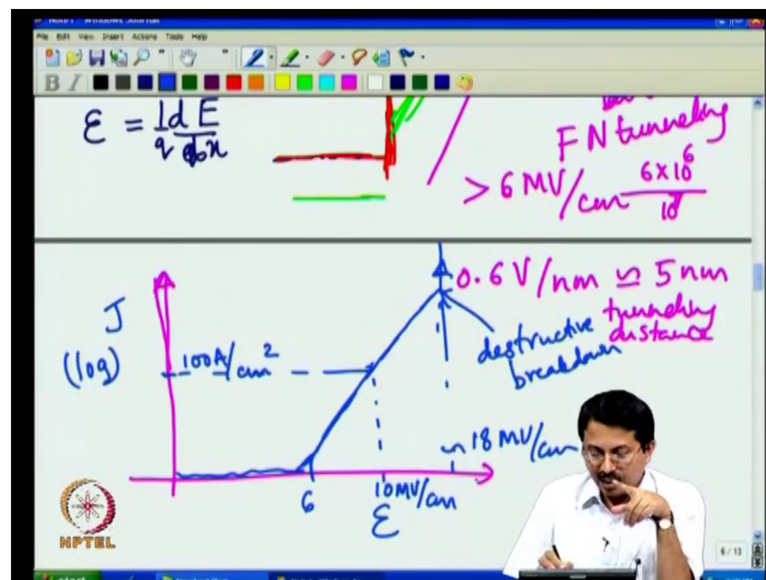

If you were to look at current density J as a function of electric field E, initially your current is very very very small, but once you start reaching the fields that ours talking about 6 megavolt kind of field.

You know you see that currents starts increasing this being a log scale you see this is a linear line meaning it is an exponential increase with respect to increasing electric field. And in fact, when you reach 10 megavolt per centimeter, this is E in 10 megavolt per centimeter your typical tunneling current density in silicon oxide silicon system are of the order of 100 ampere per centimeter square, that is the kind of current density that we will see, ok.

The 100 ampere per centimeter square number may look huge, but you need to put things in perspective, let say if you have a you know one micron square area for your transistor or a gate area is one micron square, then you can see that what current you will have right. Now you 100 ampere per centimeter square and you are talking of one micron

square. So, this is 100 into 10 to the minus 8 correct and you know that is the kind of current that you will see, which is about a micro ampere current. But that micro ampere current is now significant in the context of the transistors that we are talking about and if you continue this further, it continues to increase and if this is really very large you know what is that large of the order of 18 megavolt per centimeter. Again this number may vary depending on how good is your oxide have you done an excellent quality oxide or its little bit inferior it may be little better than 18 or little less than 18, but that is a approximate range ok.

At this point you see a huge current you know as soon as I go to that voltage I will instantaneously have a very large current it will result in thermal run away and you are metal can melt and it will cause permanent short in the device. So, that will be a destructive breakdown, but even before this destructive breakdown this is really destructive. Even before that you can still have reasonable current flowing through the oxide it is no longer an insulator in this electric field region that is the main message that I wanted to you know convey to you right oxide can conduct, if you have sufficiently large electric field and that is because of this tunneling process. And in fact, it is called Fowler-Nordheim tunneling, because there were the first to really you know sort of give the theory for such tunneling and in fact, you can.

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Reasonably you quake led this tunneling current reasonably well using this expression which is called Fowler-Nordheim expression, this is E is electric field here and you have this exponential of a various quantity, let me just right it down for you this is M o x which is a effective mass of electrons in oxide and where your A is essentially an fn constant which is again given by this expression 8 pi h phi b, here E is this electric field that we are talking about.

You see this exponential dependents on electric field and this is negative because which essentially means that has you increase E the current here increases this is denominator you see and E is electric field which is obvious, q is charge and h is Planck's constant and what else do we have m o x is what is called effective electron mass in oxide, which is lower than its free mass free electron mass and phi b is important quantity and that is called barrier height this phi b is barrier height and what is that barrier height? At that barrier height is essentially this that we are talking about this is phi b.

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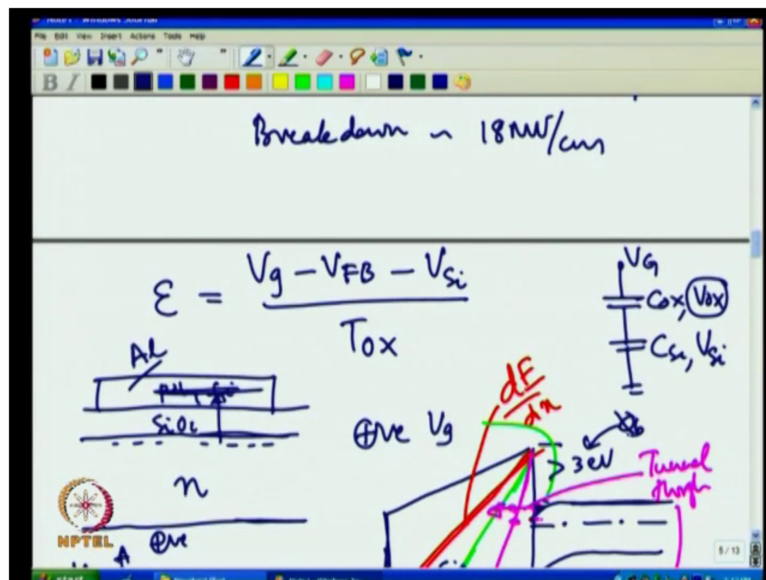

Larger the barrier lower will be the current that is not again hard to understand because there is a huge barrier for the carriers to conduct ok.

Smaller the barrier higher is the tunneling current again it is an exponential function of barrier height similarly given a barrier height for example, silicon silicon oxide system barrier height is fixed, then you start changing electric field again it is an exponential

function of electric field. So, using this expression you can very well compute the tunneling current density.

Now, let us look at you know the other important the important point again I want to stress is that the oxide current through the oxide is essentially dependent on the field across the oxide and the barrier height, whether injection is from here to here or here to here if the same barrier height exist and same electric field is there the currents will be similar. In other words they are independent of from which side the current is coming into the oxide, but what is crucial is the barrier height and electric field. In this co context it may be useful to sort of mention here the difference between n channel and p channel transistors.

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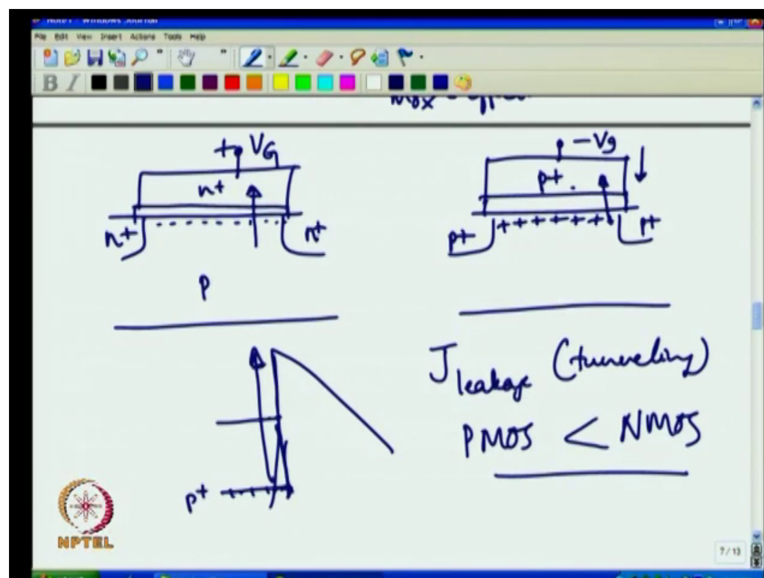

Remember n channel transistors have p type substrate and n plus poly silicon and they are mostly operated with positive gate voltage correct, that is we are interested in this kind of a tunneling, we have a positive voltage when you invert this transistor with the positive voltage there are lot of electrons. And these electrons can actually tunnel through. So, the barrier height here for electrons tunneling is what is important.

Now, if you look at a p channel transistor, you see this is p plus poly silicon and it is operated with negative gate voltage. When you apply negative gate voltage also create lot of holes here right I also create lot of electrons here and these electrons tunnel. Now you can have two possibilities right one is tunneling of electrons from p side if you are

talking of only electrons tunneling right, because this is negative electrons have to go in this direction, but turns out this may not be very significant for two reasons.

First of all it is p plus semiconductor. So, availability of electrons itself may be less, but more importantly the barrier height, now when we talk of barrier height you know it is the electrons sitting here these have to tunnel into the oxide, this is a huge barrier height. Now, because not electron sitting in the conduction band we are talking of electron sitting in the p plus layer right. So, that is why this electron current is less and there can be hole current, but again the barrier for whole injection is larger if you recall our discussion when we sketch the band diagram of oxide silicon, I told you that the band offset for electrons is of the order three electron volt whereas, per holes its of the order of 4 electrons volt at the bottom, right.

So, as an effect the leakage tunneling leakage current in p mass could be less than tunneling leakage current in n mass. So, that is J leakage due to tunneling remember we are not talking of sub threshold leakage, we are talking tunneling leakage E is essentially for p mass typically is less than n mass that is because of these considerations. So, at least this is one region where you p mass would help you a little bit, it would not conduct so, much leakage current through the gate oxide ok.

Now, let us talk about this issue of time dependent dielectric breakdown.

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We said that if your electric field is greater than 18 megavolt per centimeter there is instantaneous breakdown, but let say that E is less than 18 megavolt, we do know that even when E is less than 18 megavolt per centimeter there can be conduction. As soon as I go more than 5 6 megavolt per centimeter, we said that there is a Fowler-Nordheim tunneling current because tunneling distance has come down to 5 nanometer of that order correct. So, in other words if you look at the band diagram of the oxide, what you will see is you know.

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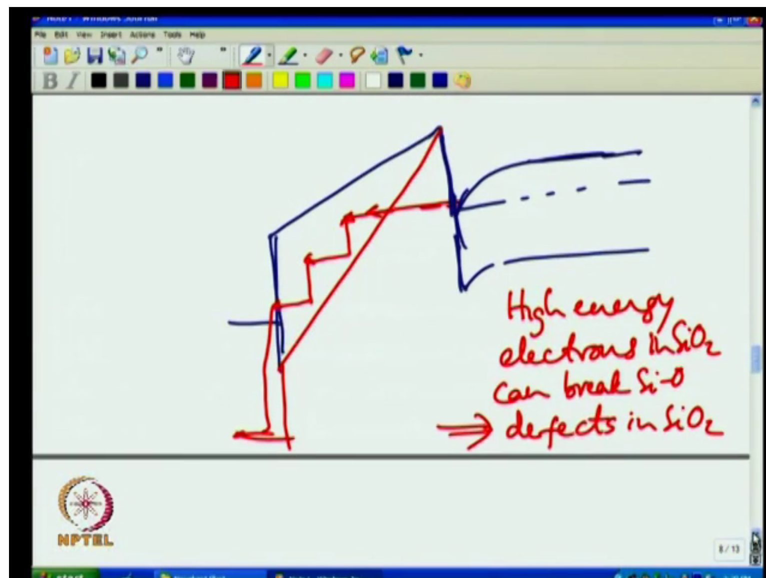

Again let me just consider the case where you have n type on the silicon and I have applied you know positive voltage on the gate and as I already told you this band bending will essentially you know increase and will result something like this correct eventually this right ok.

Now, it is less than 18 megavolt, but still there is tunneling because this distance is less than 5 nanometer of the order of 5 nanometer now. So, what happens really in now is that these electrons come into the oxide conduction band. There is large electric field they get accelerated, because of the electric field you know it means that their energy increases, but they can essentially colloid with silicon atoms and they can lose the energy and they can go through a series of this processes. And eventually they collected at the anode from cathode they are coming and collected at the anode and that constitutes a current for E,

but what can happen is that these electrons which have high energy when they impact with silicon oxygen SiO 2 silicon oxygen bond they can actually break the bonds ok.

In other words these high energy electrons in SiO 2, can break SiO bond. SiO bond has certain strength if the electron energy is more than that strength and it colloids with that it can break SiO bond and in other words it will start creating defect in SiO 2 correct. SiO 2 which was ideal now start saying lot of defects. And in fact, we also call this overtime these defect starts increasing and this is also referred to as in literature.

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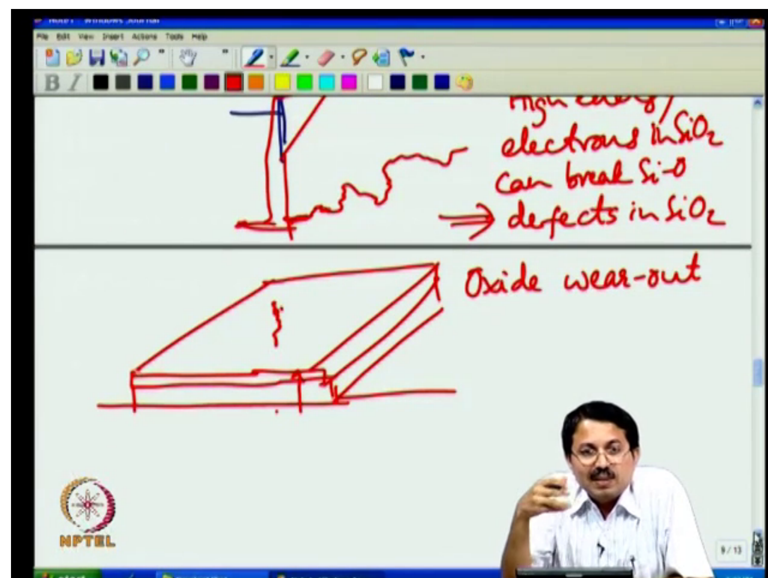

Oxide wear out you know just like any mechanical device wears out over long usage.

You know this oxide over long usage is wearing out you know slowly the bonds are breaking in the oxide and you know what happens, because of that is that you know once you start breaking the bonds these a defect site, you know they do not necessarily are like insulating materials you can model that as you know the some defect here. And you know this defect is propagating something like this depending on how the bonds are getting broken and this is what is called a percolation path ok.

Eventually you know what happens is that this along this path there is more and more electric field there is some kind of a positive feedback more carriers can go in, and eventually you can reach a breakdown condition you will have a path a defective path from anode to cathode which is not really an insulating path. In other words if you look

at the top few of the silicon oxide this is the silicon oxide that I have and this is the silicon material I have right, this is the gate silicon oxide and silicon right.

So, there is this electrons going and you know they are going of course, in all direction, but anywhere here a weak spots starts wearing out. And eventually in that spot you know there could be defective path from the gate to the substrate or anode to the cathode and hence you have a destructive breakdown under that condition. So, what it means is that although I had very low electric field which is much lower than the breakdown strength, over the time because of the oxide wear out oxide will breakdown.

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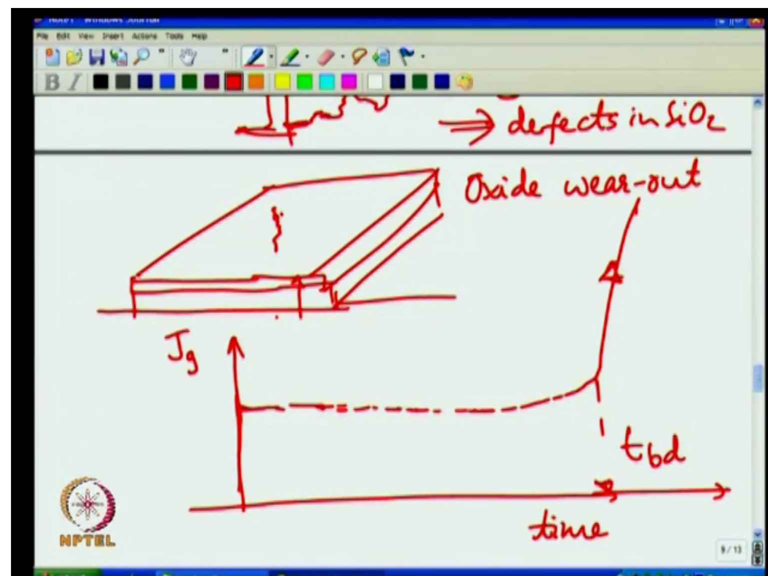

In other words if you actually look at as a function of time, current gate current or oxide current you will essentially have some current which is small current as detec dictated by Fowler-Nordheim tunneling theory given an electric field there is a current you know this current continues like this, but over sometime you know you will see an effect something like this you can see a huge current flowing in and this is what we call time to breakdown TBD. So, even though I am operating the transistor at a normal operating condition, which is much lower than 18 megavolt per centimeter one volt across 1 nanometer is 10 megavolt per centimeter approximately because you need to do V g minus V F B minus v silicon by T o x, but it will be very close to 10 megavolt per centimeter ok.

So, even at 10 megavolt per centimeter which is the normal operating condition of the transistors today in today's chips with silicon oxide as a gate dielectric, overtime it will breakdown. If you apply larger electric field this will breakdown even earlier if you have a lower electric field this will breakdown much later. So, this is why it is important to characterize the so called oxide reliability. Oxide is insulator it is a good material, but over time it breaks down does it breakdown in 1 year 10 year you cannot of course, wait for 10 years to figure out how when does it breakdown right. Because even before you shift the products in the market you need to make an assessment of the breakdown of the oxide breakdown time of the oxide in other words it is called a reliability prediction uh.

So, the where the reliability prediction is done in all these devices is through what is called accelerated testing.

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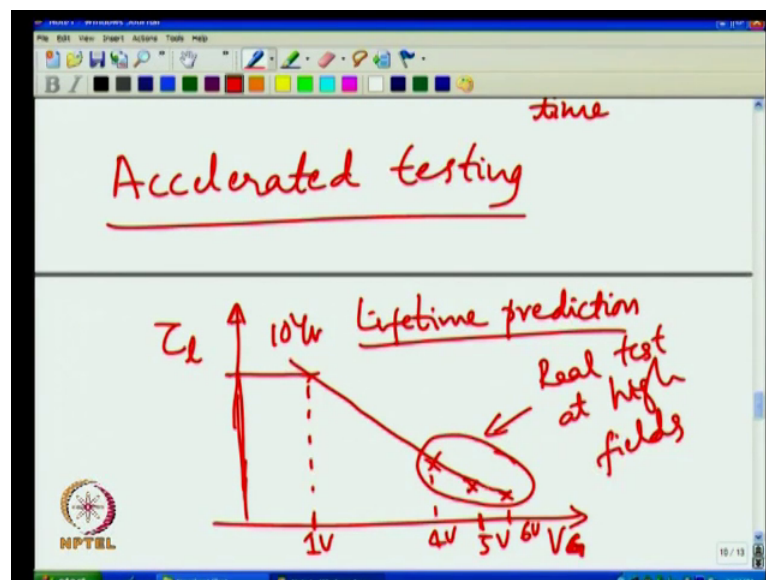

So, what it is means is the following right let say I am looking at v across the oxide or Vg what that you apply on the gate as a function of lifetime let me call it as tau l which is the lifetime of the device, and this is really going to operate at let say one volt that is the condition for let say 65 nanometer or 45 nanometer simons technology, but for this one volt it may survive for 10 years, but I cannot wait for 10 years before I shift the product in the market. So, what I do in the F A B once a make my device, is intentionally apply large electric field much larger electric field than the device will ever see in the field ok.

So, instead of one volt I may apply 5 volt let say; when you do this, this what I mean by accelerated testing the breakdown times come down very drastically which is manageable you can do the measurement in the lab you do not wait for 10 years for that. So, you figure out what is the breakdown time may be do it for a few different voltages do it for 6 volt, 5 volt and 4 volt and so on and so forth and based on that you do what is call an extrapolation for used condition.

In other words what you have really done this is the real test at high fields. In other words I accelerate the deterioration and get the trend of its lifetime dependence as a function of different voltages which are very high and I assume that the same phenomenon is valid even at low voltage the wear out phenomenon and try to do an extrapolation and say look if you are going to use this device in the field. Now, this device is going to survive for 10 years or whatever you know you get some lifetime and this is what is call lifetime prediction.

So, I do the test for a month also, because you know I may engineer this voltage such that you know the whole data should come to me in a month this lifetime may be month this may be two weeks a week whatever it is right. So, based on that I can now do this extrapolation and this is how this lifetime prediction engineering is done in foundries.

This is an important exercise and the point again to summarize is that even though oxide has an 18 megavolt instantaneous breakdown field it breaks down instantaneously, at lower breakdown field which is an operating voltage condition it will still breakdown over a long time. And what is that time is to be estimated using this time dependent dielectric breakdown measurement. And there are there are various techniques that are used to enhance the reliability of a silicon oxide you know.

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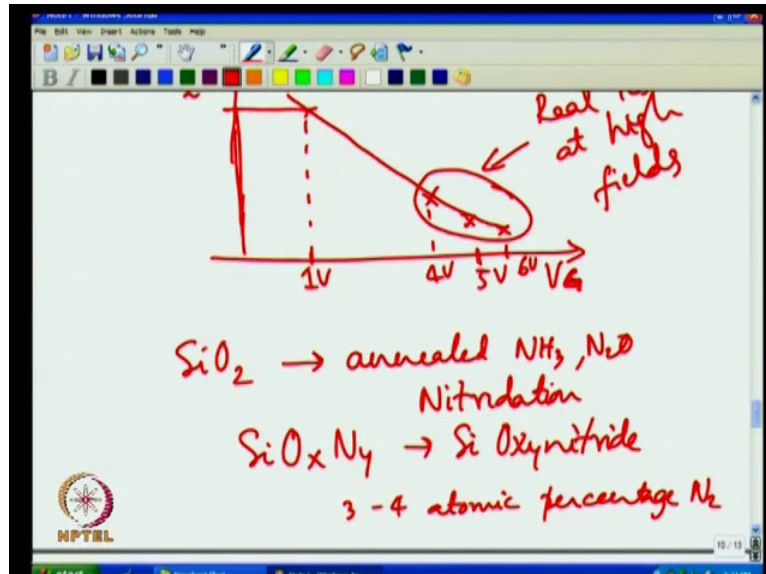

You know silicon oxide reliability is typically very thin silicon oxides also are annealed in either ammonia or nitrous oxide, this is actually called nitridation its not quiet silicon nitride, but you first create a silicon oxide may tricks if you anneal it in nitrogen, nitrogen is very inert you cannot really react nitrogen with silicon, but ammonia or N2O if you expose the silicon oxide after a oxidation process, then some of the silicon SiO bonds can be replace with SIN bonds that is why it is called nitridation and it turns out silicon nitro silicon nitrogen bonds are much stronger than silicon oxygen bonds. And hence they can sustain larger electric field.

And the other there is also other model that is used to explain the enhancement of the breakdown field and that is essentially when you grow silicon oxide on silicon silicon oxide always have compressive stress. When you put some convert some of this silicon oxide into some sin bonds, it is called silicon oxynitride this is called nitridation this is actually call SiO x n y where x is very close to two, but not quiet 2 y is little more than 0 that is why it is called SiO x N y or it is called silicon oxynitride it turns out nitride typically as tensile strength tensile stress, ok.

So, when you puts convert little bit of oxygen oxide into nitride you reduce the compressive stress right that is another theory. So, you minimize the stress if the bonds are under stress it is easier to break the bonds, if you reduce that stress its more difficult to break those bonds right and that is another theory which is also proposed to explain the fact that when you do this silicon oxynitride, you have enhance reliability. The point

that I am again trying to make is that the silicon oxide has been used may be up to 65 nanometer kind of silicon technology.

After that we have made a migration to high k gate dielectric, which we will discuss in the next class next lecture, and when we were doing silicon oxide of the order of one nanometer it was really silicon oxynitride. Because it is so thin, reliability is a concern we were actually converting part of that oxygen silicon bonds into nitride nitrogen silicon bonds very very small nitrogen by the way.

The nitrogen that we were introducing where may be 3 to 4 atomic percentage specifically at the interfaces two interfaces, because that is the key because the damage starts occurring at the interface right you really need to strengthen the interface. So, thereby you know we have been using this silicon oxynitride until very recently before we made a transition to high k gate dielectric.

So, let me summarize then silicon oxide first of all is an excellent material because it passivates the traps at this silicon silicon oxide interface which we have already seen and that is why silicon silicon oxide system is an excellent system to make fet's unlike germanium or gallium arsenide system, that is why silicon as simply displaced all other semiconductors in the industry. More than 90 percent of your electronics which is available in the commercial domain is silicon electronics that is because of fet's and that is because of silicon oxide.

Silicon oxide has really served as for you know almost 5 decades from 60s till you know very recently, that is a very large service that it has provided, but over the time because we scale this from 100 nanometer to 1 nanometer we started having this reliability problems first of all, also Fowler-Nordheim tunneling which induce the you know this breakdown time dependent breakdown and so on and so forth. And next lecture we will also see there is another phenomenon called direct tunneling, that is even more serious and because of that now we are talking of replacing silicon oxide with high k gate dielectrics, right.

So, with that let us conclude the lecture today. And in the next lecture we will start discussing about direct tunneling in silicon oxide, ultrathin silicon oxide, and why do we need high k gate dielectrics to replace silicon oxide.