Nanoelectronics: Devices and Materials
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Lecture - 06
Channel and Source/Drain Engineering

Today, we will discuss about designing a transistor in the nanometer regime. There are two important considerations that we will look at today; one we call as channel engineering.

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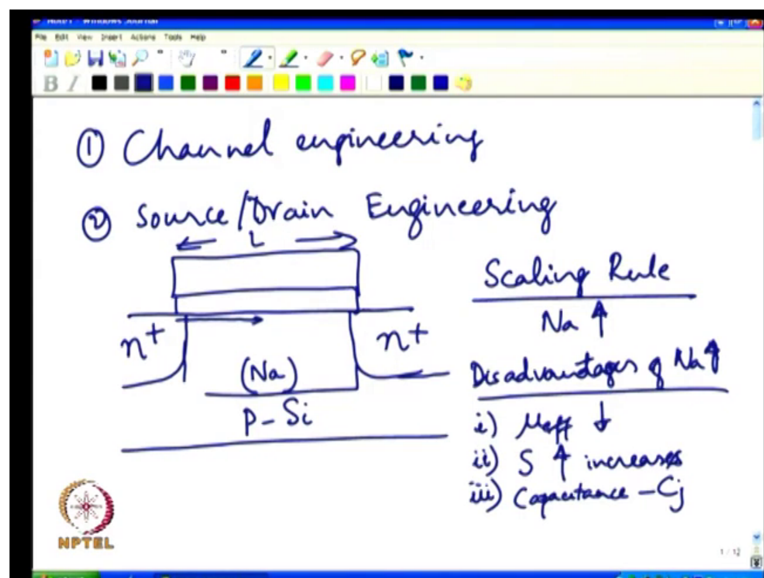

And the other one is source drain engineering. Based on our discussion so far, it has become clear that if we want to design a very small geo metric transistor. This particular case we are looking at n channel transistor.

As the scaling guideline suggest, when we start decreasing the channel length. This is our channel length. The question is what do we want to do inside this silicon, how do we engineer this silicon. As you recall the simple scaling guideline had suggested that, the substrate doping concentration which is expected impurities in a P type silicon, that should increase from generation to generation. The k is a scaling factor, which is a greater than unity, and every generation you know the doping concentration continues to increase.

So, we do know that as per the scaling guidelines, Na should increase this is very obvious, but the question is, should it increase everywhere in this region. This is my region of interest that we will look at today, and we note that while increasing any Na is very important from the point of view of short channel effect, because higher the Na lower is the coupling between drain to source, and your Vt roll off is not as much as otherwise it would be.

And in addition we also discovered that, you know if you have a higher doping concentration your drain induced barrier lowering, is also not as much, because your drain electric field is completely screened, by higher doping concentration, but are there any down sides or disadvantages of increasing doping concentration, of increase in doping concentration.

We have mentioned in earlier lecture there are certainly a few disadvantages. For one thing your mobility, field effect mobility suffers greatly, because higher doping concentration in this area especially where the current will flow very close to the interface from source electrode to the drain electrode. There is more scattering because of higher impurity and that is not good, your current will eventually suffer; that is one important consideration.

There are other important considerations as well, as you also know the sub threshold slope depends on this non ideality factor, which is one plus Cd over Cox. We want to minimize this one plus Cd over Cox. In other words we want to minimize Cd; however, increasing Na is not good, because increasing Na increases Cd, and your sub threshold slope also becomes worse. The sub threshold slope increases, you know instead of coming close to 60 millivolt per decade, it will go far away from 60 millivolt per decade, because of increased doping concentration. This is also not good.

So, what are the other considerations? You see increasing doping concentration is also not good for your capacitance; that is more importantly junction capacitance, because you have the source drain junctions, and these junctions eventually determine these junctions have certain area, and that determines your total area of the capacitance, and the depletion width will be determined by Na.

So, which is also not good, because higher the capacitance, as you know the capacitance will eventually determine your speed of the circuit, and also the power dissipation of the circuit, because as you recall from our earlier discussion.

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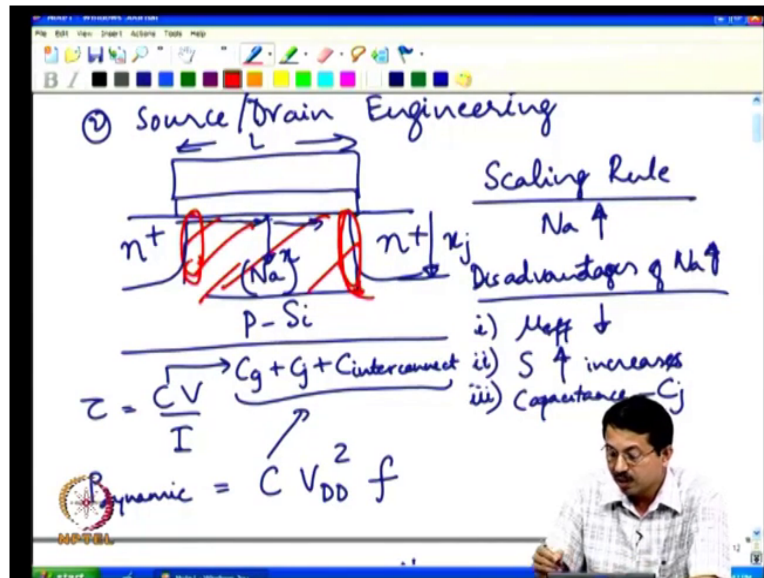

Your delay is CV over I and this C in turn includes the so called gate capacitance, junction capacitance, and interconnect capacitance. We are not looking at interconnects now.

It is interconnect between one transistor to the other transistor, we are not worried about that, but this C junction will also increase because of increased doping concentration. And similarly as I mentioned your power dissipation, in another words dynamic power dissipation, is essentially given by C V DD square trans f, where f is the frequency of switching; that is why we call it dynamic power, when you are switching what is the power consumption. V DD is the supply voltage for your circuit, and C again is exactly the same capacitance, and you see higher junction capacitance is not good.

So, these are the disadvantages, but we have to increase doping concentration in order to shrink the transistor. Now the question is, rather than increasing the doping concentration uniformly in this entire region, can we do it little bit intelligently, can we engineer this doping concentration, and the answer is yes, and that is in fact, what we call channel engineering. We would like to engineer this entire region in particular.

Let us you know consider this region going from source to the drain very close to the channel, and somewhere in the middle of the channel going deep down inside. And I will just take the axis convention here, typically I, most of the text books use this you know, going downwards I will call it x axis, positive x axis, and you know going along the channel especially laterally in this direction I will call that as a y axis ok.

So, along the y axis I will go from source which is y is equal to 0, I will have that as my reference and go to l which is the channel length at the drain side. And along this depth, I will again start from the middle point here which is x equal to 0, and x is increasing as I go down further. As you already know this dimension is what we call xj, you see and that is your junction depth and that is the value of x coordinate at which the junction is formed.

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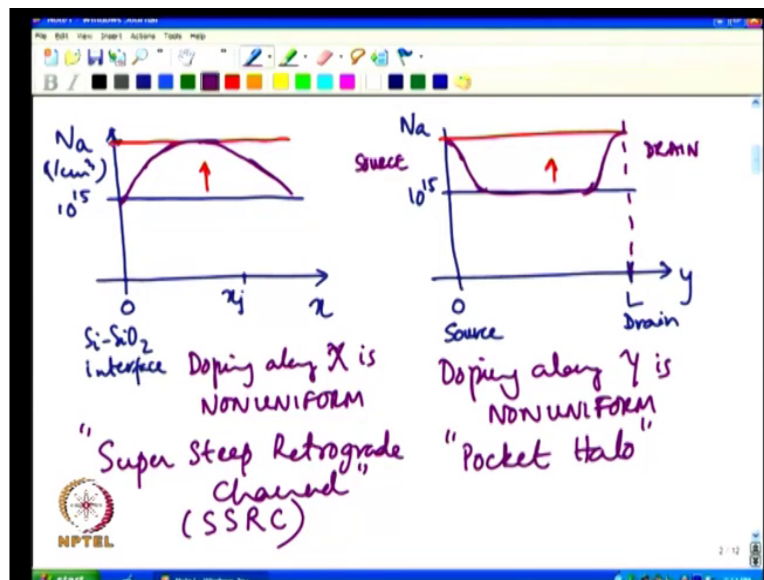

So, with this convention let us look at this, you know doping concentration along x axis and doping concentration along y axis. Now as you know y is going from 0 to L. This is your source side, and this is your drain side. x starts at 0 which is your Si SiO 2 interface; that is where I call x equal to 0, and I go deeper down, somewhere out here you will also have your junction depth xj, and in this direction I am interested to find out what is my doping concentration ok.

Now, classically what you think, that the doping concentration is constant in the substrate, and that is how you derive threshold voltage and so on and so forth. In other

words if you look at the doping concentration along x direction it is flat, and along y direction it is flat, same value. If it is 10 to the 15 per centimeter cube, this is where I am plotting my Na, 10 to the 15. This is the very classical case you know, this unit is per centimeter cube.

Now, as we already said, you know let us say this is what we had in a very old generation 5 micron length transistor. As the scaling theory suggested, when we started scaling the transistor this should start going up; that is what the scaling theory suggest if you were to start increasing it arbitrarily everywhere with the uniform doping, you know it may look like this, and it may look like this from 10 to the 15, you may start going 10 to the 16 17 18 19, everywhere in the area of the transistor that we have in this entire region ok.

If you were to do that you know that will be detrimental for your transistor and we do not do that. We recognize the fact. First of all in terms of let us say going from source to the drain. All that we need to do is to prevent this drain electric field penetrating inside the channel. So, where do we want to arrest that field? We need to arrest that field at this region. Once you make sure that the field is sort of constrained there, it is not going beyond that.

Then you do not necessarily have to worry about this entire region. All that charge sharing for short channel Vt roll off, drain induced barrier lowering. All that is determined by what happens here at the edge, how far are you letting the electric field penetrate inside you see. In other words message is that it is sufficient, if I increase the doping concentration selectively at this region, and not let the doping concentration here go up. The doping concentration here is increase selectively to an extent, that the drain electric field is suppressed in this region of high doping concentration.

So, that is what is called pocket halos. In other words what we are saying is that, we introduced very highly doped pockets, these are what are called pockets, and they sort of you know our going around the source and drain junction, and hence the name halo. It is sort of looks like a halo around the junction. So, there will be one pocket here, there will be another pocket here.

So, in other words if we were to look at, that doping engineering that we want to do going from source which is y is equal to 0 to the drain. I do not want a flat doping profile. Instead what I would like to do is a very large doping profile here concentration,

and let it drop down to as low as you can afford to have. And again as I start approaching to other end, increase it further you see.

So, the doping, the message is that the doping along y, and I have achieved my goal. What was my goal? My goal was, there is this drain electrode here, and of course, drain and source can be interchanged, this is a symmetric transistor. If this could be a source, or this could be drain, and this could be source, and I have increased the doping concentration here ensuring that, you know my electric field does not penetrate, and in this region I have minimize the doping concentration. And hence I will be able to reduce all these detrimental effects, mobility will not be degraded as much. So, threshold slope will not be degraded as much and So on and so forth.

Same argument holds good, going along the x direction as well. And what we do here is that, we do not do this we sort of do a complement of this. In other words here the requirement is, as I start going near the channel; that is where my current is flowing you see; that is where I want to minimize the carriers scattering. In a MOSFET fet device, the current is a surface channel current.

So, what I do is, I minimize my doping concentration here, and I will then let the doping concentration go up as I start going down, and then let it reach some peak value, and again as I start approaching the junctions. I want to minimize the junction capacitance, so, again I start rolling off this. So, again in the vertical direction I have a non uniform doping profile which is engineered; such that add the interface very low doping concentration, as low as you can afford to have.

So, that when the carriers are going along the channel at the interface very little scattering, because doping concentration is low, but as you start going in you provide excess doping concentration to make sure that there is no punch through from the drain into the channel. So, again as you start reaching the junctions, you start minimizing the doping concentration.

And you know in other words, again doping along x is also non uniform, and this is what we call pocket halos, and this we call super steep retrograde channel. Sometimes in literature you see this being abbreviated as SSRC, which stands for super steep retrograde channel. What it means is that, first of all retrograde meaning that the peak is

not at the surface, which is what you would have expected the peak would be at the surface, but the peak is away from the surface.

And hence it is a retrograde profile and super steep; meaning that you would like to make it as steep as possible you see. So, that when you reach the surface, the doping concentration is minimized. So, by doing this, all the transistors which are fabricated today, not just today you know, this has been there for last several generation. I think we started using these you know engineering of channel, may be from 0.35 micro meter technology onwards, quarter micron technology and onwards, certainly we have been using pocket halos as well as super steep retrograde channel.

By doing this, we make sure that we arrest the short channel affects. At the same time we do not end up with having all the disadvantages, if we have done very flat doping concentration. Now, how do we achieve this? I mean, yes we know that this is desirable, but how do we actually do that ok. Let us now consider that before we talk about the source drain engineering.

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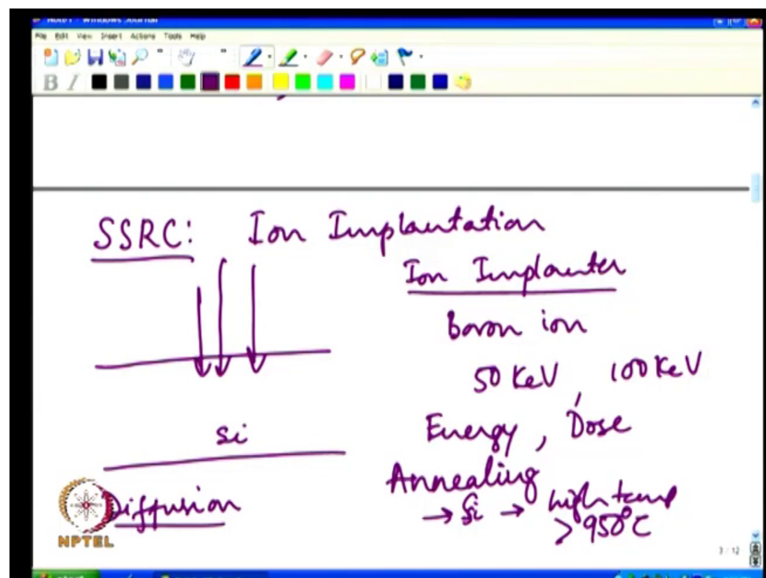

Let us take you know one by one, first take super steep retrograde channel. Typically whenever you want to, you know introduce impurities in silicon you use a process called Ion implantation. What it means. Essentially means is that, let say I have silicon. Let us say I want to introduce, convert this into P type doping concentration with appropriate impurities.

Certain region of the silicon needs to be converted into p type silicon let us say. What you do is that you bring this silicon wafer into an equipment which is called, you know Ion implanter, as you would have guess that Ion implanter is used to do Ion implantation. This Ion implanter can extract the required Ions, if you want to do a p type doping, it may take boron Ions which is very typical doping for p type.

You take boron Ion and accelerate the boron Ion at very high electric field. So, there are you know lot of knobs in the implanter equipment to set your electric field. For example, you know typically you can accelerate to very high electric field like 50 kilo electron volt or 100 kilo electron volt and So on and so forth by having a electrostatic acceleration, you give sufficient energy to this Ions, and they will essentially come in and get implanted to silicon. This is a process of Ion implantation.

It is like you know shooting bullets, you have a substrate you have these Ions which are like bullet us which are at very high kinetic energy. They go into silicon, once they come into silicon they go through a series of scattering processes, because silicon has this regular arrangement of atoms. Every scattering will decelerate this Ion and it will lose its energy eventually it will come to a halt.

So, the Ion implantation has two important process, you know process parameter; one is what we call energy, how much energy have you given, depending on the energy depth of implantation is determined, and the other one is dose. How many Ions that you want to introduce at a given energy. These are two important a metrics, but you see the Ion implantation process is always a disruptive process. Meaning that you implant it and it will destroy the crystallinity of silicon, because this is a high energy Ion coming in and it will displace the silicon atom.

So, in variably after Ion implantation you have to do a processing called annealing. Annealing is essentially subjecting silicon wafer to high temperature typically of the order of 9 50 degrees or more. The idea is that well you have disturbed the silicon lattice, you give thermal energy. This thermal energy will let the silicon atoms to go back and you know sit in their preferred lattice sides. So, that is how you repair the damage ok.

Now, a coronary is that, whenever you do annealing there is also process called diffusion. Whenever I heat silicon to temperatures like 950 degree centigrade, any impurity inside silicon can start diffusing from higher concentration to the lower

concentration, its just analogous to diffusion that takes place in gases, diffusion that takes place in liquids, except that this is what is called solid phase diffusion.

When silicon is solid not at room temperature, that room temperature things do not diffuse, but if you take it to you know 950 1000 degree centigrade then you know impurities and silicon can also diffuse from higher concentration to the lower concentration. Eventually the profile of the impurities that you get inside the silicon is due to a combination of annealing and diffusion.

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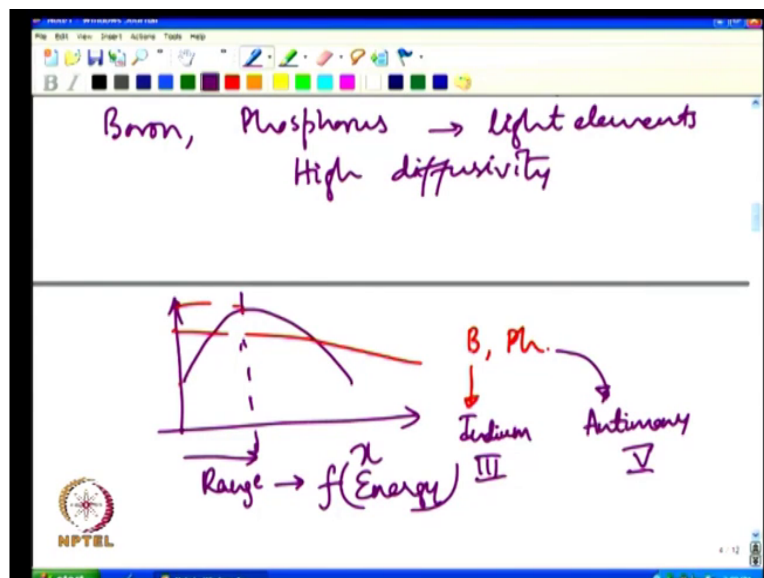

And in fact, most of the time with impurities, with impurities such as boron and phosphorus, which are the common impurities, which were common impurities for very long time is that they are very light elements. As a result of that they have high diffusivity light elements, we know we can call it imagine, very high easy to diffuse whereas the mass of the element is very large it will very difficult to diffuse it.

So, what is my implication of that? The implication is that; remember the kind of profile that I want to get along the x direction is something like this. This is what we called retrograde channel profile. Implantation as I said will let you determine what is the range, what is the peak. The range essentially is the peak of the Ion implantation.

Where you know, there is always a Gaussian distribution. Whenever you try to introduce impurities through an implantation process not all impurities will go and stay at the same

location, you know the reason for that is that it is a random process you see the Ion is coming in and it goes through a collision. Collision will deflect it in any which direction, it is a random process.

So, depending on how many collision each will see and in which direction it goes some will go far into silicon, some will go much earlier they will stopped, because they will hit more collisions statistically speaking, and eventually have a distribution, but the peak of the distribution is what we call range of Ion implantation.

So, I could potentially use appropriate energy, because range as you know is a function of implantation energy like what I mentioned you know 50 kev 100 kev I can choose the appropriate energy, and say this is where I want to have the peak, but what I told you already, is that after Ion implantation you need to do the annealing you see, when you do the annealing invariably, if the diffusivity is very large after annealing, the profile may essentially flatten out.

You know. In fact, you know either flatten out like this, because they will diffuse from higher concentration to the lower concentration, higher concentration to the lower concentration, and rather than having a peak profile you will have a flat profile, and this is what you will see invariably with boron and phosphorus, because they have very high diffuse ability. In order to get a super steep retrograde channel profile what we need to do, is to choose the dopants which have very low diffusibility.

So, you implant them, and when you anneal. Annealing process should only repair the silicon damage, you see. Annealing is required because silicon has been discoid from its lattice side, and you just you know let the silicon come back to its lattice side; however, the dopers do not diffuse much, because they are heavy elements. And hence what we do is that instead of boron we use indium, which is also a column three material, ok

Instead of phosphorous, use antimony which is also a column 5 material, and this also a column 3 material in all state of the transistors if you are doing a super steep retrograde channel design, invariably you are going to use indium or p type dopant, and antimony for n type channel dopant. In addition to indium you also use you know boron as well.

Because what, eventually what would happen is that when you are building the transistor. This whole transistor will be built in what is called a p well, and similarly the p channel

transistor is built on a n well, and well itself has to be very deep you know this p well has to be very deep. I have shown you saying that the whole substrate is P silicon you know it may not be P silicon, it could be either n or p does not matter, but then you define the values of the appropriate concentration appropriate dimensions.

So, when you do that well, the well have to be very deep and the deeper part of the well which is ensure that you know there is no leakage from the n channel transistor to a neighboring p channel transistor. The depth is defined by a light element like boron, because the light element can go far away down, because you know same energy light element goes much further down. Whereas whatever you want to do near the channel you define that with indium ok.

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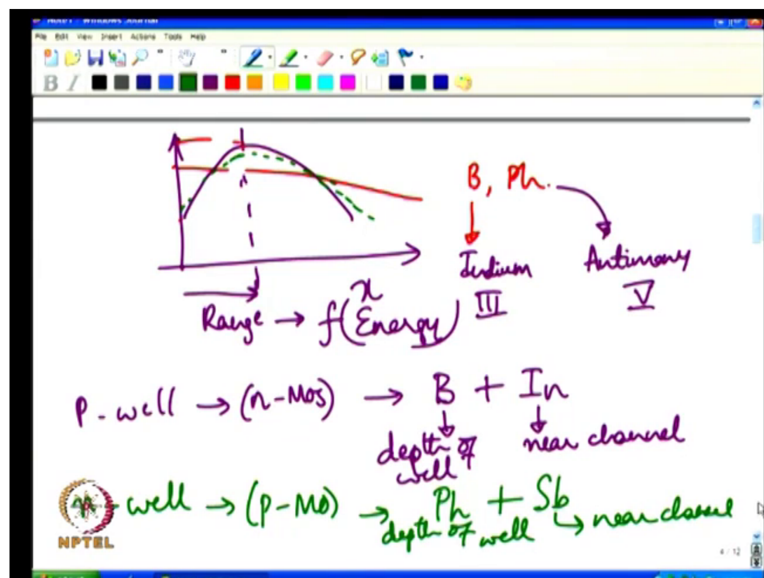

So, todays transistors really use a combination of, for example, if you want to do a p well, p well is what is required to define n channel transistor, this is for n mos. Use a combination of boron plus indium, and boron is defined, used to define depth of the well, ok.

So, that Ion implanter does not have to use very high energy to put indium very deep, but indium will really decide near the channel, how should be the doping profile. What I mentioned very low concentration near the surface, and you know peak somewhere in, and the advantage now is that, if this is your indium implantation and you subject this to

annealing. After annealing there may be very little diffusion, may be almost negligible diffusion.

You still be left with very high peak concentration here, very low concentration here, and very low concentration here. There is little bit diffusion may be, you know depending on what temperature what time you do, but nowhere compare to what would have happened with boron, and that is what we do here. And similarly for an n well, which is for a p mos transistor we make use of a combination of phosphorous plus antimony. This is near the channel and this is depth of the well again.

So, this combination will now ensure that you know I get the required doping profile, and I have done the channel engineering of super steep retrograde channel along the x direction fine.

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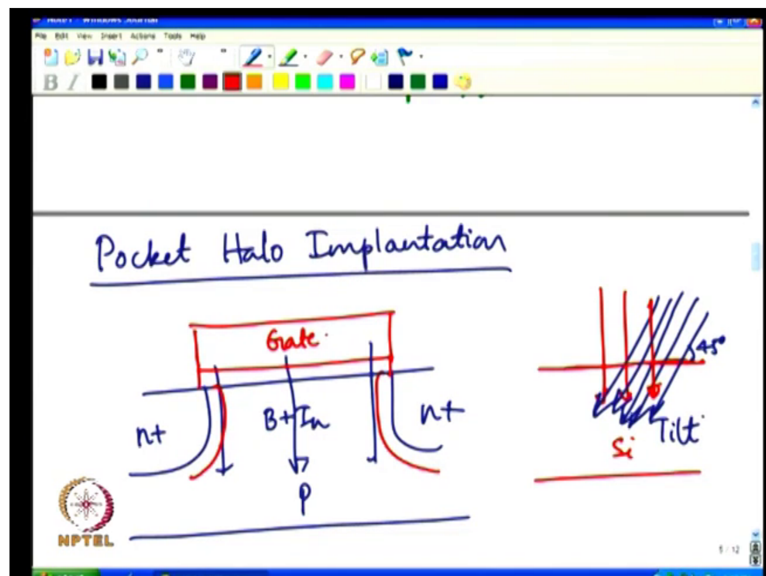

Now, let us look at the pocket halos. Again this is done using implantation, and that implantation process is called pocket halo implantation. What is the requirement for us?

Eventually I do this n plus junction and this is p type. Let us say I already done the x axis whatever doping engineering that I wanted to do, but it has been done everywhere like this, but now I have to define a non uniform doping concentration, meaning I need to selectively enhance the doping concentration in this region, and the doping concentration

in this region. And where is that region, that region turns out to be exactly at the gate edge. This is my gate.

And this is what we would exploit, and what we do is the following. During implantation as I already mentioned, you have silicon wafer and you introduce impurities, but implantation equipments also give you a flexibility to tilt the substrate during implantation, meaning, now the way it is the substrate plane the wafer looks like this. The wafer is flat here, and you are doing the, you know implantation out here which essentially.

You know this is a flat wafer, and the implantation is coming down at an angle which is 90 degree to the plane of the wafer, but I can rotate this wafer, during the implantation. And then the implantation species is coming at an angle to your wafer. So, I make use of this parameter of implantation, which is called a tilt angle, wafer is tilted ok.

So, if you were to do a tilted implant, let say I do a tilted implant, in which case I rotate the wafer with respect to your incoming beam. So, rather than rotating the wafer I will just show you the incoming beam which is coming at an angle, depending on how much is the tilt, the beam will be coming at the required angle.

Now, let us say I tilt the wafer by 45 degree, then these beam will be coming at an angle which is 45 degree fine. So, what I do is the following, usually this is p type, which is let us say a combination of indium plus boron which we have already discussed, I already defined in the x direction and selectively in this region I need to enhance my boron concentration.

So, what do I do first I pattern my gate electrode, gate oxide is there gate poly silicon or metal whatever gate, you know thick metal or poly silicon electrode is patterned here. Now I use this itself as a mask. So, this is sort of a self align process. So, what I do. I introduce boron at an angle ok.

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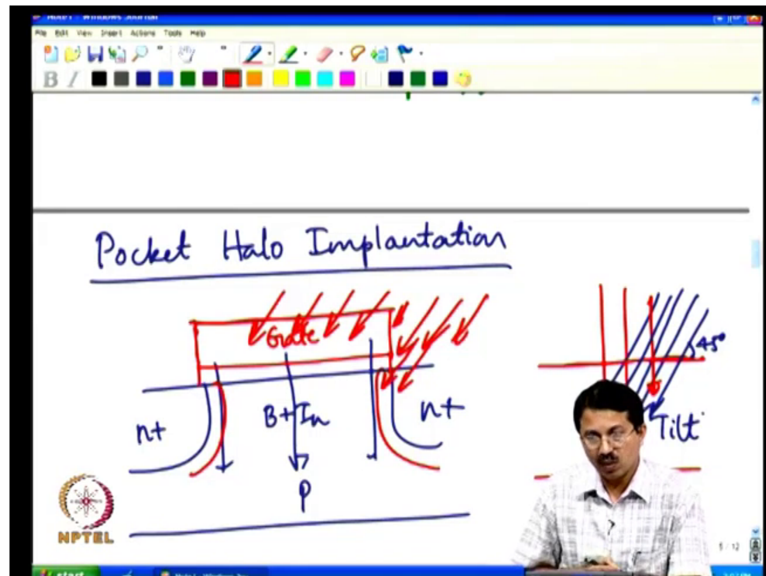

Boron is coming at an angle, when it is coming here it will get inside. Usually, the junctions are not yet formed junctions will be formed much later in the process. In one of the future lectures we will actually go through the entire process sequence of CMOS flow.

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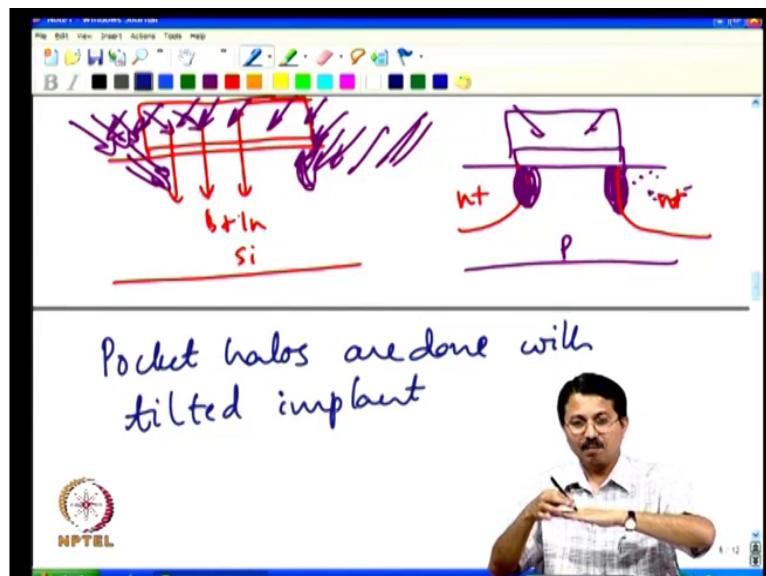

So, right now the way the wafer looks is that you are done the initial super steep retrograde channel, let us say that is your boron plus indium implant. It has been done

boron plus indium, and then you define your gate oxide, defined your gate electrode. Now you are doing this angled implant.

When this angled implant is coming, in this region this whole thing will be trapped here, because it will not go through the deep, a depth of this poly silicon, its fairly thick, but here it will just come in here. So, in this region, exactly where there is a gate edge; I been able to introduce the dopant just in this region, but access dopant has not come in this region, because this whole thing got trapped.

But this has come only at the drain end, but I also need to do it on this side as well. So, what do I do? I tilt the wafer the other way, and get the implantation done in this direction. Now when the implant species is coming, this will get inside here, but it will be all getting trapped in this region. In other words what you have been able to do, is that wherever you had this gate edge, only in this region you are able to increase the doping concentration selectively.

Of course doping has coming in this region also, but I really do not care, whatever has come in here as you know the whole thing is coming at an angle. Nothing to stop here this will be coming down here also, but subsequently this region will be counted of, then I make n plus junction there I am not really worried about that, but this region was the important region for me, where my p type doping concentration had to be increased and I been able to do that.

Whereas, this region the whole boron got trapped here and it got trapped here, and it dint reached this point at all. In the middle of the channel I maintain the low doping only at the edge, where eventually my source and drain will come you see as I mentioned, eventually my source and drain, I will counter dope is at n plus, I will also dope it as n plus. So, when I go from 0 to l, you have very high doping here, a very high doping here, and this what you do in terms of engineering the pocket halos.

So, the pocket halos again to sort of summarize; pocket halos are done with tilted implant. So, you till the wafer, you know you implant at an angle, as I said you know rather than in the pictures I showed wafer flat and this beam coming at 45 degree, but in reality beam is always coming down and you tilt the wafer like this. When you tilted the wafer, one side of the all transistors got implanted, but the other side is not implanted.

Then what do you do, you rotate the wafer, and again tilt the wafer. In other words you are implanting to the other side as well, and that make sure that implantation is done on this side here, in the picture down here, and the implantation is done on this side as well, and it turns out when we do the circuits, we do you know all these transistors in what is called, you know so called Manhattan geometry.

We lay them the transistors are laid either along the x axis or along the y axis. So, what I mean by that is that, if the transistor in the top view, when I looking from the top.

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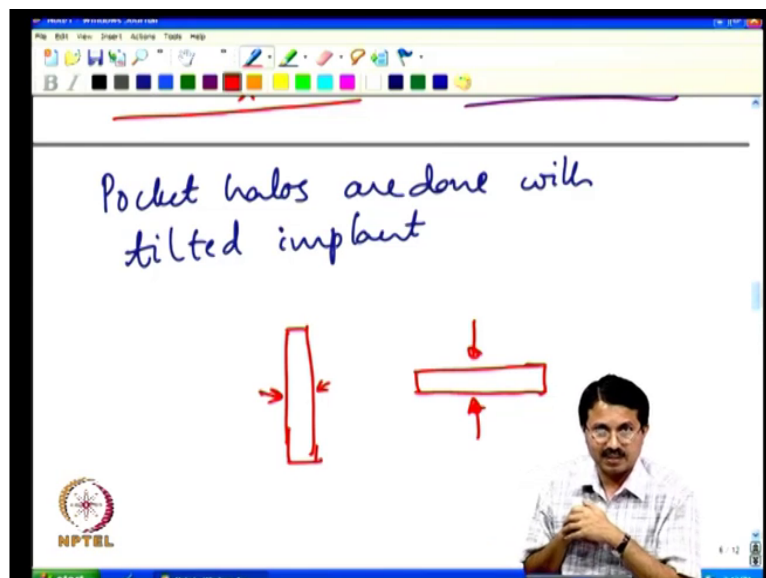

Remember this is my transistor gate, let us say, and the source is here and the drain is on this side, and this is the width of the transistor, this is the length of the transistor.

The transistors are either putting like this, or the transistors could also be put in like this, because its a large circuit you see, a millions of transistors, but they are not never put it any angle; that is essentially with this kind of consideration. So, now, what we do. We tilt the wafer and do the implantation here. We rotate the wafer by 180 degree, and do the implantation here, and again rotate the wafer and do the implantation in this direction, and do the implantation in this direction. All these are angled implants

So, we make sure that wherever you have this gate edge, you see at all the gate edges, irrespective of whether the gate is aligned like this, or gate is aligned like this. You are always doing the angled implant towards the drain side, towards the source side, to cover

all vertically aligned transistors and again at these angles and at this angle, again source and the drain of these transistors of all horizontally aligned transistors.

So, by having this you know very involved and implantation process, where you rotate the wafer, tilt the wafer, and introduce the dopants at the required angle, you are able to define pocket halos, but this is now a routine process, you know all the transistors routinely go through this process. So, by doing this you know we are able to get both the pocket halo implant as well as super steep retrograde channel implant.

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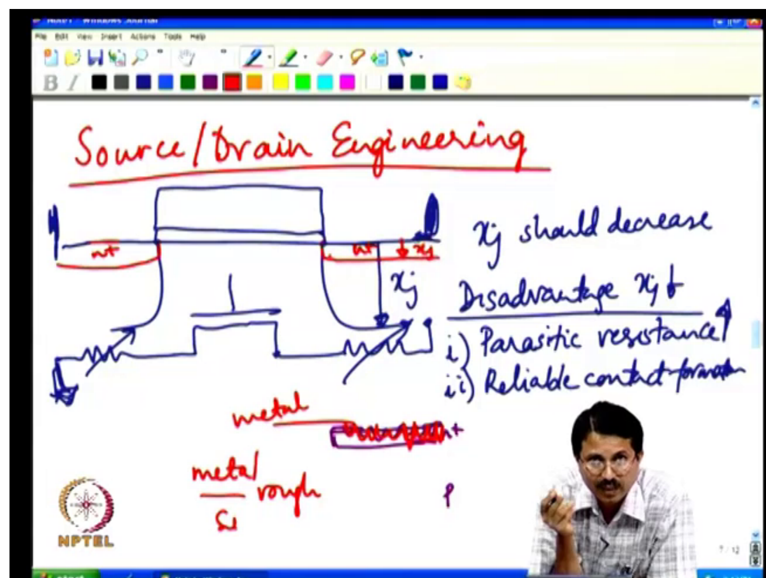

So, this is what we mean by channel engineering. The next important aspect is, the source drain engineering. So, again here what does the scaling theory tell you? This is the junction depth, with technology generation scaling; this xj should decrease, very obvious.

We already discussed the reason for that lower xj, instead of xj being here. If you have xj which is extremely shallow which looks like this, n plus n plus, very shallow junction xj, very low volume for coupling between drain to source. Here short channel effect goes down, Vt roll off is not as much. We have already discussed that based on a simple model called yaws model. Also the drain induced barrier lowering will also decrease.

But there is a problem here; there are couple of problems actually. What do the problems? You know just we were asking the question increasing the doping everywhere

at their problems. Yes there were problems, and we use channel engineering to overcome that. So, disadvantage here, disadvantage of xj coming down. First the parasitic resistance of the transistor increases. What is the parasitic resistance? We already sort of discuss this. My transistor which is gate controlled is only this this this region.

So, if you were to write a circuit equivalent, eventually your transistor contact will come somewhere here, and a transistor contact will come somewhere here; a metal contact. We have seen this in one of our earlier lectures. I have shown you this, if this is ground potential at the metal, then there is this resistance, and then this is a transistor which is controlled by gate, circuit schematic, and then again there is a resistance, and this eventually goes to your supply. These resistance are killer, this is what we call parasitic resistance, and shallower the junction versus a parasitic resistance.

There is another problem, and that is reliable contacts. Reliable contact formation is an issue. What do you mean by that? You see eventually you make a junction here, let me just blow up that region, just blow up that region, n just that region here. So, this is the junction, this is n plus p junction and I need to put metal here. When I put metal, and after that it goes through lot of thermal cycling you see, invariably there will be what is called metal spiking ok.

This is, you are putting the metal. So, let me just sketch it with a different color. This is metal, and a metal to silicon this junction is very rough. Its not atomically you see, there is going to be, what is called these spiking or undulations here. If you have a extremely shallow junction, you may actually spike through the junction.

Then you have a, you know reliable junction, which is not good. So, this is the problem. So, again you know we need to reread to a balancing act. I need to be able to shallow junction, at the same time I do not want to encounter these problems of higher resistance and dealing with the non reliable, unreliable contact and so on and so forth.

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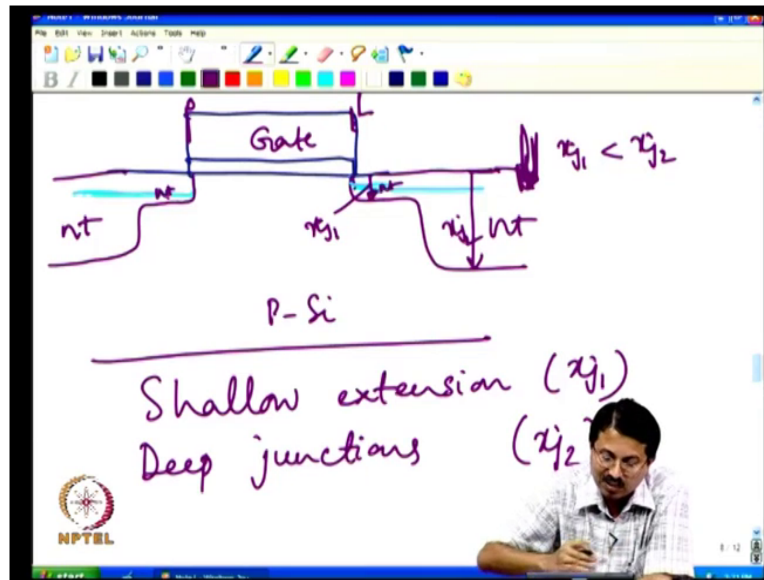

So, this is where I do what is called source drain engineering. So, in other words when I built source and drains of the transistors ideally I would have like to build a very shallow junction, which would look like this, but there is going to be lot of problems with this kind of a shallow junction. What I do. I do via media; I do something which would look like this.

So, this is now n plus, this is n plus, this is P silicon, and this is also n plus, it is the same n plus here, but you see the junction depth here, which I call xj 1, is less than this junction xj 2, let say xj 1 is less than xj 2. Wherever it matters, what is the important thing that matters; it is at the edge of the gate, the drain how does it couple into the channel.

So, in that region you make it shallow. So, that this is the region which is trying to couple to the source, and you know trying to influence, and this region is far away anyway. This the influence of this region on this region is not as much. So, this is what is called shallow extension. Shallow extension has its junction depth xj 1. And then as I go away from the gate edge. This is my gate you see. This is the gate edge which is 0, this is the gate edge which is l, this is the source side, and this is the drain side.

As I go away from the gate edge I make deep junctions, where junction depth is xj 2. You know this is something which will help you in addressing both the issues; your short channel affects will be minimized, as per the scaling guideline, you have anyway

decreased junction depth, because this is the region which will for all practical purpose control your short channel affects, drain induced barrier lowering and So on and so forth

At the same time, eventually you make the contacts here, and in this region you know you have deeper junctions, and also in this region your contact resistance will be lower, your parasitic resistance will be lower, because you have deeper junction. So, this is what you do to ensure that you have best of both worlds, you do a very reliable short channel you know sub hundred nanometer transistor using this kind of source drain engineering

So, none of the transistors today have flat source drain, you know the source drain profile does not look as if you know you have junction, which is going flat, and then then you know going up here. It always looks as shallow extension. This is an shallow arm which is touching the edge of the gate. The question is, how do you realize this.

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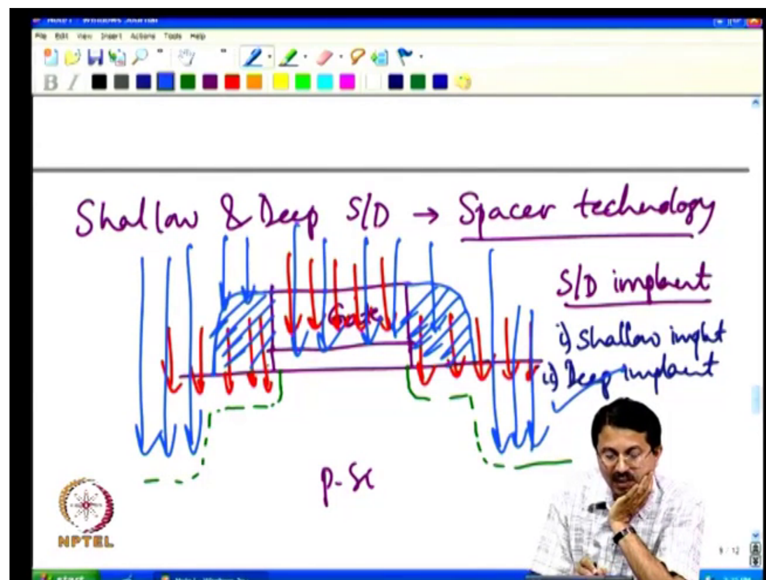

This is realized, the shallow and deep source drain, is realized using what is called spacer technology. What it means is the following you see. One is to get these junction energy, but just as I mentioned all the impurity introduction is done using implantation.

I have already done p type implantation here, you see p type well has been defined here, with the super steep retro grade channel, and the pocket halos here and pocket halos here, all that is done. Now I need to form junction, and junction is done by using arsenic implantation, n type implantation for a n channel transistor.

So, the idea is to do two step implantation. The source drain implantation is a two step process; first one is what is called shallow implant, and the second one is called deep implant. Now when you have this kind of a structure, when you do shallow implant? The shallow implant can go everywhere, it does not matter you know, the shallow implant can come even here, because anyway you want to dope it very heavily n type.

So, shallow implant should come everywhere. Again when you are doing the shallow implant, whatever is coming here is trapped in the gate you see, and that is how you do not get this entire dopant coming down here, that is why it is called as self aligned process. The gate edge defines where the source drain junctions get formed, and hence the name self aligned process.

In fact, during the same process, the poly silicon in a poly silicon gate technology the poly silicon also gets doped n plus in a n channel transistor. So, this is the shallow implant. Shallow implant will put your implant those species only at this depth, but I needed deep implant also, but when I do the deep implant, I want to protect this region, if I can somehow define region here, some insulator. And then after defining this insulator you do the deep implant.

So, when you do the deep implant, again the deep implant is coming down everywhere, because this has higher energy, you engineer the implant energy; such that and this thickness of the spacer such that, anything that is coming here will get trapped in the spacer, and only here it will go down. So, what have you done here? You have been able to protect this region, by having the deep implant go in. And hence whatever was implanted earlier for the shallow range is intact.

Whereas here in addition to this shallow range there is a deep implant, and hence you have deep junctions. Here you have shallow junctions, here you have deep junctions. So, if you can. This is what is called spacer. This is a region which you know put this deep implant away from the gate edge, by a required dimension. How much should it be and all that is a detail of transistor design.

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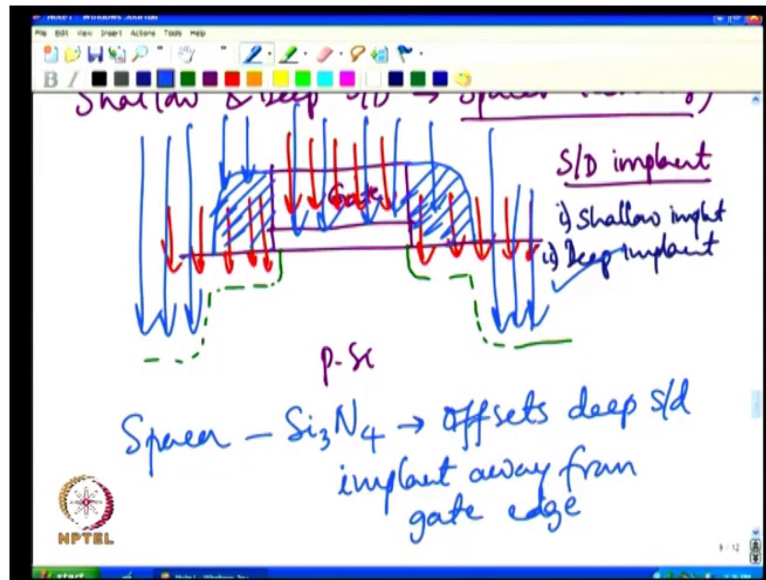

So, the spacer typically is silicon nitrite, and it offsets deep source drain implant away from the gate edge; that is the whole idea. So, at the gate edge, where it matters shallow junctions, you will retain shallow junctions, but away from the gate, defined by the spacer thickness you have deep implants. So, this is essentially done, you know with the series of you know some very simple, but very intelligent process steps.

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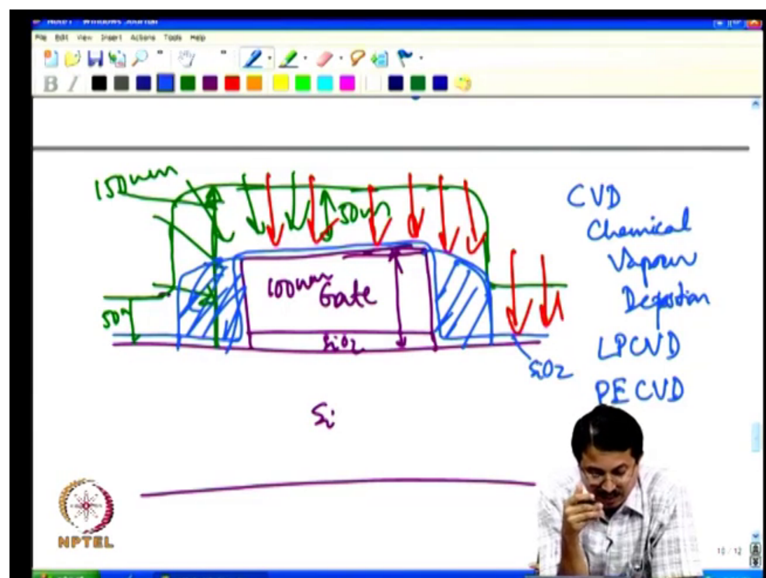

What is done essentially is that, you have the silicon wafer, you already defined this gate. Gate is defined using photolithography you see, depending on what is the length and

width of the gate, you have printed that already. This is SiO 2, and this is gate; either poly silicon or metal depending on which technology you are your looking at.

Now, what you do is that, you do a insulated deposition here, and that is done using a process called CVD or chemical vapor deposition. In fact, you know either make use of, just the low pressured chemical vapor deposition which is called LPCVD or PECVD, which stands for plasma enhanced chemical vapor deposition.

One of the key aspect of CVD process is that, the process is what we say conformal. Meaning wherever there is edge, the deposition happens along all the edges, the contours are preserved. So, typically what you do is that, if I want to build a silicon nitrite spacer, I could have directly deposited silicon nitrite, but eventually I want to etch silicon nitrite.

So, while etching silicon nitrite, the selectivity of silicon nitrite etch to the silicon, because I have to stop on silicon you see, is not so great. So, you do a very thin silicon oxide first of all through CVD. So, what this silicon oxide CVD does is that, it deposits silicon oxide everywhere. This is a very thin SiO 2. You follow it up with a thicker silicon nitrite.

So, your silicon nitrite will look something like this. As I said it follows the contour. All it means is that the reaction happens through chemical process, chemical reaction at the gas phase. You introduce you know for example, for silicon nitrite, you introduced dichlorosilane along with ammonia, dichlorosilane silicon in dichlorosilane reacts with nitrogen in ammonia, and produce a silicon nitrite, and that silicon nitrite will come and condense on top of all these open areas; that is why this CVD process is conformal.

So, the corollary is that, something very interesting, let say I have this gate, which is gate stack, this is gate stack, oxide plus gate. Of course, silicon oxide is extremely thin. Let say this gate stack is of the order of 100 nanometer, which is 0.1 micro meter tall; that is how the gate stack is. And let us say I want to offset this you know to the left by another 100 nanometer let say. The way I have drawn it may be this is little bit thinner than this let say 50 nanometers offset that I want to provide.

So, it is not to the scale, do not worry about that too much. Let say I have deposited 50 nanometer, it will be 50 nanometer everywhere, except here very interestingly, it will be not just 50 nanometer, it will be this 100 nanometer plus 50 nanometer. It will be 150

nanometer, because what it did was that, it sort of try to confirm to this profile in a process deposition was happening from all directions.

This is how the CVD deposition was happening you see, and as a result of that if you look here you have much thicker thickness of the silicon nitrite. If this is 50 nanometer, if this is 100 nanometer, this could be 150 nanometer you see. And it is only at the gate edge, because it was trying to follow this contour. This is blessing for us.

Now, what we do. We do what is called an anisotropic etch of silicon nitrite. Anisotropic etch is a directional etch, it happens only in a vertical direction, it does not happen horizontal direction. Whereas isotropic etch is you know etching in all direction, if you do etching in wet chemistry, it is almost of the time you can also have anisotropic wet chemistry, but most of the time it is isotropic etch, but if you do dry etching its invariably what is called reactive un etching is an isotropic etch.

So, what I do now is etch a 50 nanometer silicon nitrite, but that is done anisotropically. If it is done anisotropically, the 50 nanometer is etched here, 50 nanometer is etched here, 50 nanometer is etched here. If this you are left with this region you see, because this region had much thicker silicon nitrite. And now I have got these nice little regions here, which we call spacers, which are exactly aligned to the edges here. This is not done using lithography step you see, that is why we call itself align.

If you do it with lithography, that is more complicated process, and then you do the deep source drain implantation ok.

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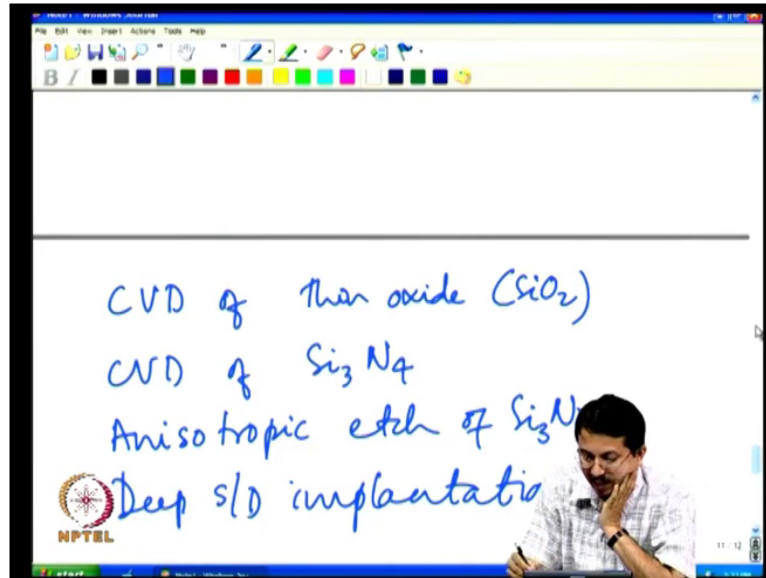

And hence you know the sequence of processes will be essentially CVD of thin oxide. Thin oxide just gives the etch selectivity, again silicon nitrite etch. Then CVD of silicon nitrite, then anisotropic etch of silicon nitrite that defines the spacer. Follow it up with deep source drain implantation, ok.

So, this sequence of simple processing steps will ensure that you have a very nice self aligned, and you know you have a very well behaved a junction profile, which is shallow here, spacer is defined, do deep source drain, all the impurities are trapped here, it comes only here, and deep junction and shallow junction.

So, then just recap and summarize what we have done today. We recognized that we need to do a channel engineering and source drain engineering, only then we get the best transistor performance.

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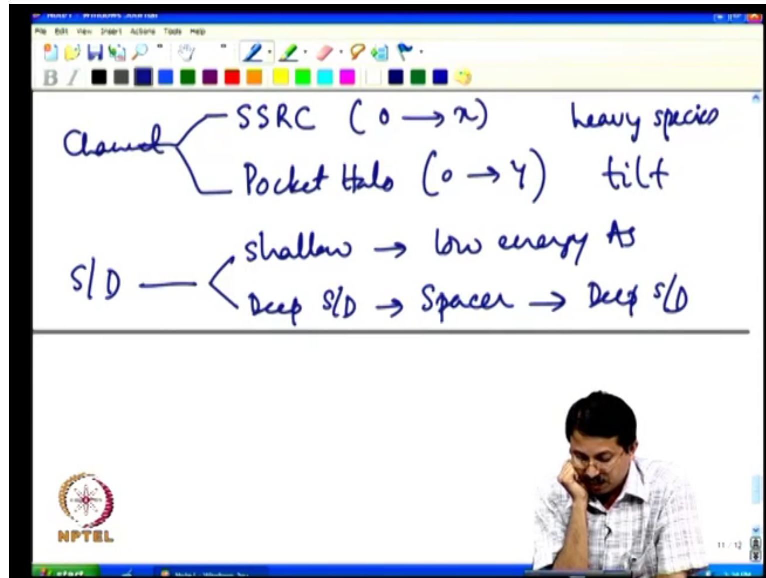

So, channel engineering is done using two different techniques; one is what is called super steep retrograde channel. This is the engineering the channel in the x direction, that is vertical direction, and then you have pocket halo; that is engineering the channel in y direction, and this is done using the tilt implant, and this is done using heavy species, like indium and antimony.

And the other important thing is, the deep source drain and shallow extension, and deep source drain. This is your source drain engineering. This is your channel engineering. Here first you do low energy implant, g arsenic implant, then do a spacer, and then do the deep source drain. This will ensure that you know you have a very well behaved transistor, which gives you the nice short channel performance. And your mobility will not be degraded, your drain induced barrier will not be worse contacts have very low, and no problem with junctions spiking and so on and so forth.

So, let us stop the lecture today. And you know we will continue further in the next lecture.