Nanoelectronics: Devices and Materials
Prof. Navakanta Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture - 05
Drain Induced Barrier Lowering

In the last lecture we had looked at the derivation of sub threshold slope and also understood the importance of sub threshold slope on controlling the leakage current, and we notice the how leakage current has increased over technology generations. So, in this lecture we will continue that discussion a little bit you know just to understand what are the factors controlling the sub threshold slope.

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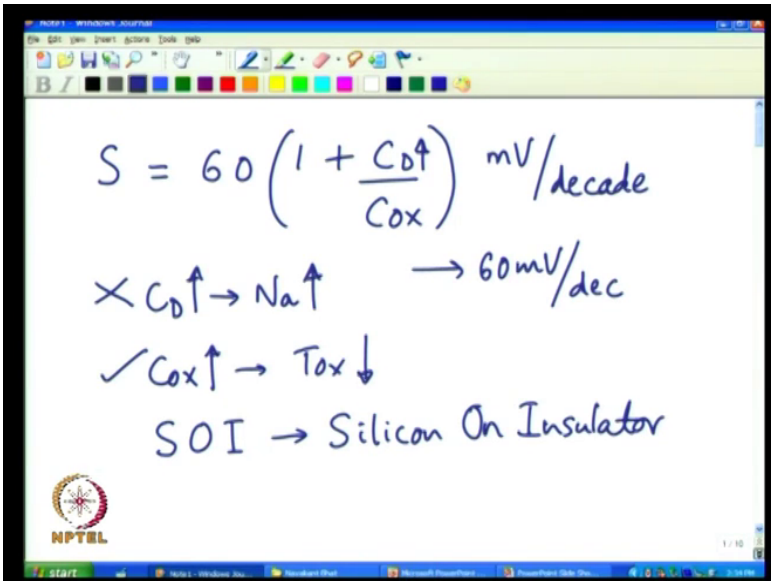

If you recall we had this expression for sub threshold slope which was given by this expression right and this is in terms of milli volts per decade right that is essentially the you know voltage required to decrease the current by one decade below threshold voltage right. So, if you notice a couple of things that become very apparent you know if CD is high then sub threshold slope becomes worse. Remember that this number should be as small as possible the best you can achieve is 60 milli volt per decade at room temperature. That is when you can ignore CD by C ox compared to unity right otherwise it is always more than 60 milli volt per decade at 3 degree Kelvin right.

So, you know CD in turn depends on the substrate doping right in particular you know you may recall the that substrate doping, if substrate doping increases CD will essentially depend on substrate doping, increase in substrate doping increases CD, simply because increase in substrate doping would reduce depletion width as you could imagine, and reduce depletion width essentially results in increased depletion capacitance.

So, depletion capacitance increases as substrate doping increases. So, you know this is certainly one of the concern increase in the substrate doping is detrimental in getting lower sub threshold slope. Now if you look at c ox right in this case increase in Cox is good because increase in Cox will make the sub threshold slope lower right.

So, here this is not good for sub threshold slope and this is good for sub threshold slope right. So, how do you increase Cox you can make use of oxide thickness as the parameter. So, in other words if you decrease oxide thickness as you can well imagine f cell Cox being inversely proportional to the oxide thickness, decreasing oxide thickness will help you increase the oxide capacitance which will in turn help you reduce this term and enhance the sub threshold slope which is also good right. So, the scaling you know as you remember indicates that oxide thickness has to decrease doping concentration has to increase as indicated by constant electric field scaling theory.

So, out of the 2 1 is favorable for sub threshold slope, but the other one is not favorable sub for sub threshold slope right. So, this is something you need to remember and. In fact, as we will see subsequently maybe in the next lecture that is why we do what is called channel engineering. In order to make sure that we get the best of both world meaning we certainly get the benefit by having decrease Tox, but even if we increasing substrate doping we do that intelligently. So, that we do not necessarily suffer very much in terms of sub threshold slope now.

So, what else you know could you do in order to reduce a sub threshold slope right. Now you see Cox if you look at that of course, increasing you know Cox is helpful, but can you make CD 0 right, but; obviously, not with a conventional bulk. So, called bulk silicon technology because bulk silicon technology as we have already seen there is going to be certain depletion width which is governed by you know that doping concentration and that will determine your depletion capacitance, but there is you know a variant of a technology which we sometimes call SOI technology where you will have a

lot of discussion on this SOI technology subsequently in one of the you know future lectures this essentially stands of for you know silicon on insulator. In fact, one of the biggest advantage of the SOI technology is that you can really achieve 60 milli volt per decade sub threshold slope and you can do that by really minimizing CD.

I mean of course, you can never make it 0, but you know in the limit it tends to very very small value right the way you do that in silicon on insulator technology is you know essentially you make this junctions remember, We have this source and drain junctions in MOS transistor, you have a very thin silicon film and you make this source and drain junction on this silicon film and this silicon film is really sitting on a thick silicon oxide this is very large right.

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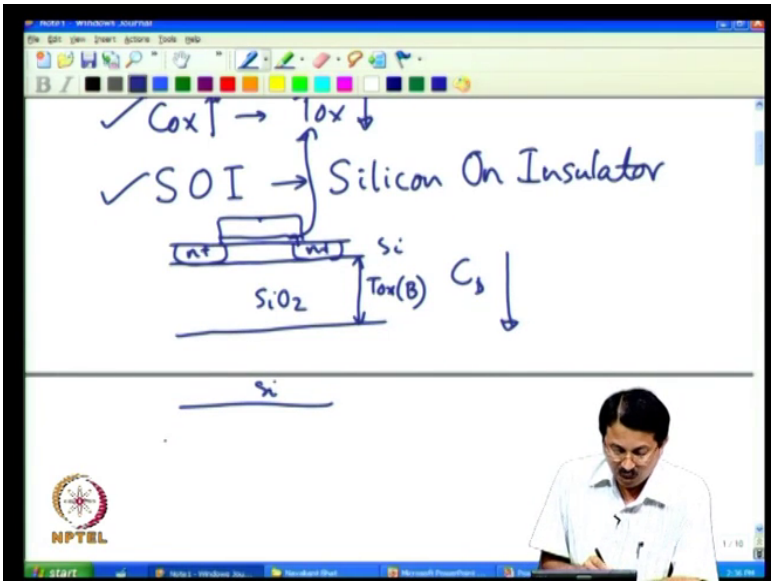

So, the fact that you have done this you know now your depletion width rather the capacitance which is going to be governed by depletion width is really you know this insulator thickness if you have a very large insulator thickness you can have a very very low capacitance. So, this is what one does in silicon insulator technology and tries to make sure that CD is brought down as low as possible this is happening because of this oxide thickness sometimes.

We call this as a buried oxide thickness just to distinguish from the gate oxide thickness right, typically when we write Tox you know that Tox corresponds to ultra thin oxide that is up here right. In amos transistor right, this Tox that we are referring to whereas, this

Tox is you know something that is sitting underneath the channel and of course, there is also silicon underneath that is why it is called silicon on insulator it is as if we have you have interposed a thick insulator in a silicon substrate. And this is one other thing that you could do and in fact, you would have more discussion on this subsequently in one of the future lectures right.

So, this is also very good for your decrease in sub threshold slope. Now there is another way you can minimize CD which of course, just for completeness of discussion. However, it is not always possible and in fact it may not make sense in most of the application that is using body bias.

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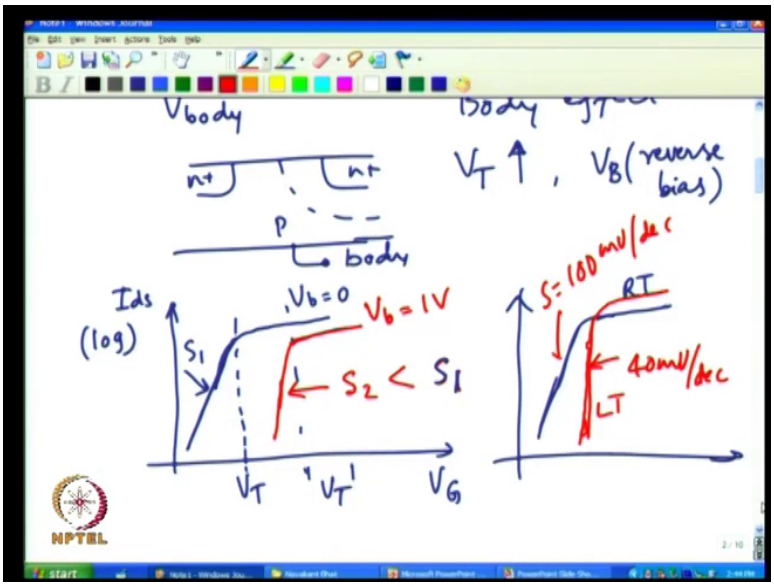

Remember the transistor is a 4 terminal device and if you may recall this P type this is the body correct in a n channel transistor. Typically you know when we talk of n channel transistor we say that body is at ground potential, but you can intentionally reverse bias this body you see by reverse biasing this body as you may remember from the basic MOS theory your threshold voltage increases, when you apply reverse body voltage. In fact, that is what is called body effect right body effect essentially means that your V T you know increases when you have V B which is essentially reverse bias.

So, this is what happens as far as threshold voltage is concerned; however, you know first of all as soon as you apply reverse bias this depletion width also increases you see and an increase in depletion width is good for you in terms of decreasing depletion

capacitance right. So, as a result of that you may expect that if you operate the transistor at different body biases, you will see a variation in sub threshold slope in particular at 0 body bias if you get a sub threshold slope of 100 milli volt per decade. As you start increasing the body bias that 100 starts coming down you see 100 may come down to 95 milli volt per decade 90 milli volt per decade and so on and so forth depending on what is the exact body bias that you have applied.

In other words if you were to look at your current voltage characteristics you have the drain current as a function of gate voltage right and as we have already seen if this is in a log scale you know your I d V G curve essentially looks something like this correct. And this is your threshold voltage point V T point and this is a sub threshold region and this is governed by the sub threshold slope right this is the sub threshold slope let us say this is at v b is equal to 0.

Now, if V b is a reverse bias on 0 voltage then what will happen is that 2 things will happen 1 is V T itself will increase as we know from the body bias says basic phenomenon right. So, V T will increase. So, your new V T will be somewhere here you know this is V T prime under a non 0 V T bias. So, that is one effect that you will certainly expect will happen and in addition to that what you will also see is that sub threshold slope becomes steeper. If this is your sub threshold slope under V b equal to 0 this is V b equal to let us say 1 volt and this sub threshold slope let us say S 2 will be certainly less then S 1, where S 1 corresponds to your you know sub threshold slope in this condition.

I mean as you can clearly see because see depletion has gone down that will decrease C D by Cox term and will decrease this sub threshold slope in other words the roll of this is much steeper that is what we want; however, it has come at an expense right it has come at an expense which is increased threshold voltage right. The increased threshold voltage is not good for your on current because increased threshold voltage will decrease your on current right. So, although in practice you can decrease the sub threshold slope using this technique, but you also suffer in terms of degraded on current.

So, this is not always the preferred technique to follow.

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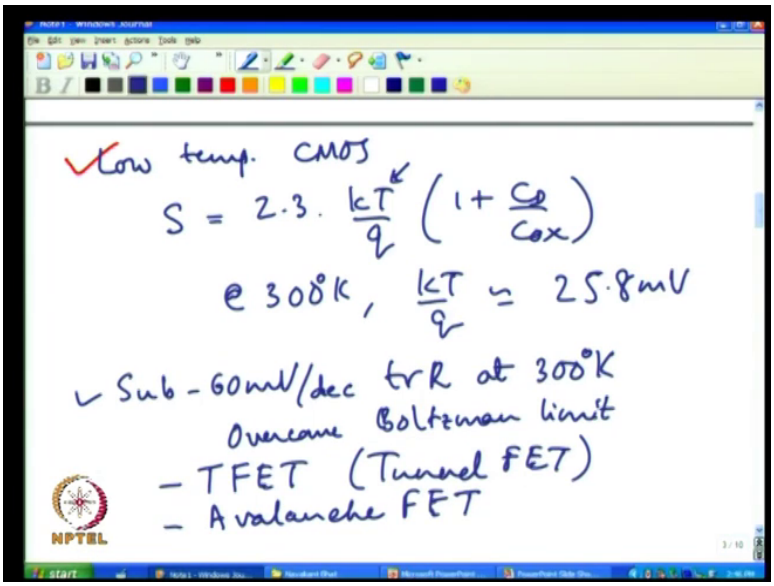

One other technique you know again which is very hard to follow, but there has been lot of research in what is called low temperature CMOs, remember I said sub threshold is sixty times 1 plus CD by Cox, but it is really 2.3 times k T over q 1 plus C D by Cox correct. And we said that k T over q at room temperature which is 300 Kelvin is at 300 degree Kelvin right, k T over q is approximately 25.8 milli volt and you have multiplied with that 2.3 and that is how you get that 60 as a number there. But you see here this temperature k is constant q is constant there is nothing you can do, but you can decrease this temperature, rather than operating the chip at room temperature or the typical commercial chips as you probably have seen from the spec sheet of these commercial chips.

They operate between minus 40 degrees centigrade to 125 degree centigrade that is the typical operating region right and room temperature. Let us say 27 degrees you know would correspond to 300 degree Kelvin. But what if you operate the chip at liquid nitrogen temperature you know some how you know pump in liquid nitrogen and really cool it to 77 degree Kelvin and you can immediately see that this T goes down from 300 to 77 and you would expect the sub threshold value to go down very dramatically right.

So, in other words you know if you have let me go back to the same graph here right, if you have you know characteristic which would look like this at room temperature if this is at room temperature. At low temperature you know you may actually see something

like this is low temperature, contrast this with what we were doing in you know increasing the body bias.

Notice that in fact, at low temperature your V T value increases you because there is an effect of band gap widening and that in turn results in increased V T; however, that increased V T does not necessarily degrade your on current your on current maybe actually better because you decrease the impurity I mean the lattice catering because temperature is very low mobility enhancement takes place. As a result of that you have large on current much better on current at the same time because the sub threshold slope is steeper your off current also decreases right.

So, this is best of both world you get best on current and best off current. So, if you can figure out a way to operate transistors at low temperature you know you know that is the greatest thing right, but we have not really figured out how to do that it is as if you know you will have to have a cooler with every chip that you have build and the cooler itself maybe huge right in order to cool the chip to the 77 degree Kelvin.

But that is something you may want to keep in mind that low temperature is certainly something that enhances your sub threshold slope meaning sub threshold performance the slope value decreases right the slope is steeper, but the way we define sub threshold slope you know you should not get confused with this is inverse of this slope you see, how many milli volt per decade change in current right and you know this will have a lower value of S, if this S here is 100 milli volt per decade, you know S here maybe let us say 40 milli volt per decade or even lower.

In fact, you can you know go down this 60 milli volt per decade limit. So, 60 milli volt per decade the so called Boltzmann limit right, which essentially comes because of the fact that the carriers have to overcome the barrier to you know conduct current. The Boltzmann limit value is different at different temperature because it depends on k T over q at low temperature it is much lower value and you know other than this low temperature is of course, very nice. But, of course again it is not really practical one of the you know biggest research that is happening in CMOs is really to achieve what are called sub 60 milli volt per decade transistors at room temperature. You see you know that is it is sort of what is called overcome the Boltzmanns limit right.

Ideally if you are building a transistor as usual at room temperature 630 milli volt is the best you can do right I mean that is dictated by Boltzmann statistics right; however, you know there are variants of transistors that are being looked at for example, you know there is something called Tunnel FET TFET which stands for tunnel FET. Here the conduction is not necessarily overcoming the energy barrier, whenever you have to overcome an energy barrier to conduct from source into the channel, there is always a barrier you see it becomes very clear when we look at the next topic which is drain induced barrier lowering, there is always this Boltzmann's limit you cannot do anything better than that.

But if you tunneling from source into the channel you can do much better than the Boltzmann's limit right. So, is not a work that is going on and there is similarly there are you know variants called based on avalanche mechanism right avalanche based FETs again these can help you to overcome that 60 milli volt per decade right. In other words you know in ideal transistors as you know should have as low value of sub threshold as possible right.

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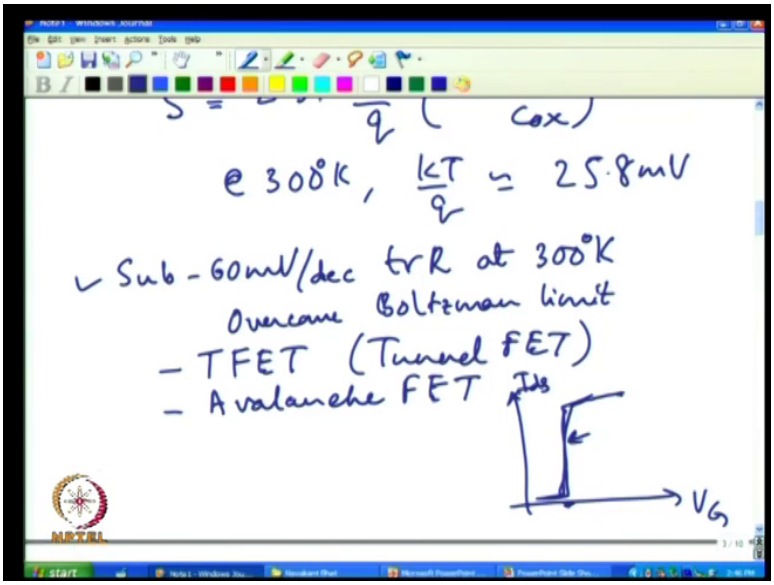

Ideally you would like to have a characteristic of Ids by VGs as some on current and instantaneously go to very low off current right. And this is ideally 0 milli volt per decade if you can right, infinite small value that you apply below threshold voltage

current should drop instantaneously by several orders of magnitude that is the best transistor that you can have.

So, these are some of the transistors that are being investigated like we are nowhere near really you know mastering that technology yet, but this is something for you to keep in mind. So, this is you know just to give you an idea that sub threshold slope is a very important parameter in a transistor design and you have to try and do whatever you can to minimize a sub threshold slope. There is different knobs that you can tune when you are designing a transistor you make use of all that and you know design the best transistor that you can.

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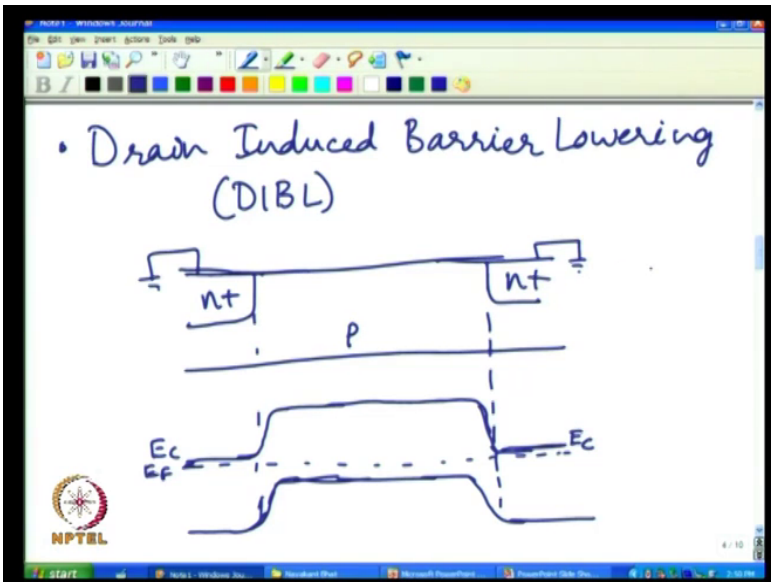

So, now let us look at another very important concept what is called Drain Induced Barrier Lowering this is abbreviated as DIBL DIBL is what we say.

So, let us look at this transistor n channel transistor and on a P type substrate you see there is a n plus P junction here and n plus P junction here. Now if I were to draw the just the conduction band you know I am interested just look at the band diagram energy band diagram right. I will focus only on the conduction band diagram let us say initially I have both source and drain at ground potential. So, when what you would expect is the following right this is a source and drainage right you will have E c which would look like this and there is this is P type there is an energy barrier there right and again it will

come down here right this is E c in n type region. E c in n plus region and this is E c in P type region these are very heavily doped almost degenerately doped right.

If you were to sketch the full band diagram the full band diagram would have looked something like this your Fermi level would have been very close to conduction band right, this is your E F when both terminals are 0 E F is flat there is no current flowing, your valence bands would have looked like this, correct this is n type Fermi level is very close to E c this is also n type verily very heavily doped Fermi level is very close to E c and this is P type and hence Fermi level is closer to valence band right. Of course, not as close to E v as this is close to E c because this is not as heavily doped as these regions are right. So, Fermi level is little bit away from the valence band.

So, I am not really interested in the valance part band right I am only interested in the conduction band part, because I am interested to find out you know when would these electrons come into the channel and how would they flow into the drain right that essentially what constitutes your drain current the carrier flow, electron flow, from source to the drain terminal.

So, now, let us look at the condition right this is when both source and drain are interchangeable now both are at same potential right it is a symmetric device they are at 0 voltage, but now let us say I apply a non zero voltage to the drain in a n channel transistor and let us see what happens.

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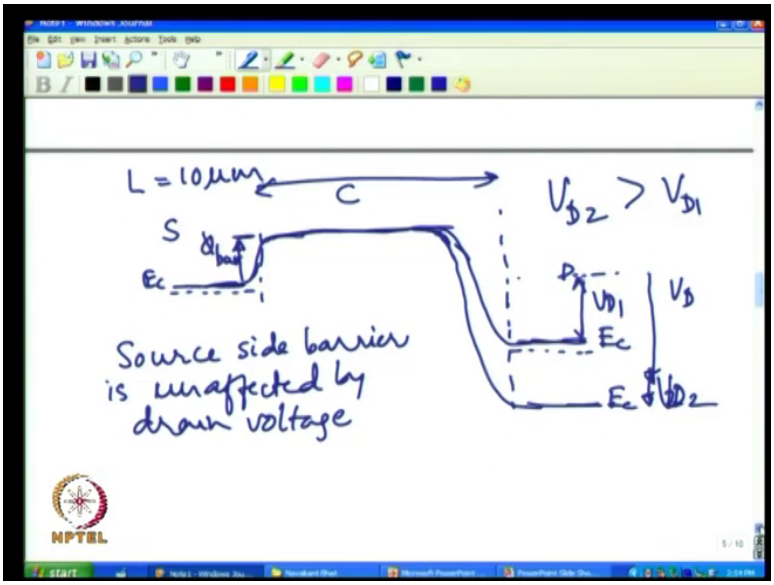

Let us consider 2 cases one where my channel length is long which let us say is 10 micro meter and let me see what happens here right this is let us say the source and drainage just have that picture over there and you know what will happen is this is E c, there is this barrier and what you have done at the drain side is you have applied a non zero drain voltage right.

So, a result of that there is an extra depletion width which is created right and you know accordingly you will have a band diagram which will look something like this. This is E c on the drain side this is source this is channel and this is drain and your E c on the drain side and E c on the source sides will be essentially separated by applied voltage, you see that is how the 2 Fermi levels. E c gets separated because the Fermi level here is here and the Fermi is out here applying a voltage in a system essentially you know moving the Fermi levels right.

Since I have applied a positive voltage on the drain side I have moved the drain Fermi level below the source Fermi level and this is how the you know 2 Fermi levels will look and accordingly 2 conduction band will look and the difference between 2 Fermi level or 2 conduction band levels is governed by applied voltage. And accordingly since you have this applied voltage there is this more band bending, because the reverse bias junction has higher junction potential now earlier that junction potential was essentially built in potential, that built in potential is not impacted on the source side.

But that built in potential on the drain side has been augmented by the reverse voltage that you have applied right and hence you have made the barrier on the drain side much larger compared to the barrier on the source side. Now the important point to realize is that when I start applying larger and larger drain voltage this is V D increasing. All I will be doing essentially for all practical purpose is essentially modulating only the band diagram at the drain side. This is for V D 2 V D 2 and this is for V D 1 V D 1 and V D 2 both are greater than 0 V D 2 is greater than V D 1 V D 2 is greater than V D 1.

So, whatever you are doing at the drain side that because a channel length is very long, the distance from the drain to the source being very long, this effect is not at all felt at the source side I mean source is far away from the drain any way. So, any disturbance that is being caused in the electric field depletion width everything happens at the drainage, nothing happens in the source side. In other words this barrier from source to the channel

this let me call it phi barrier remains unchanged in a long channel transistor irrespective of what drain voltage that you are applying. The only way to modulate this barrier is by applying gate voltage, when I apply a gate voltage I change the surface potential here and hence the barrier starts coming down, you see that is how the conduction takes place by applying a positive gate voltage this barrier would come down and there is more injection of electrons into the channel and as I start increasing the gate voltage there is more and more current flowing in.

So, that is how you know these things are in long channel transistors. So, let me just summarize that the source side barrier is unaffected by drain voltage. So, colliery of that is your conduction property of the channel or transistors are independent meaning the barrier here is independent of what you do at the drain side. Now let us look at what happens in a short channel transistor in a short channel transistor.

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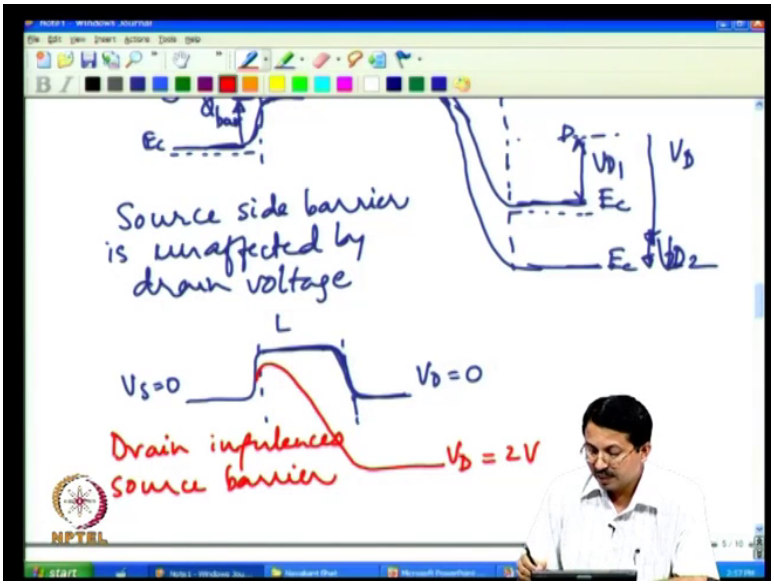

The source is very close to the drain, let us say at 0 bias this is my barrier picture it is of course, symmetric the drawing may not look symmetric right this is source side and this corresponds to V D equal to 0 and V S of course, is equal to 0. Now if I start applying drain voltage which is more than 0 non zero drain voltage positive drain voltage because the channel length is so small the drain electric field can actually penetrate all the way to the source and in the limit as l starts going down further and further this electric field can couple to the source more and more efficiently.

So, when I apply a non 0 drain voltage you may have a condition where in the resultant barrier could look something like this; this is V D non zero let us say V D is equal to 2. So, when a prime V D is equal to 2 volt not only that barrier at the drain has changed, but also because it is effect is felt near the source, it also modulates the source barrier you see if this happens you could imagine that there should be more conduction from source into the channel. In other words in a short channel device the drain influences source barrier and hence it is called drain induced barrier lowering at the source. It is the drain voltage that is responsible for this and what does it do it reduces the barrier for conduction at the source side right. So, that is what we mean by a drain induced barrier lowering.

Typically this effect of drain induced barrier lowering is that your threshold voltage of the transistor would get effected based on what is the drain voltage that you have ok.

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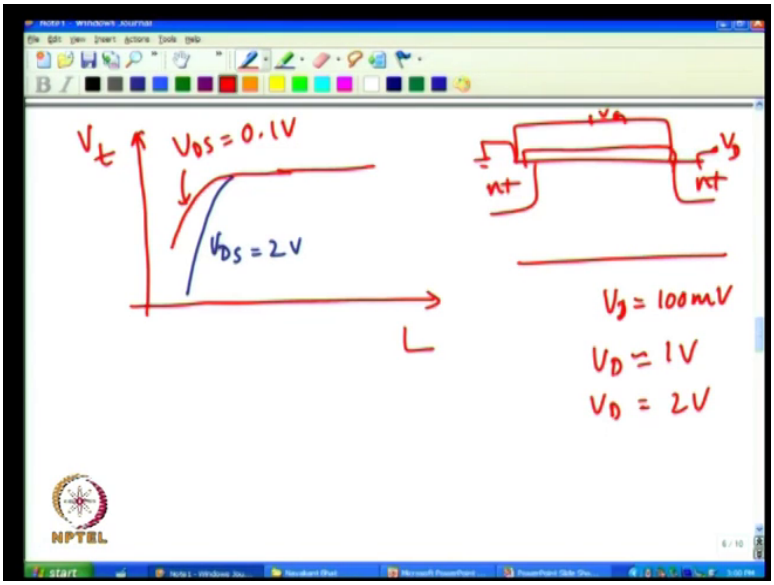

In fact, the drain induced barrier lowering it is immediate consequence is the following. If you were to plot V t versus l remember I had already told you in one of the earlier class that V t versus length, would look something like this and this is what we called short channel effect, when your length starts decreasing your V t would also starts decreasing very significantly. And this is flat at the long channel and it starts rolling off only at maybe at some microns of course, in nanometer regime it goes down very dramatically right and this is a V t roll off.

Now, when you do V t measurement right the way you do the V t measurement is that you apply a drain voltage and you stramp your gate voltage and you see when the transistor starts conducting. Typically threshold voltage of the transistor is independent of drain voltage we do not say that V t is measured at this drain voltage or this drain voltage the transistor has 0.5 volt at 1 volt drain voltage you know we do not say that transistor has 1 volt V t that is it right.

In other words the classical theory again says that the transistors threshold voltage is independent of drain voltage, but that is no longer true in an short channel device. In a short channel device you will have to also specify at what voltage are you measuring threshold voltage are you measuring threshold voltage, when V D is very small of the order of 100 milli volt or V D is large of the order of 1 volt or let us say V D is equal to 2 volt your threshold voltage value will be quite different and why is that and the reason precisely is because drain induced barrier loading.

Your conduction in the transistor is not only influenced by the gate voltage, but it is also influenced by the drain voltage in a very short transistor and more specifically you can expect that if the drain voltage is larger. And if you try to measure IDVG characteristics, you would expect a lower threshold voltage because this drain has already lowered the barrier and you know you do not need to apply as much gate voltage to turn on the transistor.

So, in other words if you were to specify a threshold voltage, especially at the you know very very short channel regime then depending on whether you have V D s is equal to 2 volt or V D s is equal to 0.1 volt you will see different threshold voltage. Again it does not happen in long channel regime in long channel regime whether you measure the threshold voltage 100 milli volt or 2 volt it is 1 and the same you see simply because as we have already discussed in the long channel regime the drains influence is not at all felt at the source side right.

So, drain does not help you in terms of turning on the transistor only if you have turned on the transistor then the drain can accelerate the carriers at larger velocity and hence you can have larger current, but you need to turn on the transistor, but in short channel devices drain can also help you to turn on the transistor. So, as a result of that the DIBL this is an immediate consequence of DIBL this is due to DIBL.

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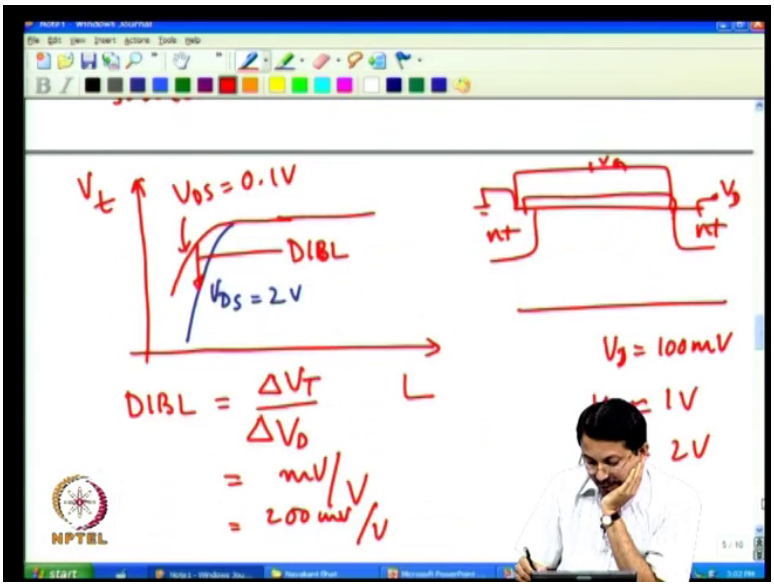

So, that is why DIBL is defined typically as delta V T per unit voltage. If you change voltage by a certain amount the drain voltage delta V T by delta V D let me make it more precise you change drain voltage by certain amount that changes your threshold voltage what is the change in threshold voltage for a given change in drain voltage. Typically it is referred to as you know something like milli volt per volt this is the unit for DIBL that is for example, you can say that my DIBL is 200 milli volt per volt that is rather than measuring the threshold voltage at 0.1 volt.

If I do it at 1.1 volt my threshold voltage would be 200 milli volt lower than what you would get at 0.1 volt right. So, that is the meaning of dibble. So, dibble is a very important effect in short channel devices and as a result of that you know you will have a significant impact on your threshold voltage and there are also what are called surface DIBL and bulk DIBL what is means is that you know.

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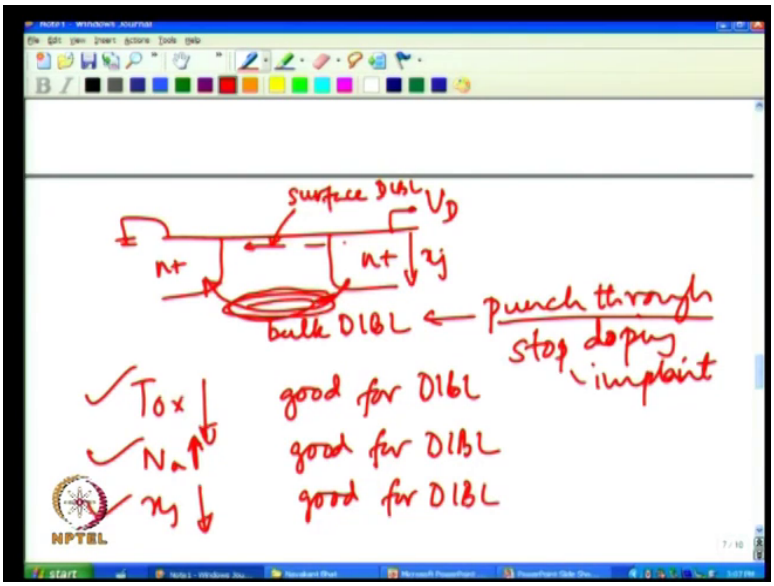

If you look at the transistor a short channel transistor again, remember this is drain voltage which is non zero this can couple to the source right. And change the barrier if this is changing the barrier near the surface then that is called surface DIBL, if it is changing the barrier in the bulk meaning deeper down that is called bulk DIBL.

So, this barrier can be you know impacted anywhere along this corridor that you have between source and the drain, and because of this you would also; obviously, expect deeper the source range junction the worse will be your dibble because there is larger area for you know drain to sort of couple to the source and you will have much more DIBL occurring if you have a shallower junction your DIBL is not as worse. Another very important point that I want to bring up here is that the surface DIBL can be controlled by gate voltage to some extent whereas, the bulk DIBL cannot be controlled by gate voltage because this is so far away from the gate your gate voltage is effectively screened by the channel and you would not be able to influence anything deep down.

And that is why invariably you know what you do in transistor design you essentially put in what is called punch through stop doping or punch through stop implant sometimes it is also just called punch through implant, what it essentially first of all what is punch through you know if you recall your bipolar junction transistor theory there is something called base punch through. If you start increasing the collector voltage, you know collector depletion will start spreading into the base region and effectively you know

may punch through the base right and there is an analog here you know you can treat your source as an emitter, you can treat your channel as a base and you can treat your drain as a collector right as you start increasing the collector voltage, you know there is this electric field sort of progressing into the channel and that is why this name punch through which is sort of taken from the bipolar junction transistor literature because the effects are similar.

In order to stop this punch through what you will have to do is that you have to selectively increase the doping concentration here. If you have higher doping concentration you will not let this electric field come in because you can screen the electric field, higher doping concentration meaning larger number of the carriers and hence the you know electric field will not penetrate deeper ideally for example, if you have a metal your electric field can be you know easily screened at a surface of the metal because metal has large number of carriers.

Similarly, high doped p type region will have large number of carriers which will help you to screen the electric field from the drain and will help you to prevent the DIBL, bulk DIBL can be very effectively prevented by increase doping concentration the surface DIBL can be prevented because it is. So, close to the gate by decreasing the oxide thickness you see if you decrease the oxide thickness you are making gates stronger the gate electric field becomes stronger compared to the drain electric field.

So, T ox going down is good for DIBL and n a going up as we did in punch bulk punch through again is good for DIBL and the junction depths what we call x j x j going down is again good for DIBL; meaning DIBL will be as small as possible if you have all these conditions. Now one other interesting point which of course, obvious from our discussion, but just for completeness, you know I will depict this graphically if you have to plot dibble on y axis as a function of channel length what would you expect.

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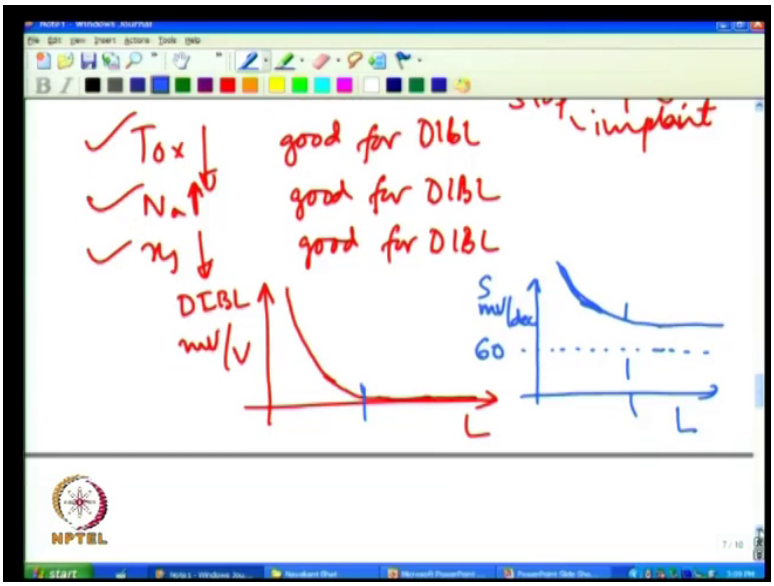

You see at large channel length your DIBL is 0 because the drain electric field has hardly any influence on the source.

So, your V T there is no difference whether you do V T at 0.1 volt or at 0.1 0.1 volt, but as you starting decreasing the channel length your DIBL starts increasing and as channel length start decreasing DIBL becomes larger and larger. Again this is evident because of the discussion that we had earlier the smaller the channel length more stronger is the electric field penetration into the channel at the source and more is the barrier lowering. And hence must more decrease in the threshold voltage and that is what you would expect here, and this DIBL interestingly also has an impact on sub threshold slope as function of channel length. When we looked at sub threshold earlier if you remember I talked about sub threshold being dependent on a variety of factors right such as oxide thickness doping concentration, but I really did not talk about whether sub threshold depends upon length or not.

Now in the context of the discussion that we had on DIBL if we were to plot the sub threshold slope as a function of channel length what you will see is the following. And let us say this is your best you can achieve 60 this is in milli volt per decade and this has you know is in milli volt per volt. When you have a long channel you do not quite have 630 milli volt per decade because we already discussed that 1 plus C D by Cox will make it little more than 60 milli volt per decade it may be 8 milli volt, 90 milli volt per decade

or 100 milli volt per decade depending on how good is your design. And when your channel lengths are large it sought of is constant you know it is really not dependent on the channel length.

But as you start decreasing the channel length you know at about the same channel lengths corresponding to where your dibble starts rising you also see your sub threshold start slope starts becoming worse.

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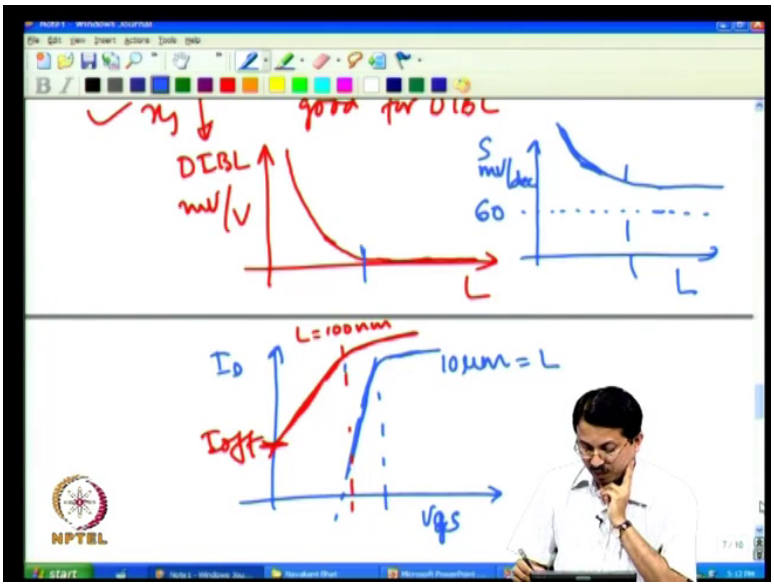

In other words you know what I am saying here is that right if you have your I D versus V g s characteristic, you know if for a long channel device if you have an I D versus V g s characteristic which looks like this, for a short channel device what you may have is you know something like this. This let us say is for 10 micrometer length and this let us say is 100 nanometer, what do you see here first of all V T is whenever we plot a sub threshold slope the transition between the exponential behavior and a quadratic behavior is a threshold voltage.

First of all in short channel device 100 nanometer against 100 micrometer or 10 micrometer does not matter your V T has decreased because of short channel effect and that is why this point has shifted to the left that is one aspect. And your sub threshold slope has become worse compared to this on a long channel device we have a steeper roll off whereas, in a short channel device you have much worse roll off.

And hence you know because of both these factors because of the fact that V T has decreased and because of the fact that sub threshold slope is also bad you end up with very large off current this is your off current right whereas, you know the off current here is very small you know it goes down because this is in log scale. Why does this happen because your source barrier it is not just controlled by the gate it is also controlled by the drain.

Now drain is also influencing your source barrier right as we have discussed earlier through the graphical representation, as a result of that you know you suffer in terms of sub threshold slope your gate control is not as good and that is reflected in sub threshold slope as well and that is why as my channel length decreases my sub threshold slope becomes worse. So, the DIBL has a very important implication and that also impacts your sub threshold slope.

I think we have we have covered all that we wanted to discuss on DIBL. I think we have discussed most the effects that the short channel regime, but let me just discuss in the remainder of the time for this lecture about the field effect mobility and you know after that we would be in a position from the next lecture to start talking about how would one design a transistor in these highly scale technology.

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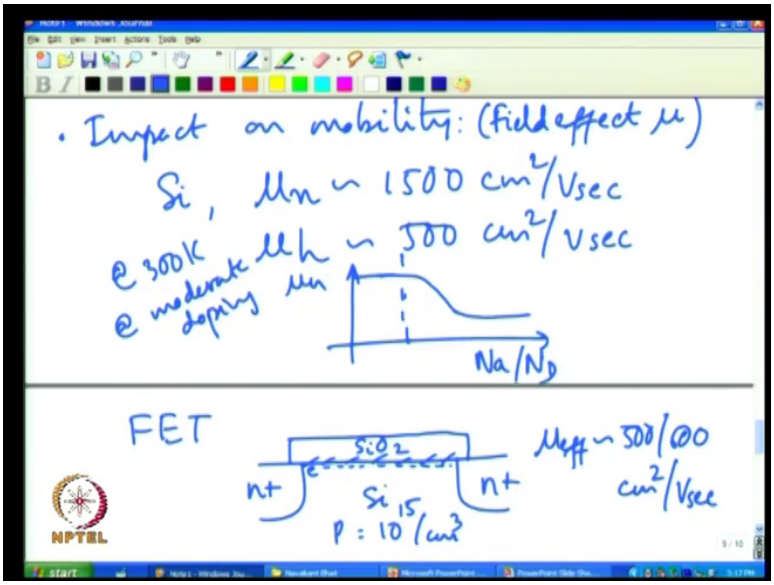

So, you know the impact on mobility due to various factors that we have in the transistor right let us understand that first of all you know this is what we call field effect mobility as oppose to the mobility that you would have seen in a bulk semi conductor.

For example, in silicon we say that when doping concentration is reasonably small not very high doping concentration the small doping concentration your electron mobility is of the order of you know 1500 centimeter square per volt second and your whole mobility is of the order of maybe 500 centimeter square per volt second correct. These are the typical mobility values which you have studied in the basic a semi conductor devices, I said at this is first of all at 300 degree Kelvin and at moderate doping. In other words mobility is a strong function of temperature because of the lattice scattering.

And Mobility is also a strong function of doping concentration once you start increasing the doping concentration beyond a limit especially if your doping concentration starts increasing beyond 10 power 15 10 power 16 you will start mobility degrading. You know more particularly you may have seen the mobility versus doping curves N a or N D, which would essentially look something like this initially it is flat constant maybe 1500 for electrons and then it starts decreasing you know it really decreases very significantly a higher doping concentration result in higher scattering and that is detrimental for your mobility.

But when we talk of FETs we really talk of field effect mobility in other words the mobility that we are interested in is for the electron, which is flowing very close to the surface. As oppose to an electron flowing in the deep inside a bulk silicon vapor, current is due to electrons flowing like this you see current is due to electrons flowing right out here at the channel and what do we have at the channel at the channel we have 2 dissimilar metal materials. SiO 2 is sitting on top of silicon; this is silicon and this is SiO 2 right. So, there is a non ideality there is an interface between silicon and silicon oxide and this interference results in lot of defects where the bilk silicon is highly pure defect free almost the surface has lot of defect and as a result of that even though you have the silicon p type region here.

Let us say my p type region has doping of 10 to the 15 per centimeter cube or 10 to the 14 per centimeter cube. This 10 to the 14 would have been in this region, you would have expected a mobility of 1500 for electrons right, but it turns out if you do a mobility

measurement in a transistor you may get something like 500 600 max you may not get more than that, for electron mobility at 300 degree Kelvin even though the doping is moderate.

So, the effective mobility is much lower you know of the order of 500 600 centimeter square per volt second for moderate doping of course, if you start increasing the doping the mobility will go down further, but first of all the reason why this happens is you know you have this defects at this interface these defects also start acting as a scattering sites. So, when this electron is moving it is not able to move freely, it gets scattered because of the charge present at the interface and hence it lowers the mobility.

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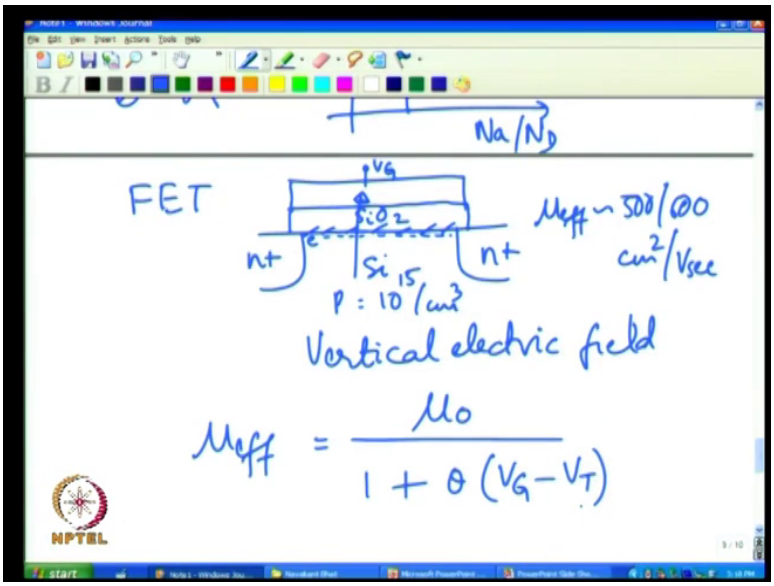

So, this is essentially a very important effect and not only that if you start applying gate voltage larger and larger gate voltage, that also starts degrading the mobility even further you see and that is because this large and larger gate voltage is setting up an electric field qualitatively speaking in the vertical direction. It is trying to pull these electrons in the vertical direction right and you know because of that you know there is more scattering here right and the ease with which the electrons can go along the channel and get collected in the drain goes down it is not so easy to do that.

So, a result of that mobility also depends on the vertical electric field. So, in other words we can actually write this effective mobility as some mu 0 right some theta some fitting parameter V G minus V T.

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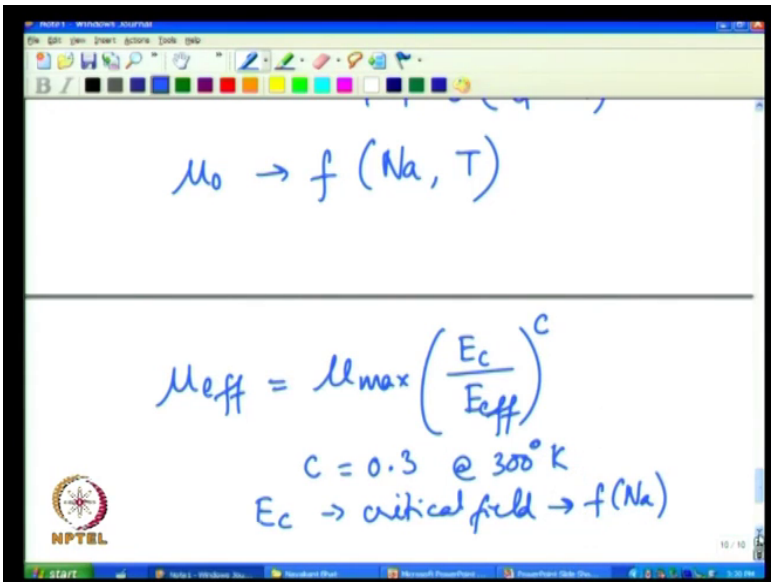

Where mu 0 is of course, a function of you know doping concentration that you have in the channel higher the doping concentration to begin with your mobility is lower and in addition you know it also depends on temperature, but if you are operating the transistor at 300 degree Kelvin you that is the mobility that we are interested, but in general it also depends on temperature.

So, having determined that subsequently V G minus V T which is a vertical electric field, once you have created the channel once V G is greater than V T there is this current flowing the vertical electric field will also impact your mobility very significantly. Sometimes you know we also use a slightly different model for this mobility. There are lots of models which are available which says you know your mobility is given by E c by E effective to the power some constant c. Where this c is about 0.3 at 300 degree Kelvin if you are interested in the mobility at 300 degree Kelvin that is at the room temperature and E c is called you know critical field which of course, is a function of doping concentration.

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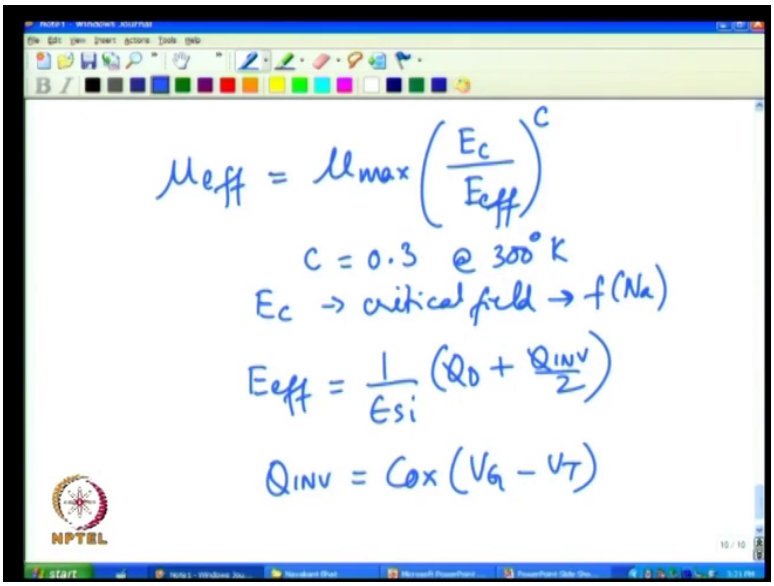

What is the doping concentration that in turn depends on that in turn governs what is your E c value and E effective is essentially given by this term here 1 plus epsilon silicon times the charge that you have which is can be approximated by this. Q D is the depletion charge Q inversion is the inversion charge, as you start increasing your gate voltage your inversion charge also increases. Remember that your inversion charge Q inversion can be written as Cox all these are in per unit area column per unit area ferret per centimeter square right V G minus V T.

As you start increasing V G minus V T effectively they are sort of related you see you know here we had V G minus V T in the denominator correct where theta was a fitting parameter the mu; mu was so of a inversely dependent on V G minus V T. And here you have this E effective term and E effective in turn is given by this and this Q inversion has this V G minus V T term again you see that there is one over V G minus V T dependency sort of captured.

So, in other words you know we you sometimes see in literature what are called universal mobility curves, which essentially plot mu effective as a function of E effective that is the effective electric field and you know that would look something like this.

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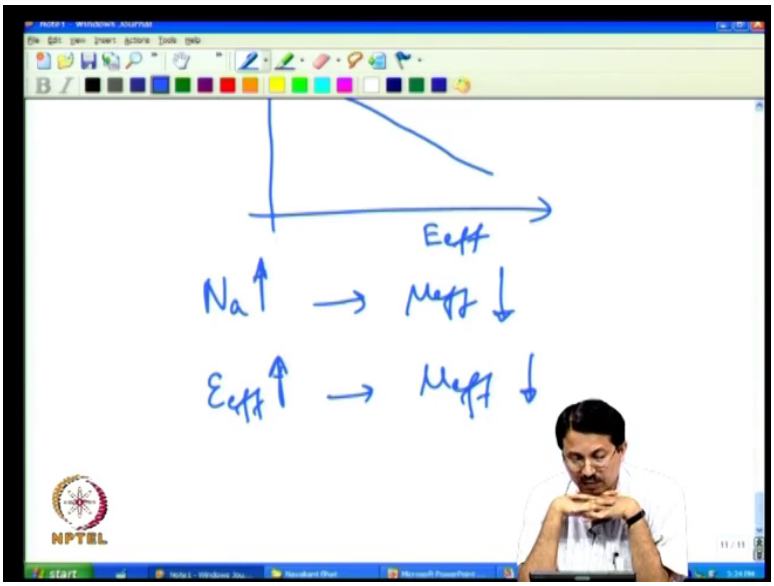

As the effective electric field which is defined you know based on the equation that we saw just a minute ago this right as that electric field increases which is capturing the vertical electrical field doping concentration all that effects are captured.

So, you know the effective mobility starts going down. So, the take home message in terms of mobility is that first of all in transistors field effect transistor the surface mobility, the field effect mobility is certainly lower than the bulk mobility, you can never approach numbers like 1500 for electron and 500 for (Refer Time: 54:07) it would always be less than that because of the defects at the interface, and on top of it if you have higher doping concentration that is not good for your mobility, if you have higher vertical electrical field that is also not good for your mobility.

What it means is that if you recall our constant electric field scaling theory or generalize electric field scaling theory which said n a should be increased right which of course, is not good for mobility, this in turn immediately degrades your mobility significantly. And it also we discovered that we do not necessarily constant electric field scaling theory, instead we have let the electric field rise over the years. If the vertical electrical fields are increasing right E effective is increasing vertical electrical fields are increasing that is also bad for your mobility.

So, trying to restore this mobility is one of the most crucial aspect when you are designing a transistor. As we will see from the next lecture we do lot of things in order to

get a very good transistor you know a very good transistor, which would have largest on current for a smallest off current, it should have a largest on current for a smallest capacitor and that is what called is called a D C matrix of a transistor and an A C matrix of a transistor and that is how we should be able to design a very good transistor.

So, in the next lecture we will look at various concepts related to transistor design more specifically what are called channel engineering source drain engineering and so on and so forth. So, to summarize this lecture we looked at sub threshold slope and dependence of sub threshold slope on various factors and we discovered that there are various knobs that you can tune for example, doping concentration needs to be decreased, but that is very difficult scaling theory does not let us do that.

So, maybe we can do various other things such as using silicon on insulator devices and you know thinner oxides and things like that we also looked at what is called drain induced barrier lowering which is a very important concept, which will impact the way the transistor will behave especially at the short channel regime. And we also looked at the mobility which is a very important parameter you know mobility of course, will be degraded, because of the vertical electric field because of the defects at the interface and also because of the increased doping concentration.

So, with that we will stop this lecture done.