Nanoelectronics: Devices and Materials
Prof. K. N. Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture - 30
Hetero- junctions and High Electron Mobility Transistors (HEMT)

We will have the one more the last presentation on this non classical MOSFETs.

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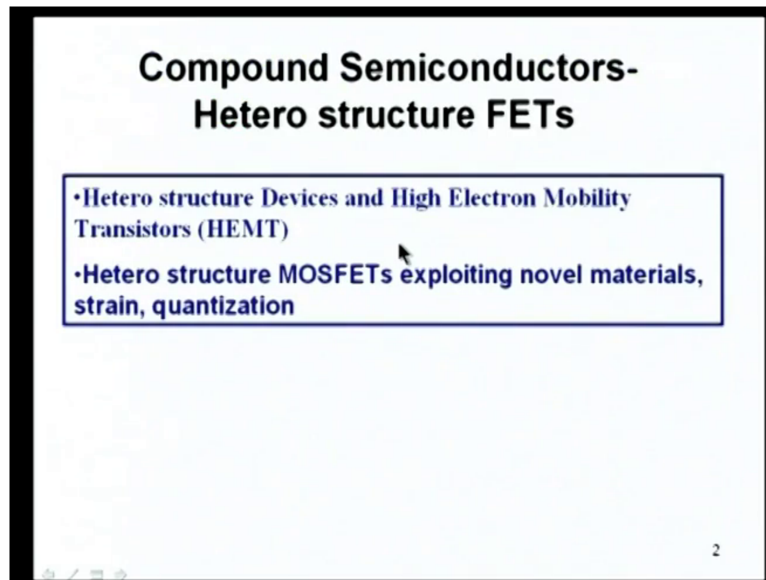

Now will continue on this compound semiconductor are under the materials and hetero structure FETs. So, under the hetero structure FETs. We will talk of the high electron mobility transistors and from hetero structure exploiting the novel materials like using strain and quantization.

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Short Channel Effects in MESFETs

1. Threshold voltage shifts in the negative direction

2. Sub-threshold slope becomes larger.

Both effects are due to 2-D field effect in the channel region. These effects can be reduced by increasing the chann ping density and by reducing the cha thickness

So, we saw that the short channel effects in the MESFETs also come into picture. So, in order to these the short channel effects manifest in terms of the threshold voltage shift in the negative direction also sub threshold slope becomes larger both effects are due to the 2-D effect field effect on the channel region. These effects can be reduced by increasing the channel doping density accompanied by the reducing the channel thickness.

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Need for Hetero junction Transistors

Increasing N_D in the channel adversely affects mobility and velocity overshoot effect in MESFETs.

The High mobility and the high electron concentration can be achieved by separating the donor ions from the region where electrons move.

This is achieved using hetero-junctions and hetero-junction transistors

Now, in fact, increasing the channel doping in the channel adversely affects the mobility as all of us are know it also affects the velocity overshoot effect in the MOSFET; MESFET, this is because the initial velocity will be smaller. So, the overshoot effect will be smaller.

So, the actual benefit that you usually see will get reduced if the doping is high.

So, in order to over these can be overcome these all problem is when it increase the doping the ionized impurity scattering is the one which comes into picture. So, one has to reduce this effect. So, this can be reduced and the high mobility and the high electron concentration can be achieved if we can separate the channel where the electron movement is there separate the channel from the region where the doping concentration is made high.

So, this is achieved using the high using the hetero junction and hetero junction field effect transistors ok.

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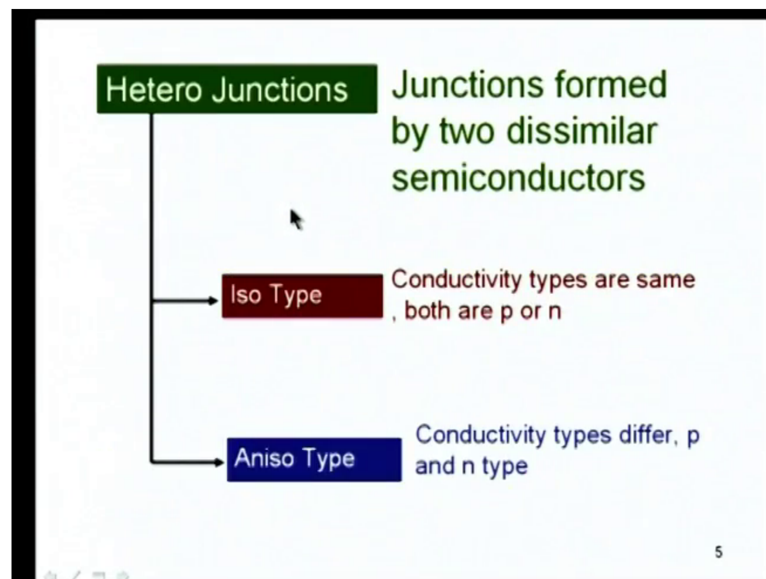

So, we take a look at hetero junctions now because that is the one which we discuss today hetero junctions are formed buy 2 dissimilar semiconductors for example, germanium on silicon that that is a hetero junction gallium arsenide on germanium that is hetero junction. Now there are 2 types normally from we will talk of you can have conductivity or of the same type in the 2 materials.

For example, p type germanium p type silicon p type gallium arsenide p type germanium that is called isotype alternately other name is aniso type which is the common type of hetero junction that you encounter that is one region is p type other type region is n type. For example, you talk of p type gallium arsenide n type aluminium gallium arsenide or aluminium arsenide, ok.

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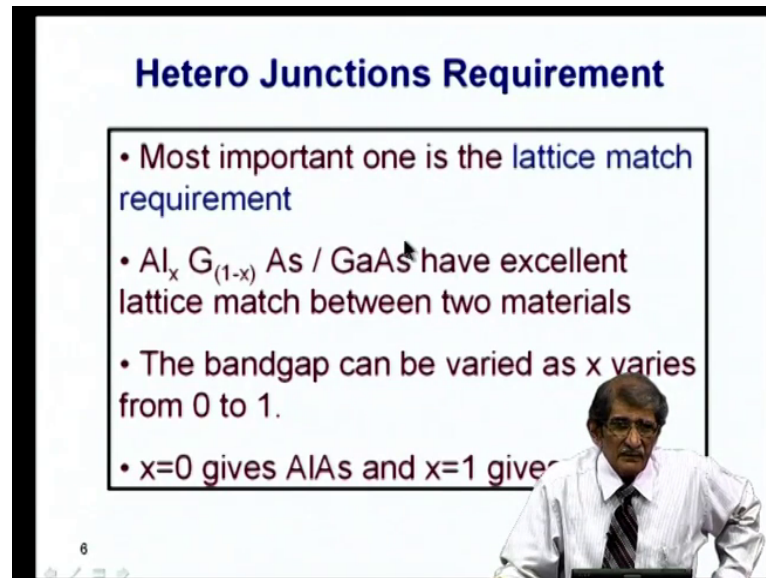

So, hetero junction requirements what are requirements most important requirement is the lattice match requirement when you grow one material on the other there should be very good lattice match between the two. In the sense lattice constant of the 2 materials must be comparable if you are going trying to grow gallium arsenide say trying to grow silicon on germanium there is problem, because the lattice constant are quite different silicon is 5.43 germanium is 5.65, but on the other hand, if I want to grow gallium arsenide on germanium there is no difficulty because both have lattice match.

Now, what we are looking out of for a hetero junction consisting of aluminium gallium arsenide on gallium arsenide aluminium arsenide has got excellent lattice match with gallium arsenide. So, aluminium gallium arsenide also has excellent lattice match with gallium arsenide. So, you can grow AlGaAs aluminium gallium arsenide on gallium arsenide very easily and you can vary this top layer band gap you can vary by varying x equal to 0 to 1 x equal to 0. As I pointed out earlier would mean aluminium component is 0 and gallium is this not g is gallium gallium is 1.

So, you will have AlG; aluminium GaAsx equal to 1, 0 would give you a gallium arsenide and x equal to 1 will give aluminium arsenide. So, you can vary x and very the band gap of the layer which are depositing on gallium arsenide.

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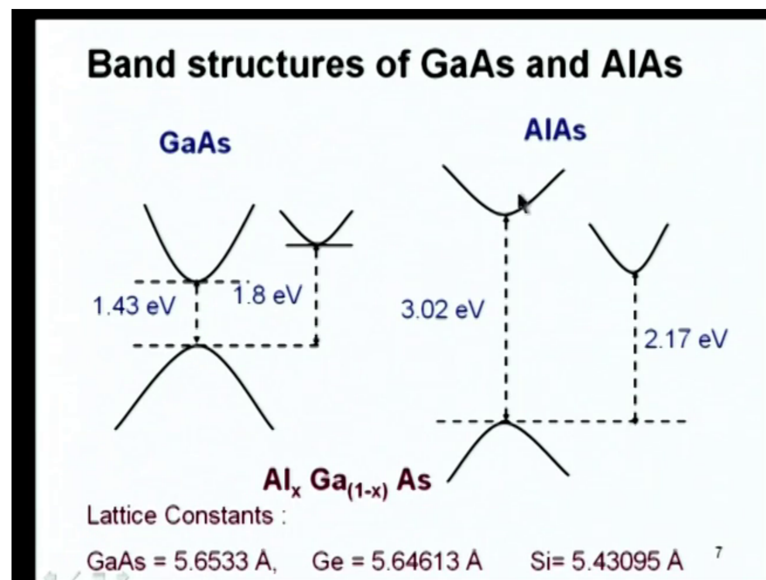

So, take a look at this. If you take a look at the gallium arsenide the lattice constant is 5.6533. Aluminium arsenide also has got very close lattice points many marginals MESFET MESFET pattern. So, you can grow aluminium arsenide directly on gallium arsenide or you can have an alloy of aluminium gallium and arsenide AlGaAs here x equal to 0 that is gallium arsenide that band structure is like this x equal to 1 it is aluminium arsenide band structure is like this.

So, notice this is a direct band gap of semiconductor gallium arsenide that does not matter for us because we are looking of micro microelectronics, it is a direct band gap even up for 12 electrons, it can be used its band gap minimum band gap which is a direct band gap e 1.3 electron volts, but there is also a valley as we pointed out earlier at displace from the central momentum 0 position with their at different momentum you have got a band gap is equal to 1.8.

So, normally the electrons will reside here and the transition will be between these 2 and if the electrons get high energy they can go move into this region at high fields here the MIFET mass is higher. Now, what we are saying is we are trying to use this gallium arsenide. Now if I have an alloy of aluminium gallium arsenide if I vary from x equal to ze 0 to 1 you have 1.43 the direct band gap tracking with this direct band gap of aluminium arsenide. So, the direct band gap will vary from 1.43 to 3.02 and indirect band gap 1.8 will vary from 1.8 to 2.17 linearly, it will vary.

Now just I want to mention also aluminium arsenide is a indirect band gap semiconductor. So, if you change completely from gallium arsenide to aluminium arsenide you will get indirect. So, if you move from gallium arsenide to the aluminium arsenide you will have after certain composition of x you will have direct band gap beyond that you will have indirect band gap, but the point that we are trying to make out do is show is that you can vary the move from the direct band gap to smaller.

So, wider band gap and ultimately it to indirect band gap. So, this is the indirect band gap with band gap 2.17. Let us see how it varies. So, for graph form notice 1.43 will very linearly with 3.02 direct 1.8 will vary with linearly with 2.17.

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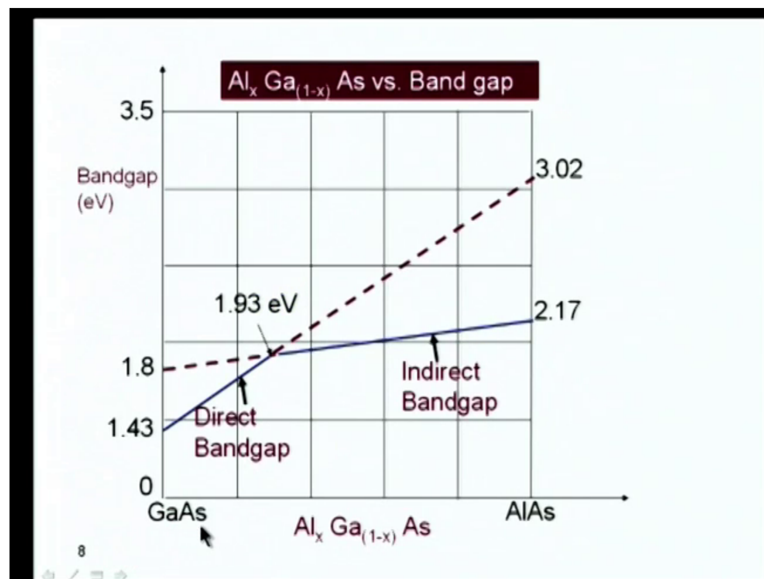

As x is varied from 0 to 1, x is 0 will give gallium arsenide band gap direct is 1.43 indirect is 1.8 as seen here 1.43 1.8 and if you go to this other end x equal to 1 that is aluminium arsenide direct is 3.02 indirect is 2.17 here. So, when you vary the direct component will vary linearly from 1.43 to 3.02 the indirect component will vary from 1.8 to 2.12. Now what happens is this see.

For example here if you see there is direct component indirect component direct compound component is smaller than the indirect. So, actual band gap is this here indirect component is smaller compared to direct component. So, the band gap is actually 2.17. So, lower is the one which gives the band gap. So, as I vary x from 0 to about 0.3 or. so, you will it will be direct band gap semiconductor because direct component is smaller

than one indirect component as you move beyond this composition x greater than about 0.3, 0.2, 0.4, 0.6 like that 0.3 beyond that the direct component is larger than the indirect component.

So, it becomes indirect band gap semiconductor. So, what we are trying to tell is you can grow gallium arsenide or aluminium gallium arsenide on gallium arsenide and the composition of the AlGaAs depending upon x you can have direct or indirect, but the band gap always we can get higher than that of gallium arsenide. So, you get a good hetero junction here.

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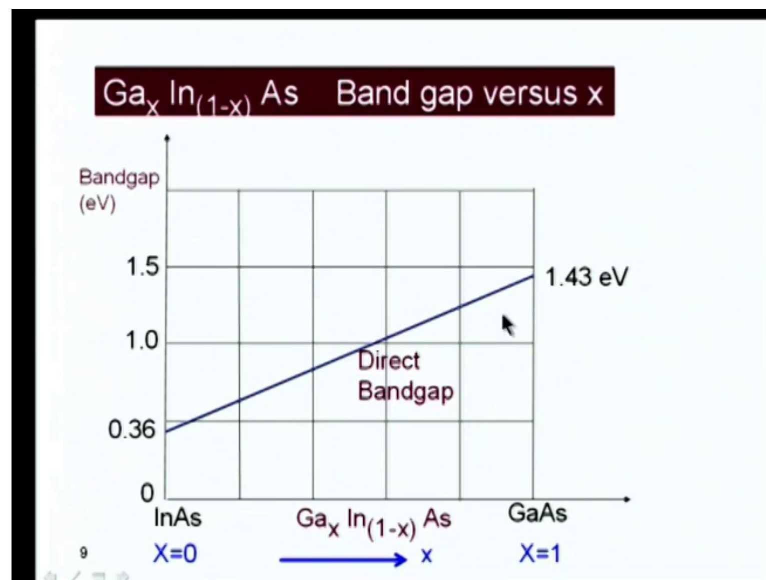

If you want to look at other materials like indium phosphide or gallium indium arsenide you can mix gallium arsenide with indium arsenide and make a compound gallium indium arsenide for example, here x equal to 0 will give you indium arsenide x equal to 0 band gap is direct band gap 0.36 and gallium arsenide also is in the is a direct band gap that is x equal to 1 this component is 0 gallium arsenide is 1.43. So, both end the steam ends you have got direct band gap. So, I can have gallium indium arsenide throughout a direct band gap material why do we talk of that mobility of indium arsenide is very high.

So, gallium indium arsenide mobility will be higher than that of gallium arsenide you can have band gap somewhere in between for example, if I have something like 0.4 or 0.5 you will have band gap which varies very close to 1.

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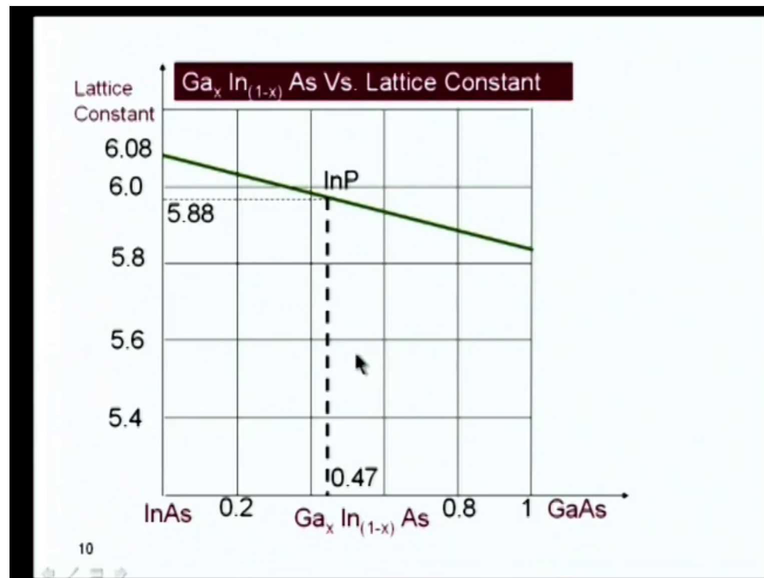

So, why we talk of gallium indium arsenide you can make hetero junction with gallium indium arsenide on indium phosphide, because when x equal to 0.47 gallium 0.47 indium p 0.53, the lattice constant is 5.88 angstroms which matches with the indium phosphide.

We can grow gallium indium arsenide or indium phosp on indium phosphide make high mobility transistors using that we will today focus on the AlGaAs type aluminium gallium arsenide gallium arsenide.

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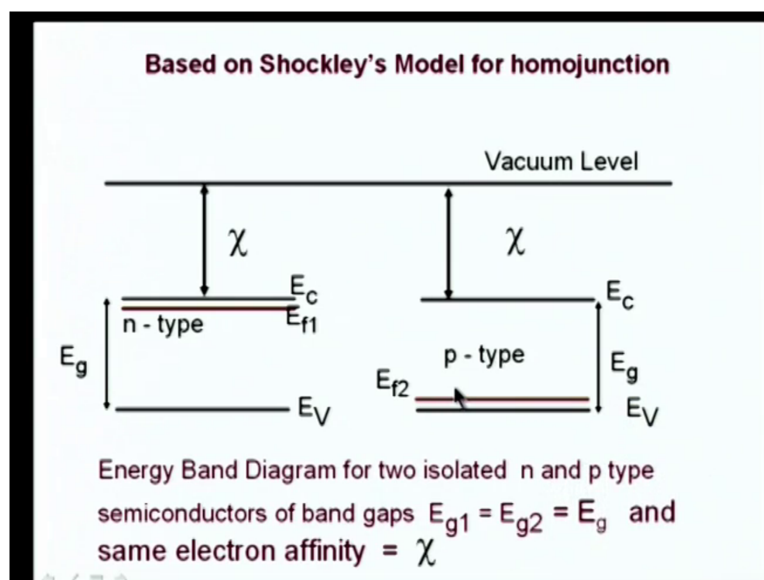

So, what is the hetero? Hetero junction, if I take a look at the homo junction; for

example, if I talk of silicon; silicon n type material, p type material; when you talk of the same material band gap of material, one is the same as the band gap of material 2 the electron affinity that is the energy gap between the vacuum level and the conduction band E c chi is the same in both cases silicon is 4.05.

Now if I take Fermi n type Fermi level is very close to conduction band and the Fermi level here is close to valence band when you put them together you can see that if you put them together the Fermi level here is higher than Fermi level here. Therefore, the in the system from the theory of Shockley model, we know that you when you form a junction electron from this le region where electron concentration is high will flow to this p region which would actually deplete the region on the surface. And you will have a band bending upwards here and from here the holes from this side will move from left to right depleting this, when this depleting band will move down here.

In fact, you can just quickly see else see where I can show that to you see for example, if you see the when you form the energy band diagram.

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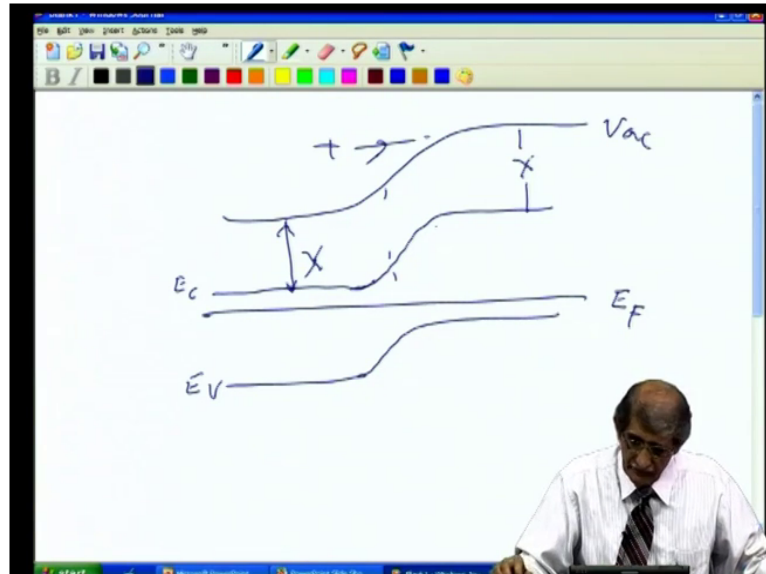

The; you know that Fermi level is slat and in n type, it will Fermi level is here well no conduction band and valence band and because of the band depletion layer it will go like that. So, this is a conduction band this is the valence band correspondingly the 0 level whatever chi was there it will be there that is the vacuum level. So, that is chi and this is also chi

So, you get same chi, so, there is no dis continuity discontinuity in the energy band diagram. So, notice somewhere here the region joint bends up that bends down. So, the electric field at because this is depleted the electric field is like that negative charges here plus charges here this is a standard theory of homo junction homo junction means band gaps are same chi is the same, there is a continuity everywhere vacuum level represents the change in the potential and with respect to vacuum level the conduction band will be located; so, will go back to our theory of the hetero junction. So, same thing holds good to the case of hetero junction here.

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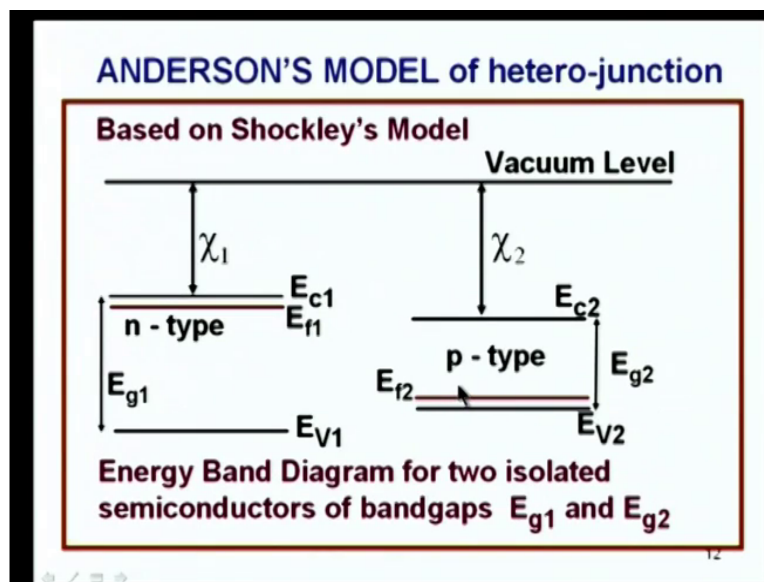

We are talking of a band gap which is wider compared to wider band gap E g 1 compared to another band gap narrower band gap two. So, the Fermi level is higher here compared to this.

So, when you join them and here one more thing is chi 1 that is the energy difference between the vacuum level and the conduction band chi 1 is smaller than chi 2 this is the basic Anderson's theory of model this model holds good up to certainly you to understand, but actually there is more much more than that what is say happens. So, let us straight understand it what happens in energy band diagram when you join them together energy band diagram bends up here exactly the same way as you sow here the energy band energy band diagram bends here its bends up here on this side and it continues to bend up because this bends up that is bends down. Now let us go back here. So, when you put them together because electrons get transferred here this will be depleted actually

holes are transferred.

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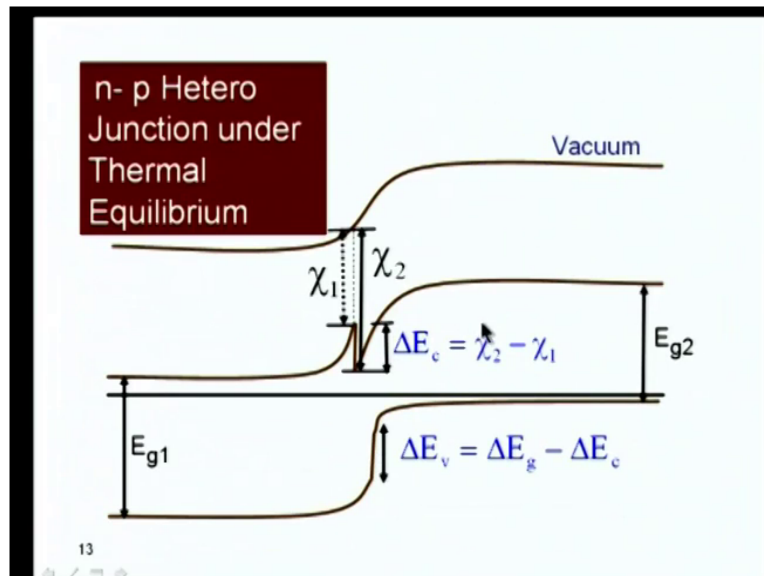

So, this will be depleted. So, what you will get will be a vacuum level, there will be plus potential here minus potential here. So, the vacuum level will bend exactly same way as a happen in the homo junction because the energy band at the vacuum level does not have any discontinuity it represents the way the potential varies.

So, that is continuity if you take a look at the conduction band in the n type material wider band gap material it has depleted and bend up all through here chi 1 is the vacuum level chi 1 is the electron affinity here same thing is here, but when you come from that side vacuum level bends down here, because of potential variation like that plus here minus there. So, the conduction band also bends up down like this till they come to the junction now you can see at the junction all through here this chi 2 from the top to bottom is chi 2 and when you come here the gap between the vacuum level and the conduction band in the p type material is chi 2 where is at the same point the joining point of the n type material which is wider band gap there the chi 2 is the electron affinity is chi 1 chi 1 is less than chi 2. So, these 2 conduction bands do not meet at the same time there is a certain discontinuity here discontinuity here that is the specialty of the hetero structure the energy band diagrams are not continuous there is a notch here.

So, if there is a notch here it is almost like the notch that is you see in the MOSFET. So, if they are electron some. So, on this side if the electrons are injected on to this side they

will get collected here and those electrons cannot cross up this barrier they will get they remain there it is like what you have in the case of the I am sorry; oh this is similar to what we have in the case of the MOSFET see for example, in the case of MOSFET you should recall what you have is the oxide; oxide is there ok.

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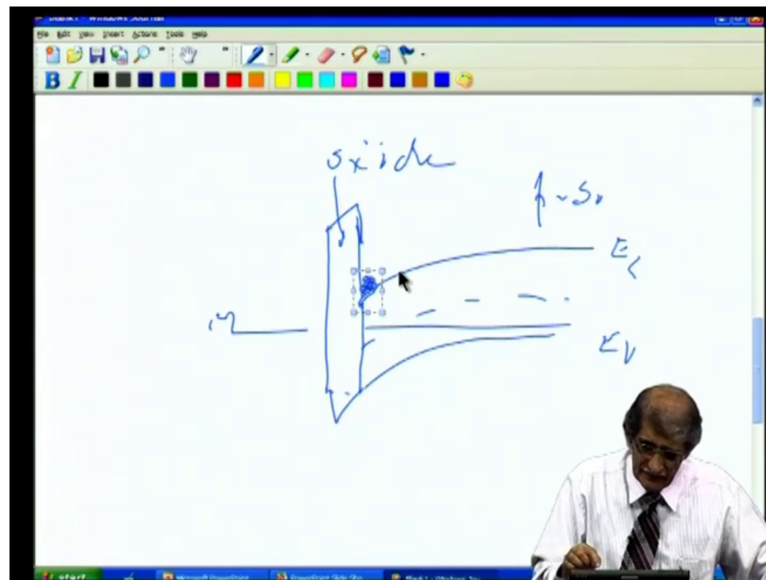

That is like that then if you have p type semiconductor you have got the Fermi level like this then you have got like this conduction band E c and E v and you have like this oxide this is oxide and this is a p silicon and you have the metal. Now, you can see there is high band gap here about 3 0.3 electron volts is there.

So, when its inverted here the electrons get lock down knocked here electrons remain here they cannot go up that is why you will have to go when they invert it, here when it has become n type you have got electrons locked in the notch. So, whenever there is a notch like this there is a barrier height like this there will be electrons collector there you can make use of that as the channel if I connect the 2 ends of this channel by source and drain we can make a MOSFET. So, exactly same notice the similar type of notch is there in the case of hetero junction that is this you have got this bending here there is a notch here.

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Experimental Results on $Al_xGa_{(1-x)}As/GaAs$

$$\frac{\Delta E_C}{\Delta E_g} = 0.6 \text{ to } 0.64$$

$$\Delta E_g = 0.5\text{eV when } x = 0.4$$

$$\Delta E_C \approx 0.64 \times \Delta E_g = 0.32\text{eV}$$

This value is different from $(\chi_2 - \chi_1)$

$$\Delta E_V ;\ 0.47\, x(Al) = 0.18\text{eV for } x = 0.4$$

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So, the band bending is actually such that; so, much that there are electrons collected here. So, now, what you can do will be I before you go into the structure, I just give what will be the value of this. So, this notch is actually equal to you can see that is chi 1 minus or chi 2 minus chi 1 that is a first order theory and that is delta E c is the discontinuity in the conduction band and if the band gap E g 1 is larger than E g 2 this is actually E g 1. So, E g 2 will be E g 1 plus delta E c plus delta E v therefore, delta E v there is a discontinuity here also discontinuity will be delta E g minus delta Ec.

So, what we are trying to say is this is first order theory, but in practice here it looks as if delta E c is chi 2 minus chi 1, but even in materials which there is chi 2 minus chi 1 is not that much you see a difference and that is governed by how much is the band gap difference between the two. So, the delta is ultimately is related to E g 1 minus E 2 that is delta E g.

So, it is seen that experimentally that delta E c by delta E g is about 0.6 to 0.644 AlGaAs gas system AlGaAs is aluminium gallium arsenide. So, delta E g for x equal to 0.4 from this particular thing over x equal to 0.4 delta E g is something like 1.43 plus 0.5. So, delta E g is 0.5. So, if delta E g is 0.5 delta E c is 0.5 plus 0.64 is 0.32. So, you will have delta E c of 0.32 electron volts if the band gap of this region is 0.5 E g 2 plus 0.5 electron volts in the AlGaAs you can get that the value difference. Now if delta E c is 0.32 electron volts and if delta E g is 0.5 delta E v see if this is point delta E g is 0.5 delta E c 0.32 this will be 0.18 that is what you put here ok.

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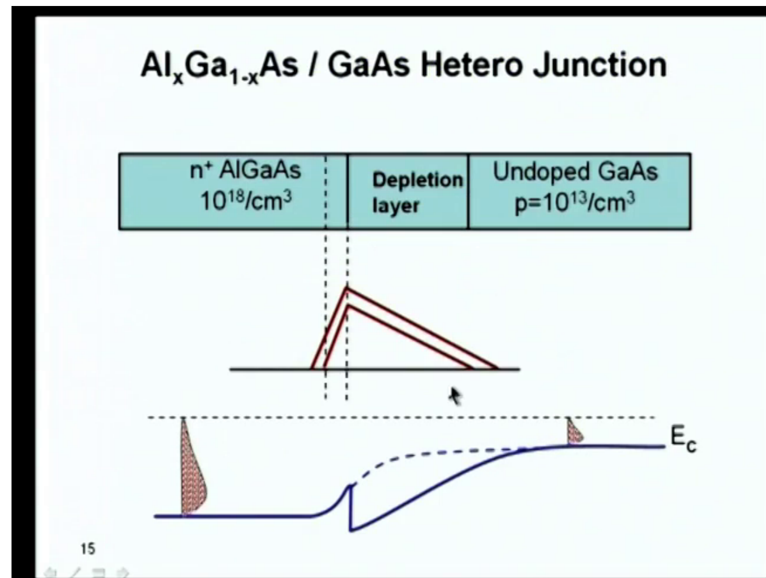

So, what you have is now AlGaAs gas system which can be used as a gate you can have the channel here this region can be used as channel this is un-doped which actually turns out to be very lightly doped 10 to the power of 13 and there is a depletion layer here we saw the p region is depleted and there will be small depletion layer in the n plus aluminium gallium arsenide also this is electric field distribution here.

So, what you will have will be if I do not have any gate connected put here this region is not depleted. So, conduction band goes like this gets depleted then because of this work function chi difference etcetera and delta g difference its nerf down here by delta E c 0.3 naught 0.32, then it rises up, because there is a depletion layer here electric field is in that direction. Therefore, the conduction band will rise up here the point that you have to note down here is that in the case of conventional junction there is no delta Ec. So, this would have gone up like that straight away like this, but in this case because of this delta E c they start from the lower end then the track raise up to the same amount so that the electron distribution here and here matched together.

In other words you will have a total potential drop across this which is some of the which is more than the conventional built in voltage of the MOSFET or the pn junction and the delta E c delta E c by q. So, what we are telling is I can actually have a transistor made by this this is a gate region this is a channel region n plus region over that.

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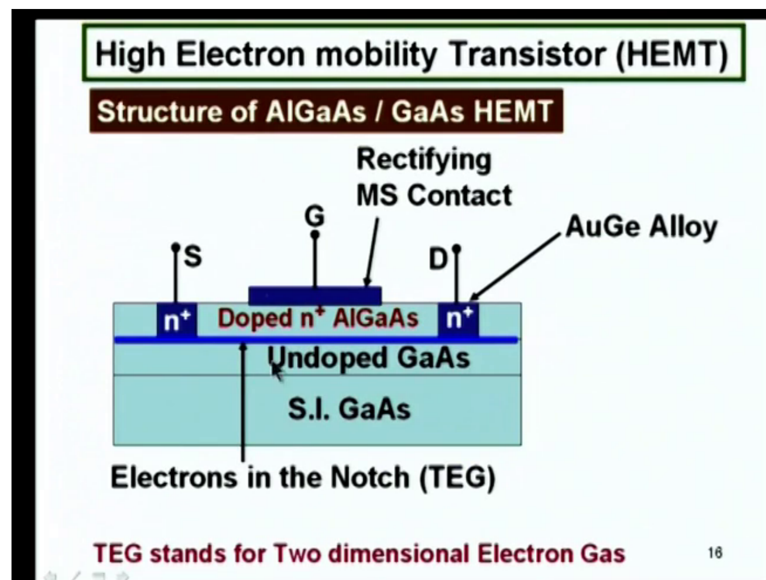

Doped gallium arsenide channel region n plus aluminium gallium arsenide over that rectifying contact; so, if I do not have a rectifying contact what will happen will the.

So, we have also source and drain region that is heavily doped n plus region which is usually realized by gild germanium alloying on to this region it goes through that. So, because of the AlGaAs gas structure you have that notch here and electrons are present here throughout this region, if the electrons are present here throughout the region if I have n plus region here and n plus region here when I apply voltage between the drain this we can call it as drain and the source when I apply voltage the electrons there is electric field from here to here. Therefore, electrons will be injected from here to the channel they will be collected here.

There will be current flow, but now if I do not have the gate you saw when you did not have the gate there is a channel here, but this there is a region which is not depleted. So, if I have a ca source drain connected like this realized like this not only there be current flow through this particular layer there will also be current flow through this heavily doped n plus layer inside.

In fact, the entire current will be masked or controlled by the current flow through this heavily doped region if it is current flow through the heavily doped region the mobility will be very low there is no use. So, what you do is put a metal gate here. So, the metal gate here you can the work function will be such that you can either deplete it completely

or if it is not depleting completely you can apply a negative voltage and deplete it.

So, in from the MESFET theory we know that the voltage required to deplete the entire n plus layer is called the pinch off voltage, voltage off, voltage, voltage Vp 0. Now the voltage if the pinch off voltage if the depletion built in voltage is different from the pinch off voltage if you lower than that you have to apply gate voltage which is equal to V bi minus Vp 0. We saw it in the MESFET theory threshold voltage of the MESFET is V bi minus Vp 0; that means, it is a gate voltage that must apply to pinch of the channel ok.

So, we can apply V bi minus V chi Vp 0 that is actually the point at which the channel will be conducting will a current flow now let us go further on that. So, the work function of the gate is to dip totally deplete the n plus layer it also does the job of controlling the charge in this particular region we can see once it is fully depleted it is like a MOSFET metal insulating layer and the channel where inversion layer is there. So, by applying voltage to the gate I can control the channel charge here. So, you can have right equations exactly similar to the MOSFET.

Where we have mu c oxide W by 12 into VGS minus V threshold, but if V threshold will be different from that of the MOSFET and MESFET will see what it is that is. So, in one way it looks like a mo MESFET, because they say short key barrier otherwise it looks like a MOSKET MOSFET because this metal depleted layer and the channel.

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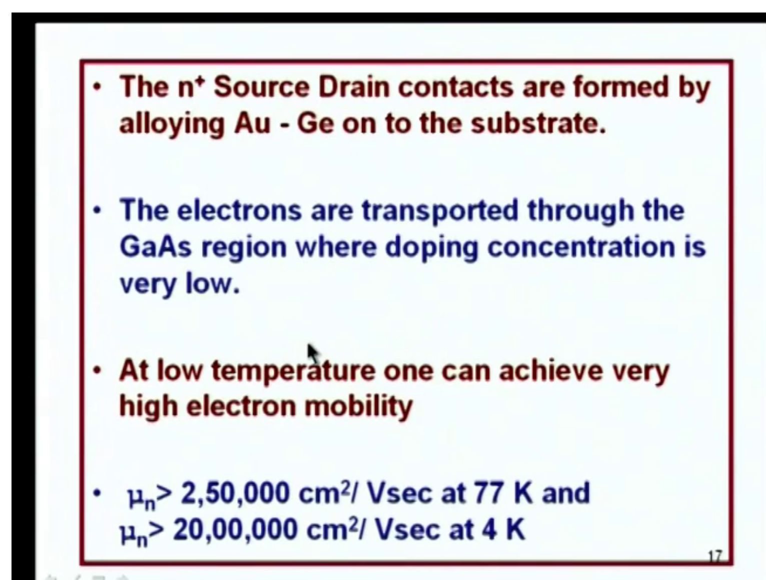

The n plus source drain contacts are formed by alloying this they will transfer transferred

through the gallium arsenide region where the doping concentration is very low since the doping concentration is very low the ionized impurity scattering is absent. Therefore, you get very high mobilities, you get mobilities as high as ideal 8500 centimeter square per volt second at room temperature you reduce the temperature to 77 Kelvin you get 250000 centimeter square per volts sec.

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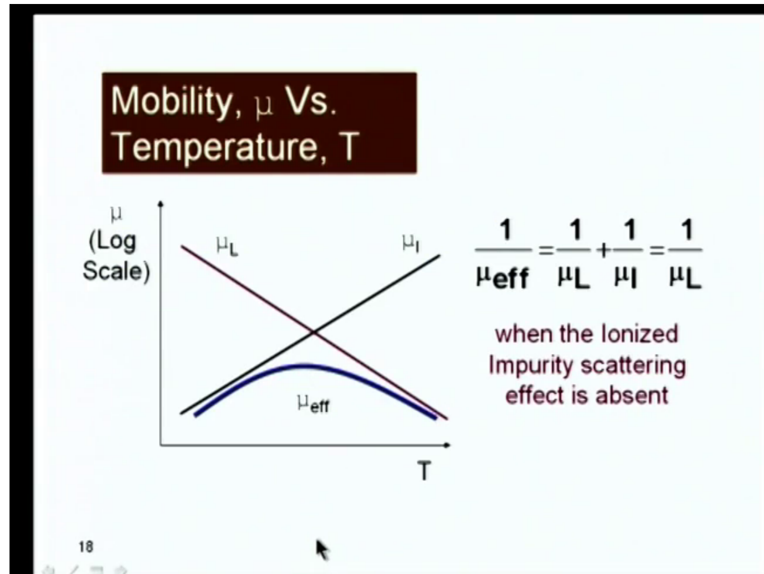

These are reported values in literature you go down, even down, you will get much higher mobility what is the due to you can see a mobility effective mobility depends upon the lattice scattering mobility as the temperature goes up lattice scattering mobility goes down mobility governed by lattice, because lattice vibrations increase if lattice vibrations inc increase the scattering of the electrons by the lattice atoms increases. Therefore, mobility goes down ionized impurity scattering when they go to lower temperature the ionized impurity scattering increases. Therefore, the ng ionities the scattering decided by the impurities increases therefore, mobility governed by the ionized impurity scattering goes down.

That is because when you go down to low temperature the velocities of the electrons re lower. So, therefore, if there is an ion present the electron actually will move very close to as it goes to the close to the atom the impurity if it close; close to the impurity, it gets deflected by the electrostatic force if the velocity is lower it gets deflected more towards this if electron gets it gets more towards this ion when it moves like that if the velocity is high it chance of deflection is less because it slips through that layer very fast. So, when

they go to lower temperatures velocities are lower.

So, scattering probabilities is also higher therefore, mobility falls now the combined effect of that is one by mu lattice plus one by mu i. So, that is this combined effect if the doping concentration is high; you can see you maybe if you reduce the temperature mobility will reduce drastically, but if the doping is 0 very little this component is 0. So, only this particular component is there mu L is there. Therefore, what you will have will be the what you will have in that case will be like this what you will have will be the temperature verses mobility will be like that.

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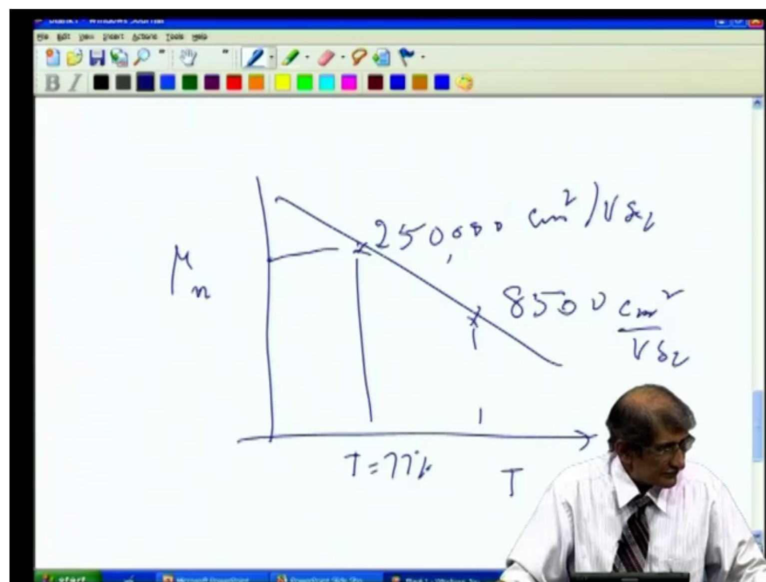

So, room temperature you may have about 8500 centimetre square per volt second as you go to lower temperature t equal to 77 degrees Kelvin you will have 250000 centimeter square per volt second. So, you will have get very high mobility because other component you have eliminated by removing the dopands. So, that is about that.

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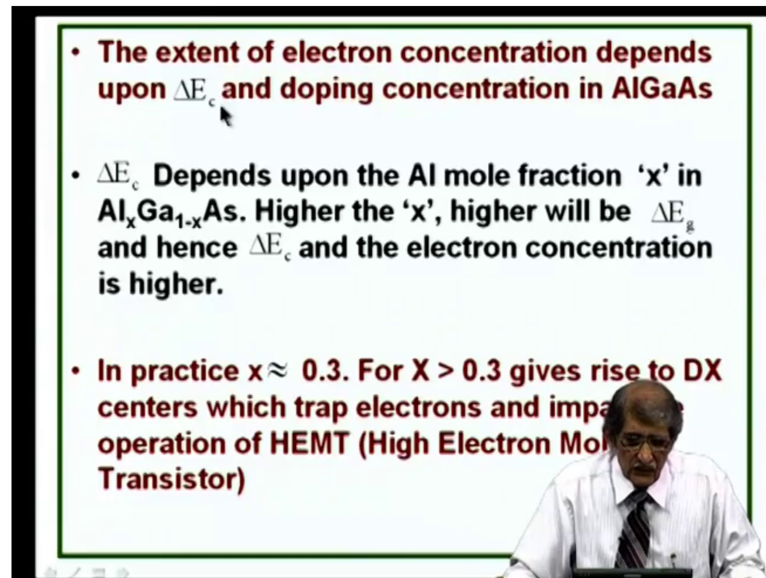

So, the extent of electron concentration depends upon delta E c because higher the notch higher the notch more chances of the having the electrons more chance of bending here therefore, more electrons will be present. So, the delta E c if its higher you will get more electrons, but be more current flow for a given voltage. Now delta E c depends upon mole fraction because delta E c depends upon delta E g delta E g depends upon how much is the band gap of AlGaAs higher than that of gallium arsenide, how much higher the electron con aluminium concentration higher will be the band gap there higher will be the delta E g and higher will be the delta E c. In practice you do not choose very high aluminium concentration because the aluminium itself is unstable it gets oxidized etcetera and also it gives rise to trap centers and it effects the mobility.

So, highest value of x that you choose is about 0.3 aluminium concentration which will give about 1.9 electron volts as the band gap.

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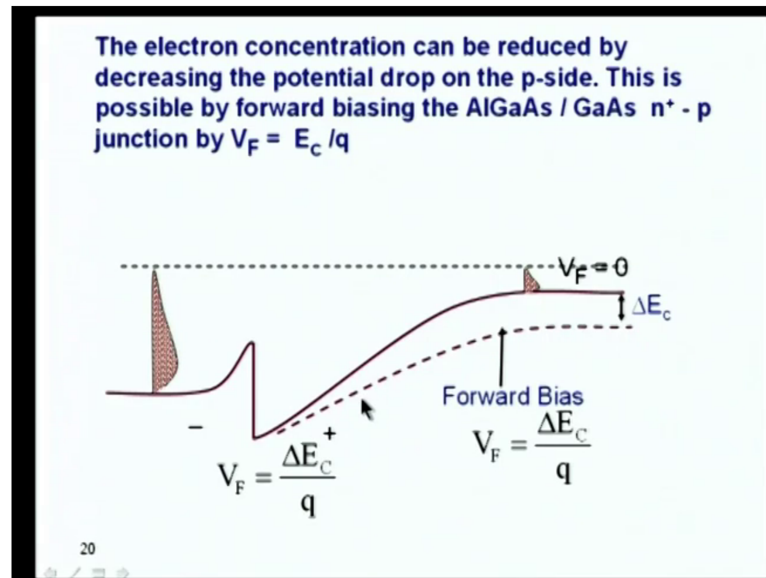

So, now one of the things that you want to see is when you deplete the whole this top channel completely because there was already this particular delta E c was present there will be charges how to turn off the device what will be the voltage that you must apply to the device to turn it off that is actually the threshold voltage. So, this was the diagram that we have drawn conduction band. Now you have got you have to apply voltage equal to V bi minus Vp 0 to deplete this region that if from the gate side. Now in thermal equilibrium, you have got both the electron distributions here; here is very little because it is undoped here it is high from they saw theory of junction and Schottky barrier you know that the thermal equilibrium transform electrons from here to here will be 0.

Now there are electrons here because of this high band bending in the conventional homo-junction there are no electrons there at that point there is no because there is no notch now the band bending is more than that in the conventional junctions by an amount equal to delta E c and because of the delta E c more band bending is there when you have that particular thing you have this thermal equilibrium achieved because band bending is more than that of in the conventional junction you will have virtually like an inversion layer here now to remove the inversion layer here you must reduce the band bending by whatever extra amount of delta E c by q is there you must reduce. So, the amount that you must reduce that band bending is actually delta E c by q.

So, the polarity of this voltage drop across this layer is plus here minus here if I want to reduce that voltage by delta E c by q that is VF I must apply voltage plus on the right

hand side and minus on left hand side p is net plus with respect to n. That means, you must have a forward bias to the junction. So, that the barrier height is reduced by delta E c which is delta E c by q. So, what we are telling is if I have this MESFET.

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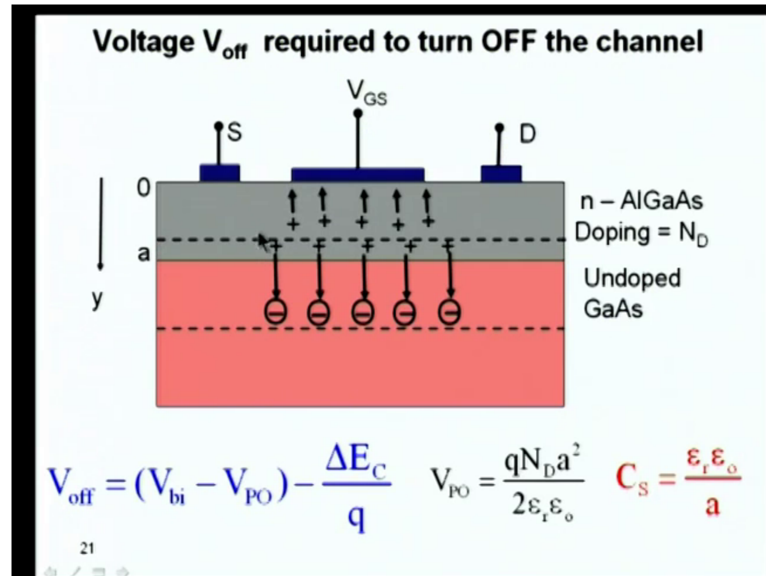

I apply V bi minus Vp 0 the whole thing will be depleted, but across this layer there is built in field there is are electrons here to remove the electron I must apply plus here minus here. So, V bi minus Vp 0 is actually negative total potential plus here ma because the charges are plus here donors donors are these are the donors plus here minus here. So, electric field is towards the gate here, but AlGaAs to the semiconductor this is np field is like this there is 0 field here the depletion layers meet here, but there is also there are electrons here.

If I just deplete it come up to this point there are electrons here on the interface. Now to remove those electrons I must reduce this barrier I must apply plus here minus here or in other words once it is depleted completely if I increase the voltage by another another term or a by an value equal to delta E c by q say make this more negative whole thing is depleted. So, there is this depletion layer actually will slightly fall because this gets forward biased. So, what you do is at a voltage equal to minus to this point this is already depleted. So, that minus delta E c by q that you apply here goes across this junction minus here plus here which is actually equivalent of forward biasing this which removes which reduces the barrier. So, electrons from here are actually removed. In fact, they are taken to the gate.

So, when you do that when you apply more negative voltages whatever see there is a connection between this source and this particular channel if you take a look at this here when I apply a negative voltage to this after this depletion if I increase further the negative charge is transferred from the channel through this to this gate to transfer this voltage completely from here to here the voltage additional voltage at must apply delta E c by q once I apply more delta minus delta E c by q after depleting the whole thing I apply additional minus delta E c by q all the electrons would be transferred from here to here that is what is happening here.

So, if I apply a voltage V of equal to V bi minus Vp 0 required to delete this and delta E c by q required to remove the electrons from here back into this the channel width and all that will be actually the threshold voltage we call it we do not call it threshold voltage here by convention they call it as the gate voltage that must be apply. So, that turns off the hemt.

So, here the V off can be positive or negative depending upon what is this value delta E c by q. Let us say it is what we said is it will be something like 0.3 delta E c 0.3 electron volts. So, this quantity will be 0.3 volts. Now I can adjust the doping and adjust Vp to 0 depending upon the doping or depending upon the barrier height I have between the short key and the aluminium gallium arsenide you have got V bi I can adjust the doping and the thickness. So, that V bi minus Vp 0 is more than 0.3 volts if V bi minus Vp 0 is more than 0.3 volts is because this is 0.3 volts V off will be po positive. So, I can have V off either positive or negative supposing this term this is negative supposing this term is minus 0.1 volts this is 0.1 minus 0.3 volts you will have V off is minus 0.4 volts. So, you can have enhancement or depletion type of high electron mobility transistors using this HEMT structure ok.

So, the doping you remember you are not adjusting the doping here its undoped all the doping that you are talking of is doping in this particular layer AlGaAs layer. So, increasing the doping is not effecting the mobility of electrons here it is only adjusting the threshold voltage. So, you can have independent control of threshold voltage without effecting the doping here you can adjust the thickness here and the thickness controls the capacitance as I pointed out the working of this is now once this is depleted the gate gets coupled on to this channel here. So, you can talk of right equations similar to that of MOSFET.

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I_D Vs. V_{GS} Characteristics

Same as the MESFET

$$I_D = \frac{\mu_n C_S W}{2L}(V_{GS} - V_{OFF})^2$$

$$g_m = \frac{\mu_n C_S W}{L}(V_{GS} - V_{OFF})$$

$$V_{off} = (V_{bi} - V_{PO}) - \frac{\Delta E_C}{q} \qquad C_S = \frac{\varepsilon_r \varepsilon_o}{a}$$

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And the ID VD gas characteristics transfer characteristics are be ID is equal to in the case of MOSFET mu n Cs W by 2 L into VGS minus V threshold square here instead of V threshold we have V off given by this term negative or positive negative means depletion or type positive means enhancement type and Cs in the case of MESFET it is a channel thickness in the case of MOSFET.

It is oxide capacitance in the case of MESFET it is channel capacitance that is this quantity. So, in the case of me MOS mod effect I am sorry, high hemt; HEMT is also called mod effect that is modulation doped FET mod effect mod effect HEMT all are same. So, in the case of mod effect or HEMT Cs is you can increase the CFS by reducing the thickness of that layer that is that layer, but then to adjust the threshold to adjust the V off you must actually increase the Vp 0.

If you want to increase keep that when you reduce that you must increase it to adjust the dopping to keep the Vp 0 same when you reduce a you must increase nd. So, there is no upper limit to ND because as you go to higher and higher doping concentration the metal semiconductor contact will not no long be rectifying it will become ohmic contact because of tunneling current between the small depletion layer found between the ND and this quantity. So, upper limit on the doping the doping on that controls the doping on this layer. So, there is a lower limit on a that you can choose.

You may use something like a few nano meters 100 nano meters of that order we can

choose 0.1 micro meter or even slightly lower.

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$$V_{off} = (V_{bi} - V_{PO}) - \frac{\Delta E_C}{q} \qquad V_{PO} = \frac{qN_D a^2}{2\varepsilon_r \varepsilon_o}$$

Enhancement and Depletion Mode type of devices are made by adjusting V_{po}

- Reduce "a", V_{po} goes down and V_{OFF} can be made positive.
- g_m can be increased by reducing "a" $C_S = \frac{\varepsilon_r \varepsilon_o}{a}$
  - This can be done by increasing N_D for V_{OFF} adjustment.
  - Upper limit on $N_D = 10^{18} / cm^3$ decided by the schottky barrier gate.
- Spacer layer = 20Å is added to improve μ_n

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Because the upper level on doping concentration is something like 10 to the power eighteen that you can do because of the limitation of the Schottky barrier dope. So, enhancement and depletion more types can be made with by adjusting Vp 0 by adjusting that you can get this positive or negative you can reduce a then Vp 0 goes down V off can be made positive by you reducing that now gm can be increased by as I pointed out gm can be increased by reducing the channel thickness this can be done by increasing the doping or the V off adjust V off adjustment upper limit on ND is 10 to the power eighteen. So, that limits how much low we can to here.

So, what we are pointing out is you are able to increase the doping here in the aluminium gallium arsenide layer without increasing the doping in the region where the electrons are flowing all that you are doing is tailoring the doping at thickness in the other wider band gap material where the electrons are not following you can tailor that tailor the threshold voltage and substrate is un doped mobility is high. So, you get very good characteristics now here also I am sorry just here also what you do is in addition to this AlGaAs doped layer when you do that you all usually.

In fact, is put a thin layer of un doped aluminium gallium arsenide just about 1 or 2 nano meters that is because, if the whole thing will is doped the entire layer up to this channel is aluminium gallium arsenide heavily doped. Then these electrons which are moving on the

channel see the effect of the doped layer some scattering is there to overcome that you put a thin layer of AlGaAs here. In fact, the optimization of that layer also is involve 3 trans conductance adjustment ok.

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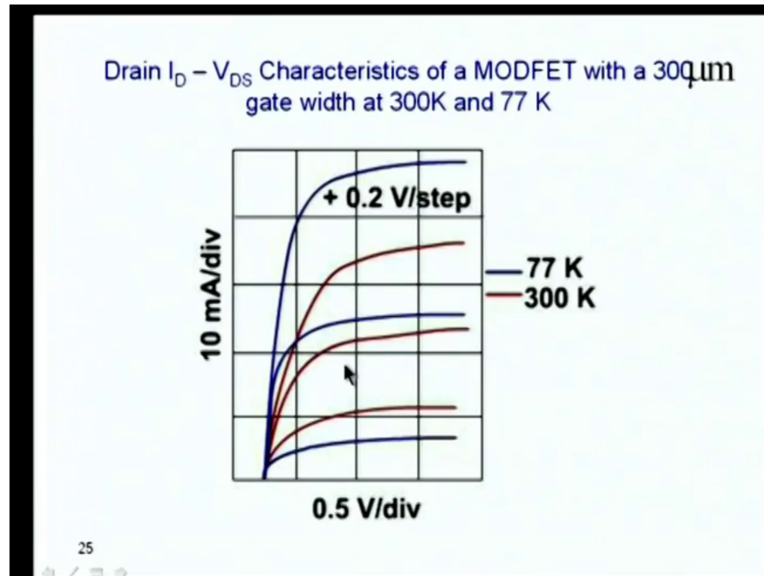

Now, quickly run through the thing the characteristics this is just to show you that people have made this type of devices at 300 degrees Kelvin the transfer character.

The output characteristics ID verses VDS you can see it saturates like this red curve is the 0.2, 0.4, 0.6 gate voltage and as VDS is varied from 0.511, 0.52 volts low voltage current 10, 20, 40, 60 milli amperes per division here the most important thing the we note is the current here current here at this gate voltage at 300 degree Kelvin is something like 0.2, 0.4, oh, 10, 20, 30, 35 milli amperes whereas, here it is 40 to 50 milli amperes 10, 20, 30, 44, 35, 40 and 45. So, above 10 milli amperes higher much higher current you get lower temperature this is because of the mobility notice also the current rises deeply here in the linear region, because the mobility is high they conduct tunnel conductance is high.

Therefore, the current rises deeply the on the resistance of this high electron mobility transistor is very low compared to the on resistance of the same at room temperature by lowering temperature mobility is increased and the on resistance is reduced very good for digital application in digital applications you want very low on resistance ok.

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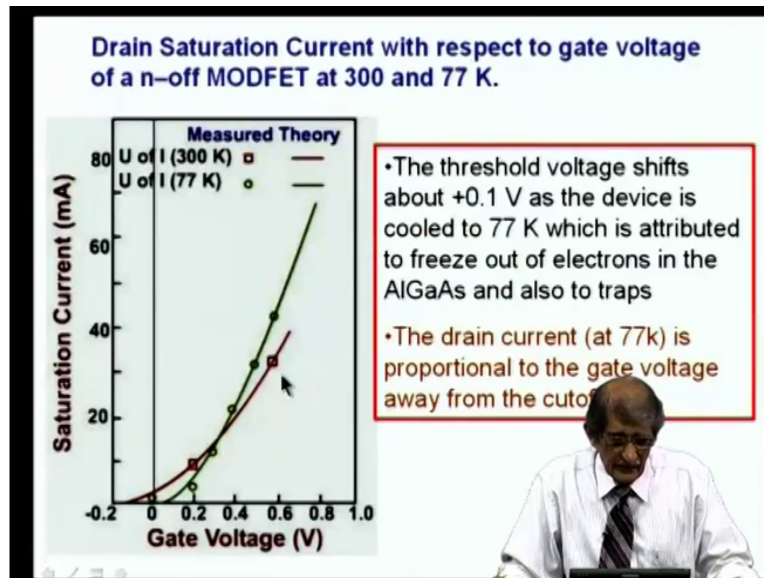

This is the saturation current ID versus with transfer characteristics in the linear region you can see that the there is a crossing over and the current. Current rises steeply at lower temperature, because improved mobility also notice that there is a threshold voltage increase when you go to lower temperature this is attributed to the freezing of electrons in aluminium gallium arsenide layer. Therefore, you must apply more voltage I am not gain going down to details of that this is the trans conductance this is the saturation ID versus VGS trans conductance.

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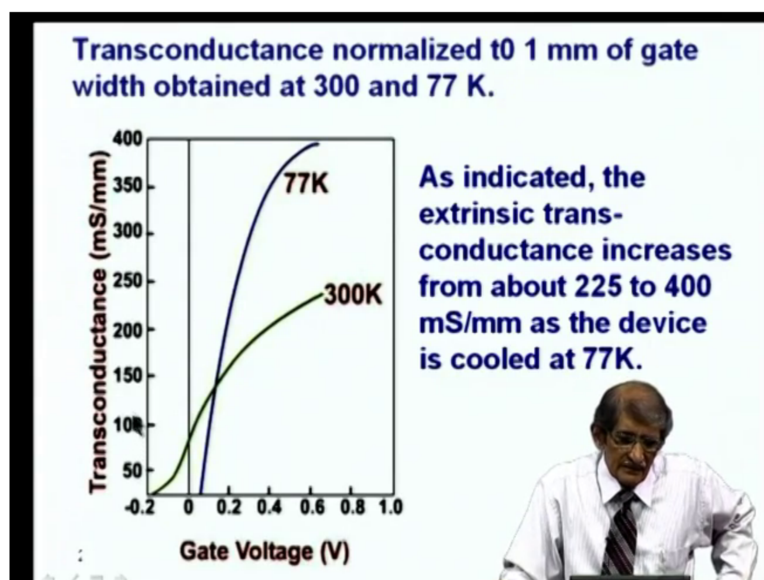

You can see you can see the trans conductance is very steeply rising in the gate voltage you get trans conductance increases from about 225 milli ampere per volt.

225 milli amper per volt here to about 400 milli amper per volt at this 0.5 volt 0.5 volts it is the trans conductance is much much higher because the trans conductance depends upon mo mobility trans conductance on resistance everything improves, because of the mobility go to lower temperature you get higher mobility higher trans conductance by big factor. In fact, such high trans conductance also to tells you it is not due to velocity saturation it is due to the velocity overshoot effect it if at all inefficient because of the high mobility.

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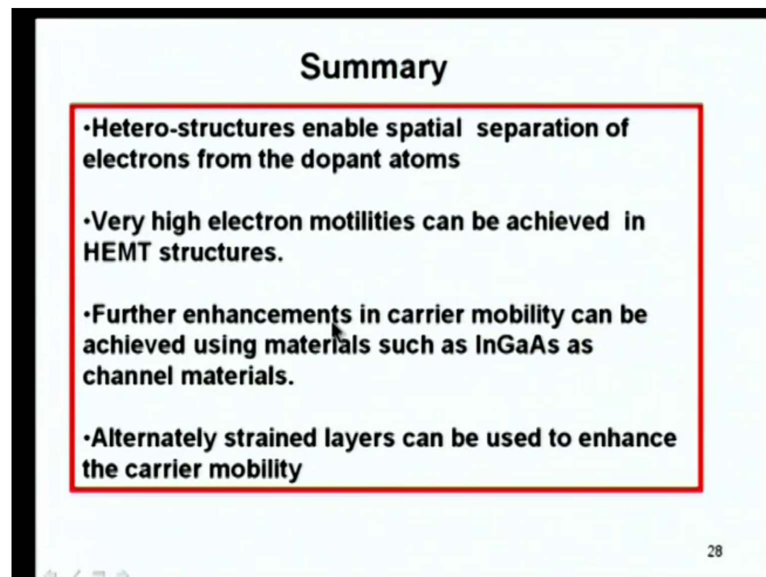

In summary of first part of this a few more things I will discuss hetero structure enables spatial separation of electrons from the dopant electrons atoms. Very high mobility you can be attained enhancement of carrier mobility can be further enhancement can be achieved using materials such as indium gallium arsenide as channel materials; what we are using is gallium arsenide room temperature mobility is about 8500, but if you go to indium gallium arsenide you can get much higher mobilities at least 2 to 3 times more than mobility than this at even room temperature. Alternately you can use strained layers ok.

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Impact of Strain on the mobility of holes and electrons in silicon

- Longitudinal tensile Strain along the MOSFET channel improves the electron mobility and reduces the hole mobility
- Longitudinal compressive strain increases hole mobility and reduces the electron mobility

- In P-Channel Si MOSFETs when the source and drain regions are formed using SiGe, the channel is in compressive stress – increases μ_p.
- In N-Channel MOSFET electron mobility is improved by a top layer of nitride which introduces tensile stress

Let us see what is that if the region where the this is in addition to this HEMT etcetera even if you use conventional MOSFETs you can go to use silicon itself and subject the strain silicon to strain if you have longitudinal tensile strain that is if I have tensile strain along the length of the channel it is stretched the then the electron mobility improves stretch it along the length of the channel electron mobility improves. So, N channel devices you can actually stretch it by depositing elec silicon nitride on the top of the finished device that gives you raise to tensile stress which touches the channel along the channel length which actually increases the electron mobility with P the Intel people have tried this out therefore, it fine; now at the same token if there is a P channel device.

If I stretch it along the channel by tensile stress the mobility goes down, I will not get it down to the physics of that due to time, I will just now discuss it at this moment. So, it goes down, but if you compress it; if I subject the channel to compressive stress, then the whole mobility goes up. So, the moral of the story is if I have N channel transistors that region you compress subjected to longitudinal tensile stress along the channel by putting silicon nitride in the top of that channel of the gate you can increase the electron mobility of the N channel device where ever you have P channel devices you subject the channel to compressive stress; how do you compress it between the source and drain; for example, between the source and drain see for example.

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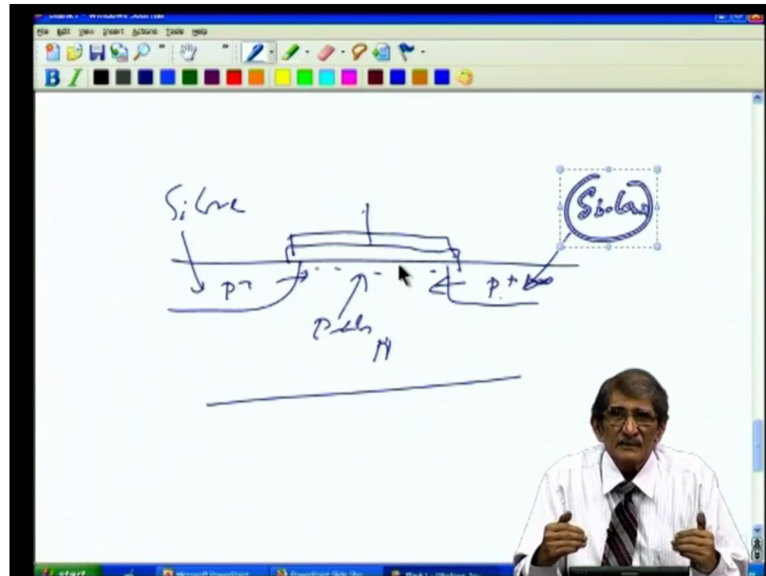

If I have the channel here, if I have the p plus here and if I have P plus here this is [noise], I am talking of P channel device oxide here and then the gate; now what I should do is I must compress it in this direction.

Because this is the P channel I must compress a P channel how do you do that you put introduce, here silicon germanium silicon germanium alloy here when you do; do this implantation or diffusion introduce also on both sides silicon germanium this actually because these atoms are bigger compared to the silicon atom the channel is in between the 2 in between the 2 layers which actually has bigger atoms. So, it pushes this channel in this direction that use to compressive stress. So, the P channel devices P channel gets compression compressed gets compressed along the length of the channel the mobility of the holes goes up this.

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Impact of Strain on the mobility of holes and electrons in silicon

- Longitudinal tensile Strain along the MOSFET channel improves the electron mobility and reduces the hole mobility
- Longitudinal compressive strain increases hole mobility and reduces the electron mobility

- In P-Channel Si MOSFETs when the source and drain regions are formed using SiGe, the channel is in compressive stress – increases μ_p.
- In N-Channel MOSFET electron mobility is improved by a top layer of nitride which introduces tensile stress

Is the trick that the analog devices, I am sorry intel here has done this all that sais here is about indium in P channel de silicon devices. Then the source and drain regions are found by using silicon germanium channel is in compressive stress increases mu p in N channel MOSFET electron mobility is increased by top layer nitride which introduces tensile stress.

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Strained NEW Channel Materials

- Strained Germanium
- Strained Silicon
- Strained $Si_{1-x}\,Ge_x$

Refer : DA Antoniadis et al; IBM J. Res &Dev , Vol.50, No.4 /5, pp.363-377, July / Sept 2006,

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Now new materials last few slides strained germanium strained silicon all these can be used to increase the mobility over and above that if I have silicon, I can subject it, if I

have tensile stress, you know electron mobility can be increased. If I subject it to compressive stress that electron hole mobility can be compressive hole mobility can be increased, you can have germanium you can enhance the mobility over and above; what it has got electron mobility and hole mobility by subject it into strain.

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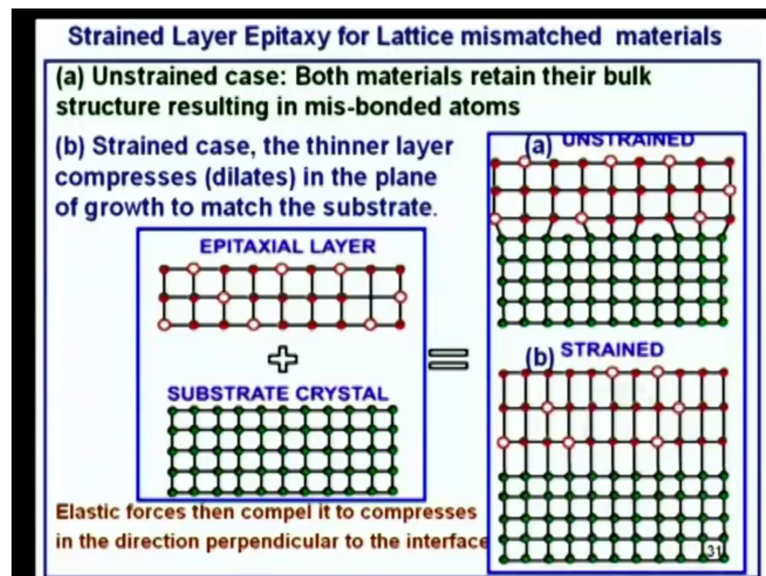

How do you do that? You can do that growing dissimilar metals we said for hetero structures you must have lattice match, but if I use lattice mismatch structures for example, I have silicon here which have lattice constant 5.43 between the atoms I grow germanium on the top of that lattice constant is 5.65 silicon germanium will be in between either I go silicon germanium or silic germanium as I grow thick layer the lattice will be there at of these silicon germanium.

But in between you can see the if it is thick layer it will relax to its own lattice constant and there will be broken bonds defective layer, but if I use the layer very thin there compared to this silicon layer then the silicon layer forces it back it the this is a this is there is no strain here there is; there are defects here thick there is you cannot go thicker layers of hetero structures, but if I grow very thin layer then the thinner layer gets compressed by the bottom, its pulls; pulls its back when you have one layer over the other the top layer is thin and the bottom layer is thick that actually pushes it like that compresses because it tries to this bottom layer tries to pull it along that direction.

So, that bond length increases like that there is compressive stress on this. So, bigger

lattice atoms that is germanium on silicon will get compressed if it compressed it is good for P channel, if I have silicon germanium on germanium silicon germanium is smaller lattice constant compared to germanium is the tensile stress you can make N channel MOSFETs higher mobility.

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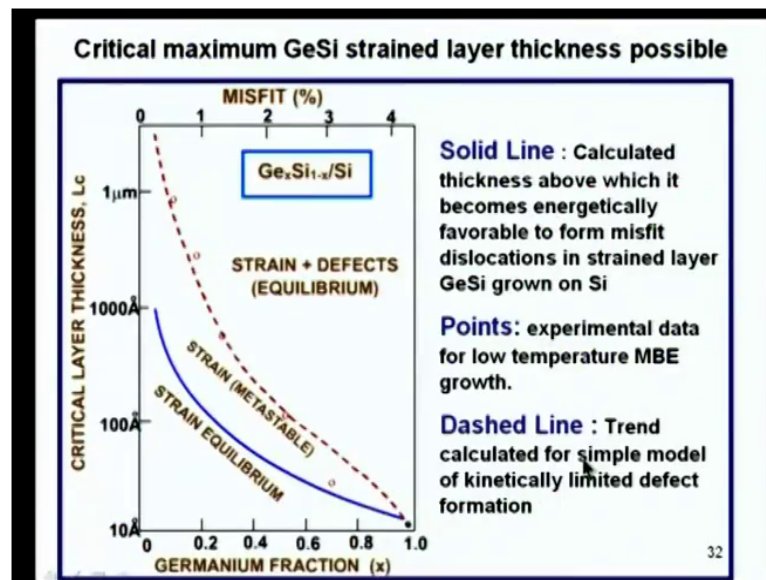

So, that is what is done is done what is done there. So, this gives you actually there are you actually there are you know this as you grow there is a critical thickness up to which you get this strain layer beyond that there is no strain layer its defective see for example, if I am growing a am growing a germanium silicon germanium when germanium is x; x is x; x germanium is 0.2, I can grow a about 0.1, my 1000 angstrom that is 0.1 micron layer thickness which is strained with the which has no defect that is like this I can grow if I grow more than that thickness, then it will be it will be like this like this defective layer so.

So, this tells you that if you want more germanium you know thickness that you grow will be very little for example, if I x x mole fractions of germanium you can grow hardly 2 nano meters of germanium which is strain layer with the which is defect free defect free. So, this layer is defect free, but it has higher mobility compared to that. So, now, will see how the strain induced layers can be introduced.

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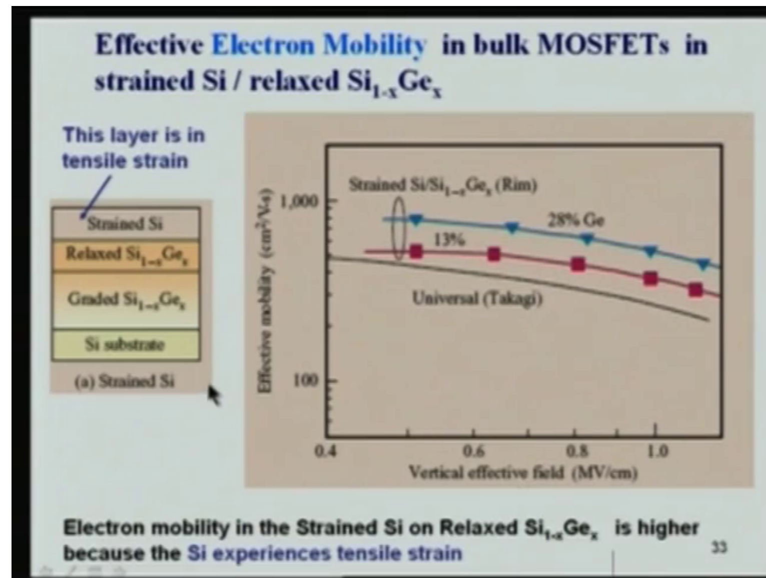

So, the one of the approaches is the silicon substrate graded silicon germanium, then relaxed silicon germanium which actually has lattice constant more than that of silicon, if I grow silicon layer on the top of that it will be strain and it experience compressive stress because along the horizontal direction compressive stress because lattice constant of this is more compared to that and this relaxed layer. So, it will start stretch it, it will stretch it. So, its senses tensile stress you can use that for this will act lattice constant of this is more compared to that and this relaxed layer. So, it will start stretch it, it will stretch it. So, it senses if the enhances the electron mobility by controlling the x in this layer you can control this lattice constant of this layer.

So, bigger the lattice constant more will be tensile stress more the x here bigger the lattice constant more will be stress here more will be the strain more will be the mobility. So, you can see x is 0.13 you get much better than the classical reported mobility of electrons if I make expand to it you get even higher. So, this is one of the approaches which was reported in literature by some of authors. So, electron mobility in strained silicon grow on the silicon germanium is higher because of the silicon experiences tensile strain.

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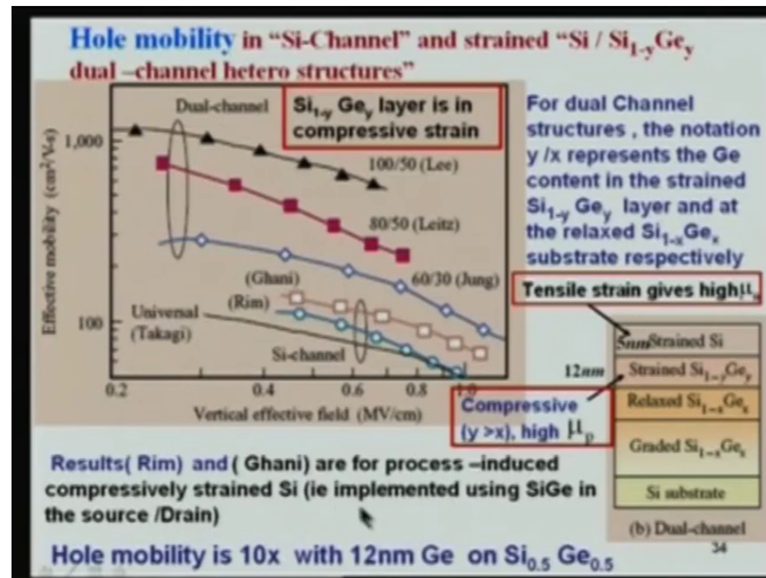

Now, there is one we can get dual channel this are the reported in literature few years back.

Silicon graded silicon germanium x is what is the mole fraction of germanium and then you grow on that is relaxed layer means actually the lattice constant is governed how by how much x is there on the top of that you go grow strained you grow silicon germanium with mole fraction of y larger than that of x; that means, y larger than that of x means actually germanium content is more in this layer compared to the germanium content is here. So, if germanium content that is about 12 nanometers if the germanium content is more in this layer; that means, its lattice constant is more compared to the bot bottom layer if the lattice constant is more it will be experience because of this layer, it will compress it, it will try to bring it equal to this particular layer.

So, there will be compressive stress on the careers here say if it is compressive stress you get the compressive stress for y is larger than that of x how much is the compressive stress depends upon how much is y compared to x ok.

So, because due to compressive stress the hole mobility in this layer can be increased tremendously. So, these are the results which are being reported experimentally for example, if y is 0.6 and x is 0.3 y is greater than x its double you get a mobility for this is as a function of vertical electric field for a given electric field you get the whole mobility which is about 390 meter square per volt second nothing much to most of, but I got the y

0.8 that is 80 and 50 much higher y, you get mobility which is getting down to 800 holes mobility, 800 much more than that in silicon you go to 100; that is germanium itself there strained germanium then you get mobility much more than 1000 centimetre square per volt second that is the hole mobility.

So, you can see the power off strained layers. Similarly if I put on this layer silicon strained layer I can get because this is smaller than this, I can get tensile stress, I can make N channel here, I can get P channel devices N channel device that is dual channel MOSFETs you can make here.

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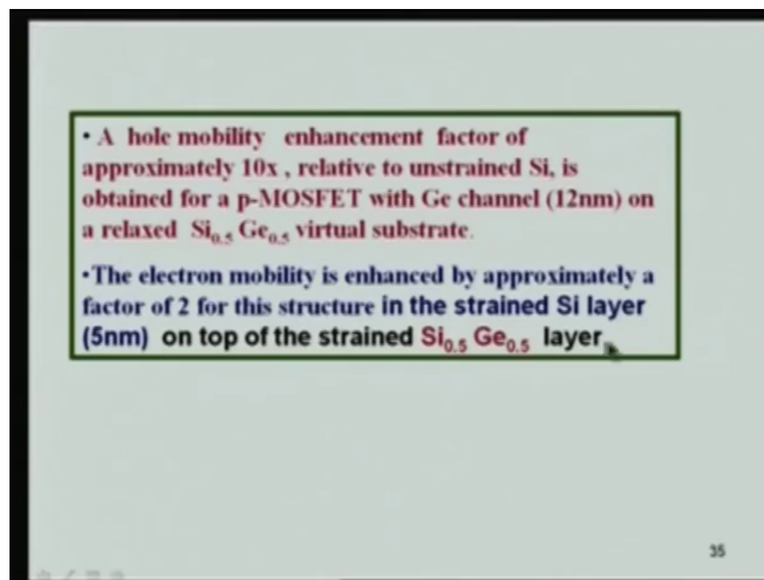

So, the hole mobility enhancement factor is about 10 x; there and electron mobility is enhanced approximately by factor of 2 all that they can be seen in that case. And this is actually, we result that we get hole mobility enhancement you get if you use silicon germanium at the source end, but this is you see strained layer you had much larger hole mobility compared to what you seen by using the silicon germanium in the source and drain.

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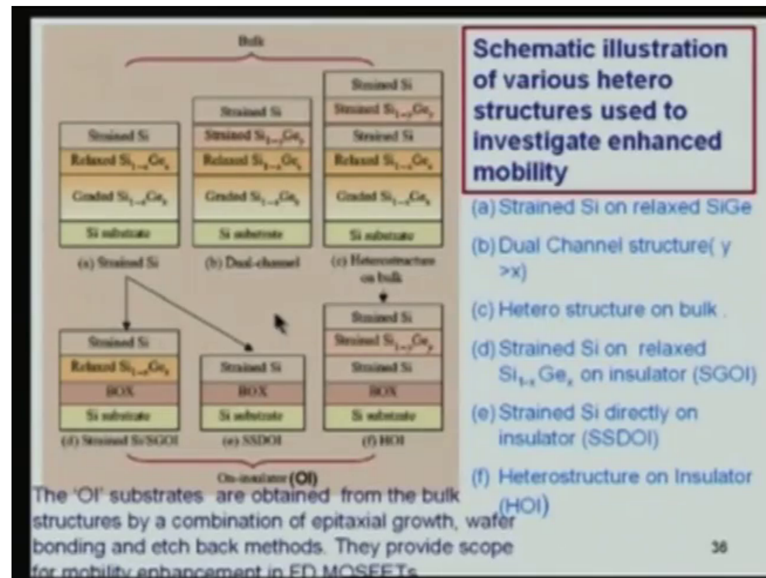

Now, the last one what I am trying to point out here is actually we can have the hetero structure on insulator there is hoi. So, you can have the; you can grow relaxed silicon germanium on that and you can grow strain layer here and put it upside down and bond on the on a silicon with oxide h set of layer you can get strained silicon layer. So, what I am trying to point out is by using this combination of this bulk layers mounting it upside down on the bottom layer and etching down the unwanted layer like this you can get strained silicon.

For example here you can have this layer contact on to the buried layer you can see here you; you have got silicon silicon strained silicon silicon put upside down, bottom you have got this is coming at the bottom like this and want it and etch at the unwanted layer you get the structures like the hoi.

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Summary

- Process-induced stress has been used to achieve significant mobility enhancements in short-channel devices (e.g., ;2x for holes in 65-nm technology .

- Si/SiGe materials system has the potential to achieve very large improvements in mobility (e.g., ;10x hole-mobility enhancements for strained Ge channels).

- Hetero-junction devices such as HEMT enable very high mobility transistors using doped wide band gap Semiconductor over a narrower band gap undoped semiconductor

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So, what you have summary process induced stress are then used to achieve significant mobility enhancement in short channel devices silicon silicon germanium material systems has the potential to achieve very large improvements in mobility. For example, 10 x hole mobility enhancement for strained silicon germanium channels have been reported hetero junction devices such as HEMT enable very high mobility transistors using doped wide band gap semiconductors.

With that I conclude my discussion on classical MOSFETs, where we have covered where there be channel HEMT.