Nanoelectronics: Devices and Materials
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Lecture - 29
GaAs MESFETs: Enhancement and depletion types
Velocity Overshoot effects In GaAs MESFETs

We continue our discussion on the compound semiconductors.

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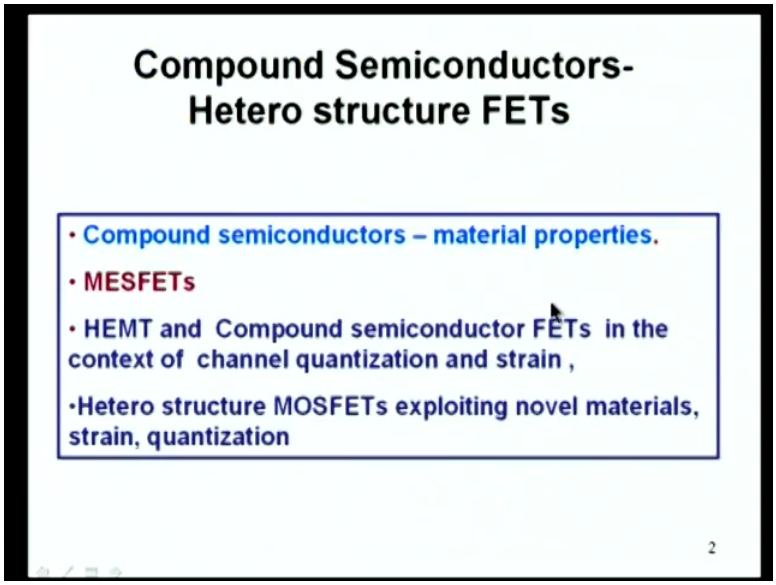

Particularly we move on to the FETs and hetero structure FETs we have just begun our discussion.

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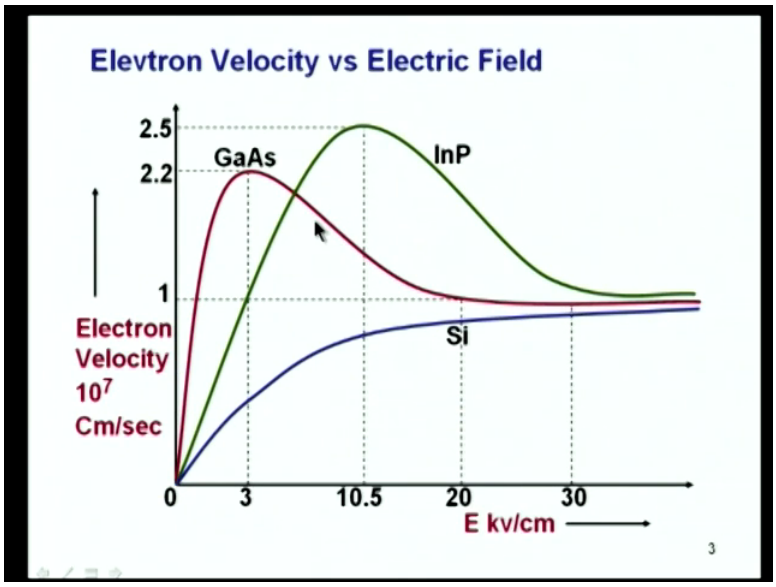

And as we have shown that the gallium arsenide and indium phosphide have got electron velocity versus electric field totally different from that in the case of silicon we have claim that this is because of the transport mechanism the electrons tend to be in the high; high electron mobility region that is no effective mass region at a slightly lower energy and it gets transferred onto the higher mass region where the mobility falls. So, it go through that region and ultimately goes into the saturation region.

So, if you have bias the device or if the electrons enter into this high field region suddenly it does not go there straight, it will go through this portion and go there. So, due to that there will be a time interval during which the electron goes through this peak velocity.

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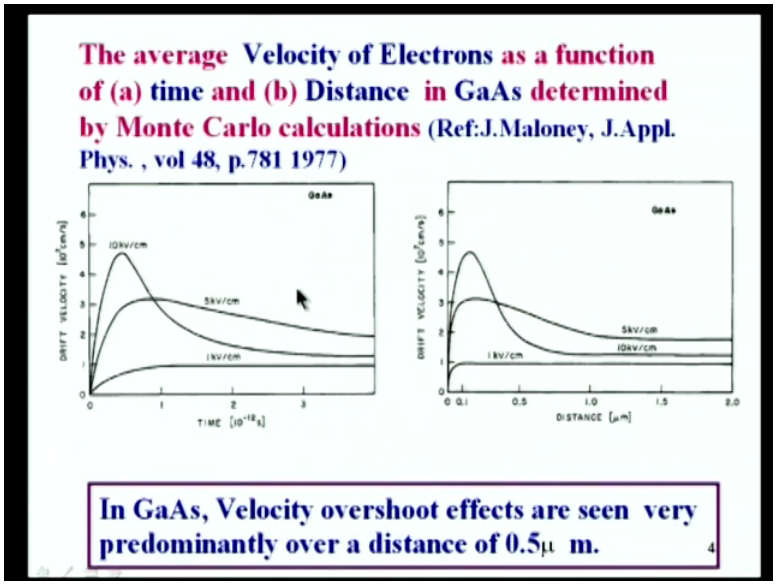

So, that is shown in this graph that is time versus drift velocity of gallium arsenide if you take if I apply 10 kV that is a saturation field at 10 kV, but in the initial couple of microseconds the velocity much higher than the saturation velocity because the electrons are located in the no mass region.

So, their velocity is high at that field, but once they acquire energy they go into the region where the mass is high. So, it saturates. So, if you convert it into distance we know that now this distance see by the time it has moved reached that velocity it has moved through this region. So, drift velocity versus the distance along the channel from the source will have the velocity like this for 10 kV. So, that would tell us that there is specific benefit for gallium arsenide devices and indium phosphide devices.

Where if you go to short channel length the over the entire region the velocity will be higher than the saturation velocity. So, that give you a higher current driving capability for a given dye device and also higher trans conductance there is a driving capability is better.

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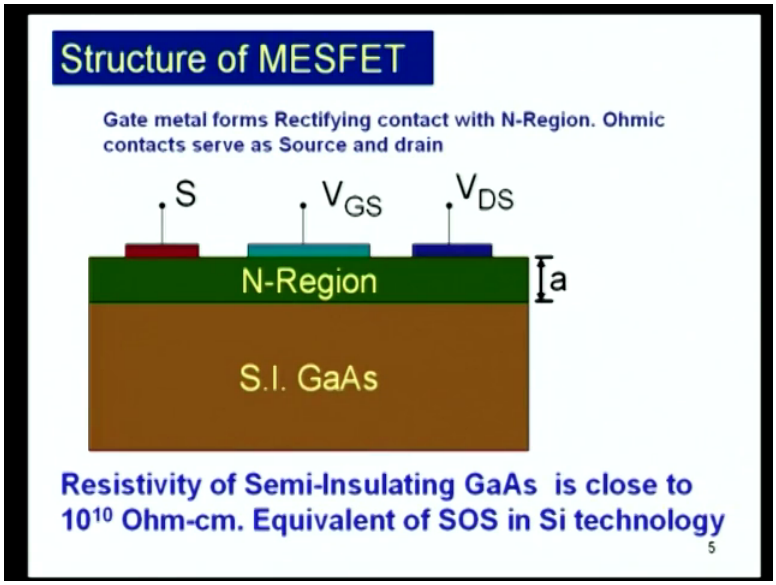

So, device which is very popularly used in the gallium arsenide material is the is the metal semiconductor field effect transistor rather than using the MOSFET as in the case of silicon, all the most of these gallium arsenide microwave millimeter microwave integrate circuits m I my mic. So, those devices are made up of MESFET logic circuit though there are improvements which we can discuss in the next lecture other type of devices like the HEMPT which are being attended to know. So, here I already pointed out that you have got the source and then which are ohmic contacts through the n type region which is a thin layer realized on semi insulating gallium arsenide now this contact is a gate contact in case there is no gate the between the source and drain you have got this conducting channel.

So, there will be it is equivalent of a resistance as you vary the voltage the current will vary across through the resistor now how much is the current flow depend upon the doping here and how much is the thickness of this n region suppose the thin layer is very thin the; now if you are is not there at all the full layer is available for conduction suppose in this metal semiconductor contact which is the rectifying contact which is serving as the gate is present on the top of this layer, there be there will be depletion layer below that channel below the gate, because some key contact or rectifying contact will. Now always have a depleted layer suppose due to that built in potential the depletion layer below that is completely depleting the channel the current flow between the drain and the source will be 0, because there is this is there is no careers available entirely depleted. So, if I want to bring it on condition what I have to do would be I have to reduce the depletion layer

width.

I can reduce the depletion layer with by thorough by see this metal semiconductor contact apply plus voltage to the gate depletion layer can width can open that is the level of current of flow; that means, the device can act as announcement more type of device if it is depleted with then there is a 0 gate bias alternately if the doping at thickness are such that the depletion layer width at 0 bias is 0 less than the thickness of this channel. Then even without applying gate voltage there will be current flow because some channel is open as you can see here that will be depletion type.

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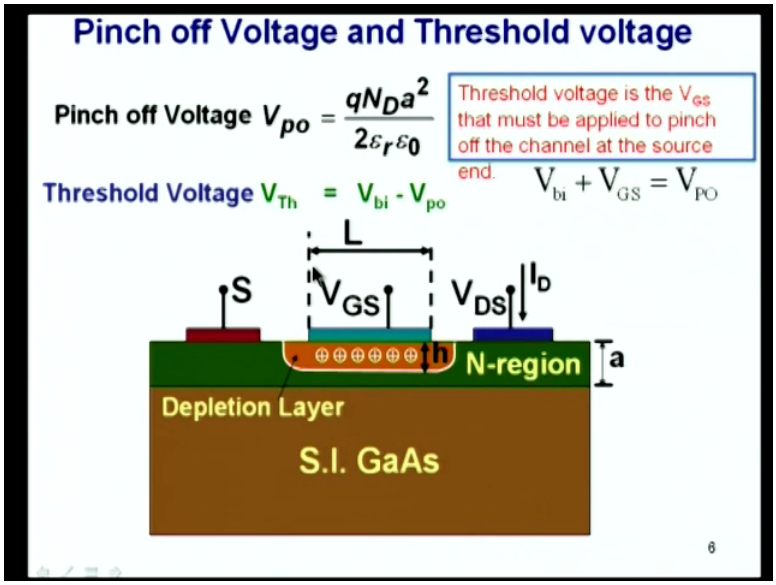

For example here, the diagram that I have shown even without the gate voltage if there is a depletion layer like this of height h then the current flow with through this region between this plus charges are the depleted layers between the semi insulating layer and the depleted layer depletion layer there is a path for current flow. So, if the and 0 when the gate bias is 0, if the depletion layer width is less than this channel thickness a then the current will be the present even at without gate bias that is depletion type of device.

Now before you go into a discussion of this type of device, we will see how couple of definitions one is the pinch off voltage pinch off voltage is the voltage or the potential that must exist across the depletion layer which completely depletes that channel. So, due to the potential V p 0 present across the depletion layer if the channel is completely depleting then there is no current flows that is pinch off that is channel is completely pinched off

from source to drain completely. So, you can see that from the standard relations from the abrupt junctions of the model the pinch off voltage will be q Nd is the doping a is the thickness of the layer a square divide by twice epsilon r epsilon 0 epsilon r is the permittivity of gallium arsenide if it is silicon it is that of silicon it is about 12.8 for the case of gallium arsenide for silicon its 12.

So, how much is that pinch off voltage depends upon the thickness and the dopping of this thinner layers pinch off voltage it is higher doping pinch off voltage will be higher for a given thickness. So, now, you can see that if the built in voltage is less than the pinch off voltage the depletion layer width will be less than the channel thickness; that means, it will be normally off. So, if I have to turn off the device I have to add additional gate voltage to the built in potential. So, that the depletion layer becomes completely equal to a. So, if V bi it is equal to h V bi plus V GS actually V GS is should be negative because the polarity of V bi is plus here and minus there, you have to add on gate voltage means actually you have to pay ninety voltage. So, if I apply VGS. So, that the depletion layer widens and becomes equal to a then V bi plus V GS is equal to VP 0.

So, what you are telling is if I apply a add V GS to V bi then it will be VP 0. So, the channel will be pinched off now the definition of threshold voltage. So, let us come back to this now suppose V bi equal to VP 0 even if your slightest voltage is applied to the gate plus voltage the depletion layer width will reduce suppose V bi is less than VP 0, I must apply negative voltage to the gate.

So, that depletion layer widens to turn off the device for example, when the built in voltage is 0.5 volts if the depletion layer width is h, I must add let us say and let us say d built in potential is 0.5 and VP 0 is 1 volt then I must add 0.5 volt to the gate. So, that deplete entire channel is depleted; that means, the V GS will be actually what you reply will be same polarity as the built in voltage that is gate voltage will be negative. So, if I apply 0.5 volts negative voltage to the gate then the channel will be pinched off the gate will be turned off..

So, threshold voltage is the voltage that you must apply to the gate. So, that when you apply that the potential across the channel is equal to VP 0. So, that V GS is actually equal to V bi minus VP 0. So, V threshold voltage threshold voltage of the MESFET is defined as the gate voltage that I must apply. So, that the tan channel is just depleted see in the example that you have taken if V bi is 0.5 and VP 0 is 1 volt threshold voltage is 0.5

minus 1 that is minus 0.5 volts, I must apply minus 0.5 volts to turn off the device it is in the verge of turn on suppose in the V bi is 0.8 volts and pinch off voltage is 0.5 volts V bi minus VP 0 is plus 0.3 volts; that means, I must apply 0.3 volts to bring it to conduction plus voltage because even without applying the if this is 0.8 and VP 0 is 0.5 even without the gate voltage channel will be depleted I must apply plus voltage to the gates.

So, that the channel is just opening up that is a definition.

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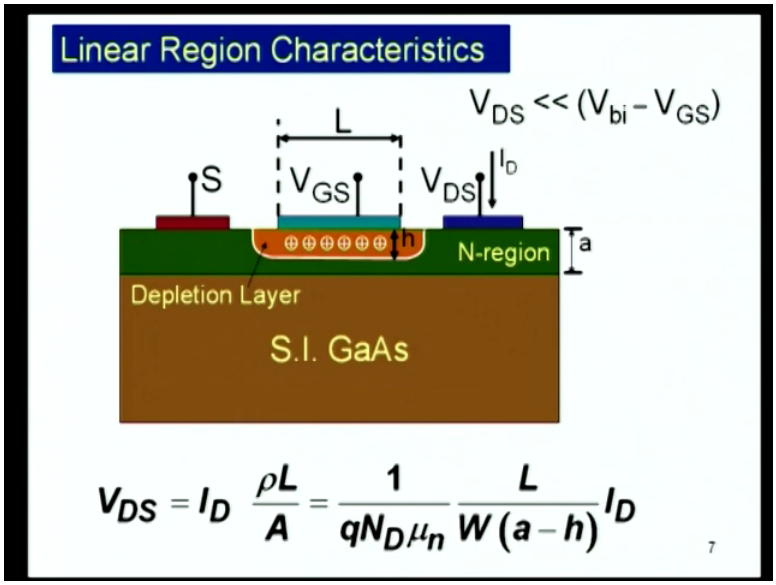

Now, let me go into the quickly into the analysis of this device not into too great detail, but how it comes about just like in the case of MOSFET or any other FET the MESFET also have got linear region, then the try out region and the saturation region. So, if in the linear region, it behaves like a resistor that is the channel thickness is same from source into the drain end that like in the case of MOSFET the channel charge is same from source into the drain end here channel thickness is the same from the source into the drain end. So, we are talking of the drain voltage which is very much less than whatever voltage is present here V bi minus Vb; V GS see for example, when V GS e equal to 0 there is certain depletion layer width now V GS what we have applying here is if I write just V b; VGS, then you have to if you deplete it you must make it negative. So, if I add V bi minus minus V V GS this is negative. So, then depletion layer with widen. So, V bi minus V GS is actually a total voltage present here to example if I want to give plus 0.5 minus of minus 0.1 volts that is plus 0.5 plus 0.1 0.6 volts.

So, this is actually more than the V bi which you are applying here. So, then the depletion layer will be widened here. So, if the VDS is very small compared to this voltage drop across this depletion layer; that means, drop from here to here train to source end e is negligible compared to this depletion layer width. So, which would mean if I go from this end to that end the depletion layer width is not changing.

So, as a result what we can say is when I apply voltage VDS which is small compared to this voltage across the depletion layer, the current will be or the current voltage relationship is just like a resistor. So, VDS is actually. In fact, what you are saying is doing is you are neglecting the drop between this point and this point assuming that this is very close in contact with this gate region.

You cannot keep in touch with this gate region because then it will sort there must be some finite space ID into r is the voltage drop across the resistor r is rho L by a rho is the resistivity resistivity of the channel L is there rho is 1 by sigma is qN D into mu n. So, this is actually this is actually the whole term is rho or one by sigma length area of cross section for the current flow in the along the channel is channel thickness channel thickness into width cross section if you take that is thickness into the widthness perpendicular to this plane of this one. So, area of cross section to the current flow is a minus h that is that thickness into w. So, you can see that w into a minus h is the area of cross section. So, this rho L by a into ID is the voltage drop.

So, I just rewrite that we will develop on that what is A? A can be correlated to the pinch off voltage through this relationship so. In fact, I can say that a is proportional to square root of VP 0 and what is h? H will be see VP 0 is actually the voltage total potential present across the channel when the its depleted depletion layer width is equal to a now in this particular situation the voltage present across this is V bi minus V GS that is a voltage. So, if h is the depletion layer width when the voltage is V ba minus V GS then you can use the same equation V bi minus V GS is equal to qN D into qN D into h square. So, you can use that relationship to get that depletion layer width like this. So, this is related VP 0 and h is related V bi minus VP 0 that is all VG 0 that is what you have to remember ok.

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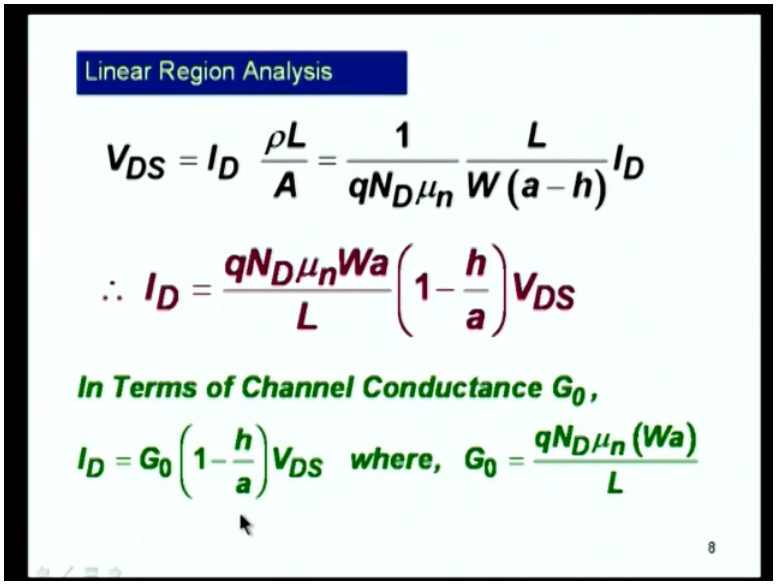

So, VDS is this one I have rewritten this equation whatever we explained now; now ID therefore, I can write ID by re writing this taking to the other side q Nd mu n into W into a divided by that this quantity.

I rewritten that what is this quantity this is sigma divided by L channel length into cross section cross section of the channel when it is fully open w into a is actually the entire cross section w is the depth a is the thickness. So, W into a is the cross section. So, if you see this; this is the conductivity, conductivity into area divided by L that is a conductance instead of resistance it is conductance qN D mu n into V and then. So, that you can write it as and I just pull that out a. So, you get this one. So, in terms of the channel conductance G naught this is G naught I can write ID is equal to G naught into 1 minus h by a why we are writing like this is you know that a will be proportional to root of VP 0 and because if VP 0 is present depletion layer width is a and if the voltage across the depletion layer width is V bi minus V GS h is a depletion layer width.

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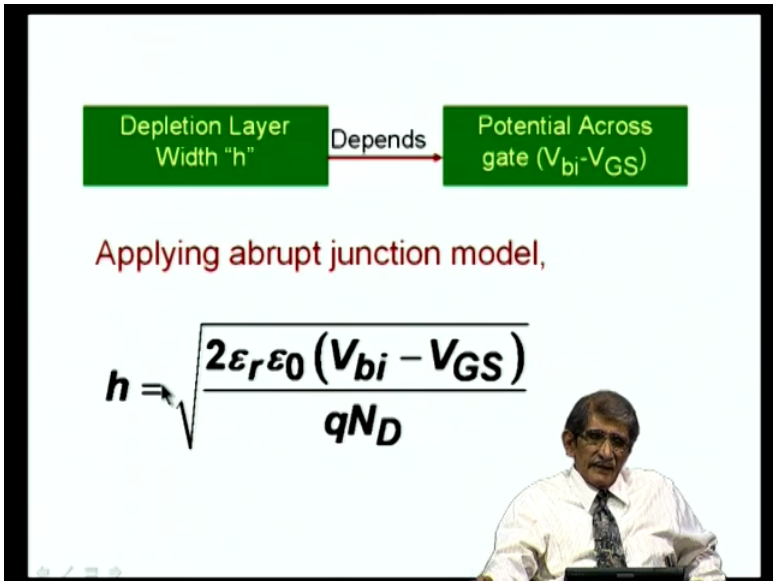

So, you can write this as ratio of the 2 will be square root of V bi minus V GS divided by VP 0 that is a thing h is equal to qN D see qN D h square divided by twice of epsilon r epsilon 0 is the voltage drop across the depletion layer that is a standard equation if your VP 0 that will be way where a is equal to this whole term into VP 0 h is equal to this whole term into whatever voltage is present across the depletion layer that is V bi minus VP 0. So, if I take a by h this term will cancel I am sorry; if I take h by a; this term will cancel and h by a will be square root of V bi minus V V GS by a.

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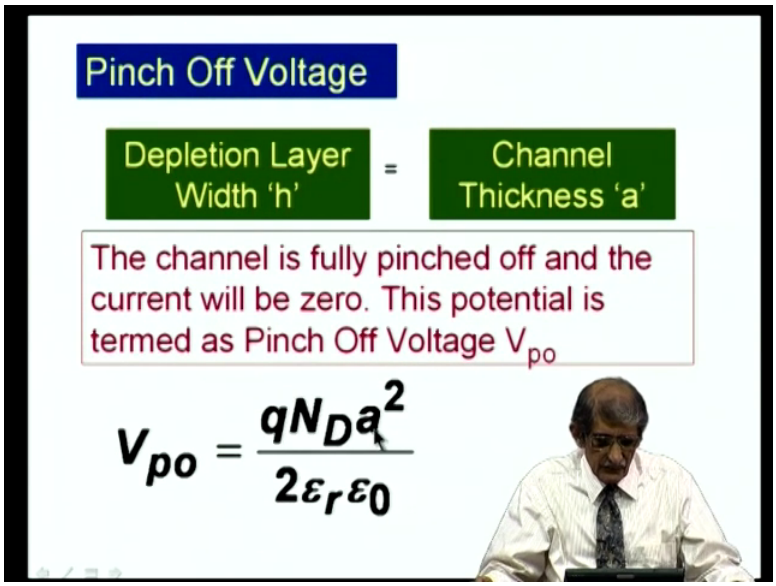

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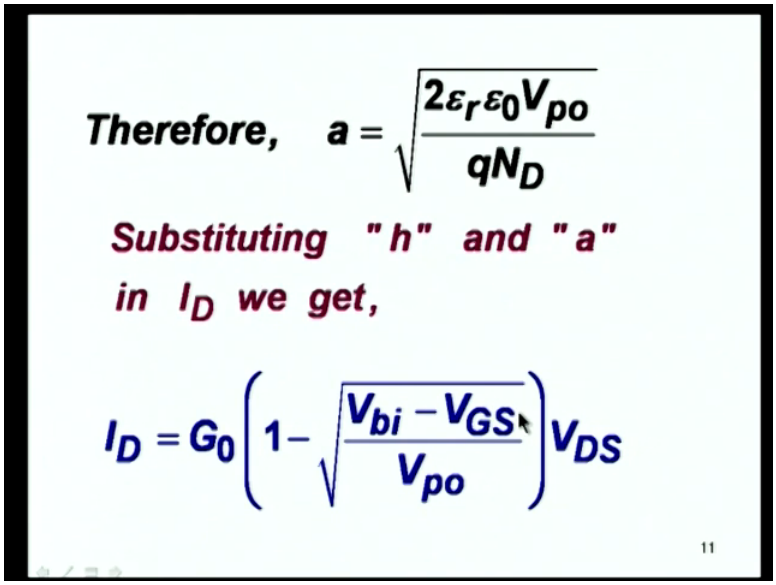

So, VP 0 is that a is that. So, substituting both the things as I just pointed out ID is equal to G naught into one minus h by a into VDS that is what we saw; now for h by a; a is this quantity h is a same quantity, but replaced by V bi minus V GS 0.

So, h by a will be this. So, this is the ID versus VDS then VDS is small compared to be the voltage drop across the depletion layer implying the resistance is actually it behaves like a resistor between these portions the depletion layer width is remaining the same thing because the drop from here to here is not changing we have VDS is very small there is some. So, that is the thing.

Now if I take the ID characteristics of this small MESFET what will happen this is constant it is actually channel conductance when it is fully open and for a given voltage this is constant. So, if I vary ID if I vary VD ID will vary linearly V GS is actually negatives of this will add on. So, if I keep on increasing the V GS negatively this term become larger and larger this become smaller and smaller depletion layer width become wider, wider and wider. So, the channel conductance total conductance will become reduced current will reduce.

So, far given a gate voltage there will be linear relationship. So, V GS equal to 0 1 minus V bi VP 0 into VDS.

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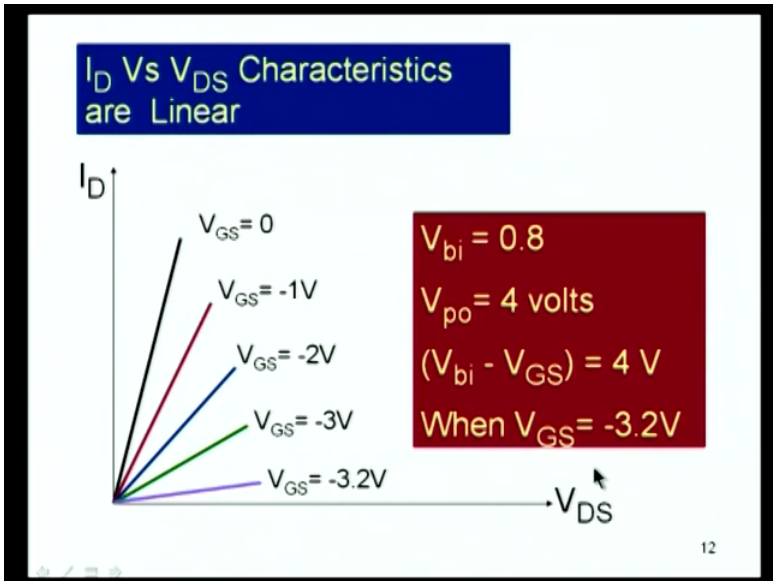

So, if I increase the gate voltage the depletion layer width increases channel thickness available current flow will reduce. So, current is reduced that. So, you can see several linear characteristics you can obtain by keeping on increasing the V GS till you spins out the channel completely when you spins out the channel completely current will be 0. Now what will happen if I increase the drain voltage further.

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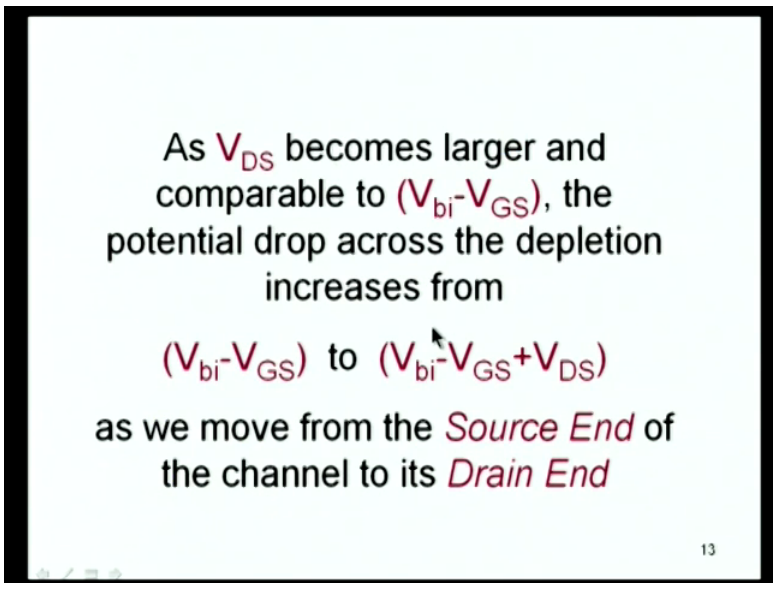

As VDS becomes larger and comparable to V bi minus V GS what we are telling is I increase the VDS initially when the VDS is small the depletion layer is constant

everywhere.

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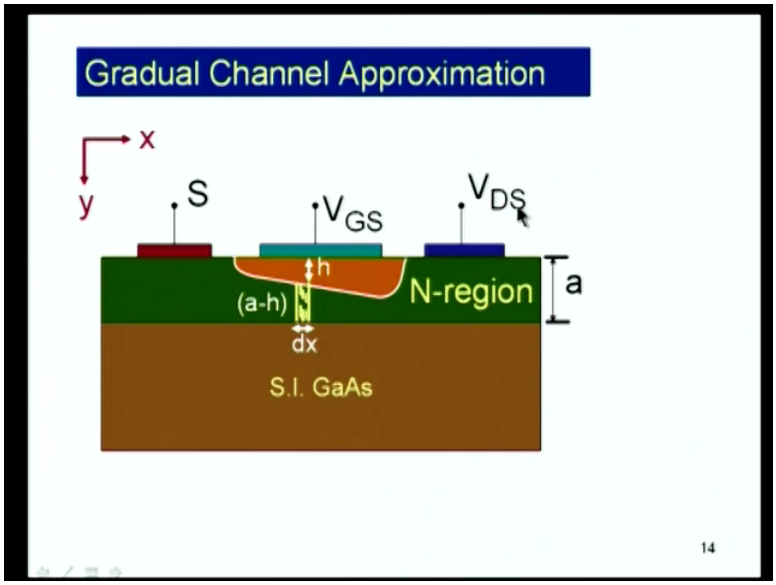

Now, as I keep on increasing the voltage that drop from the drain to the source region becomes comparable to the depletion voltage across the depletion layer width depletion layer the voltage across the depletion region was V bi minus vgs. In fact, if you take the magnitude it is V bi plus magnitude of VGS. So, that is plus here minus here now if you move in this direction there is radiation plus voltage here. So, if this is V bi minus V GS from here to here.

If I take the drain end the voltage from here to here will be for example, if it comes from here V bi minus V GS rise from here to here from here to here further we VDS; VDS rise is there. So, total voltage drop across the depletion layer will be V bi minus Vb V GS which is the drop there plus the drop across the channel that is exactly what you did in the case of MOSFET. So, voltage drop across the depletion layer at this edge will be more than the voltage drop here by an amount equal to the VDS even in the linear region, it will be there, but it is negligible compared to this voltage.

So, because the voltage drop is more here you can see the depletion layer width will be something here h naught a; a move here it will keep on increasing. So, that is what we are saying here at the drain end the VDS as VDS becomes larger and comparable to V bi minus V GS that is a voltage that is present at the source end then the potential drop across the depletion layer increases at the source end at the source end from V bi minus V

GS to V bi minus V GS plus VDS at the drain end.

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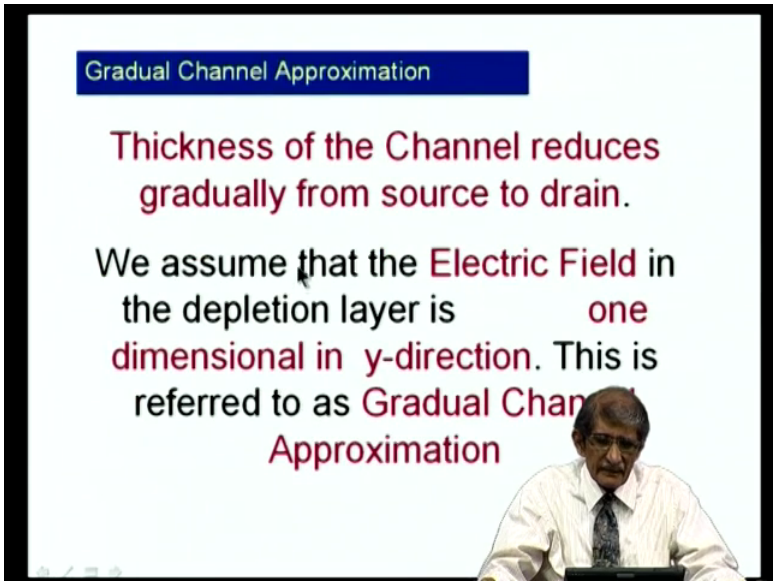

As you move from the source to the end of the channel. So, as a result depletion layer width will be wider the thickness of the channel it reduces gradually from the source to drain because potential drop here is something here it is more by an amount equal to VDS. So, depletion layer gradually decreases increases from here to here and the channel thickness decreases from here to here.

So, it is equivalent of a resistor if the resistor is like that if the resistor is like this constant width when you increase the voltage current will increase linearly suppose if the resistor becomes narrow at the drain end due to the depletion layer width the effective resistance of the channel increases. Therefore, even if the resistance are constant current would have increased linearly, but because as you increase the drain voltage the shape of the resistance keeps on changing like this the resistance of the channel of increases as you increase the drain voltage because the resistance increases with the drain voltage the current will not increase linearly with the drain voltage.

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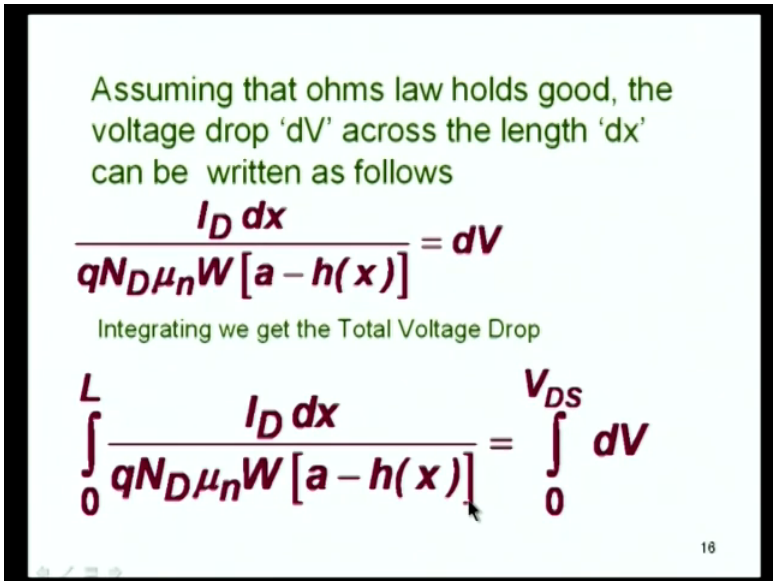

As a result what happens is you get a I am sorry, just you get a you as a result of that there is deviation from linearity and ultimately, the current will saturate current will saturate when this particular region thickness becomes very very small here; drain end when the depletion layer almost reaches to this end of the channel thickness, it is almost closes when it almost closes the resistance becomes very very large, it cannot close anymore further it in the small gap there.

So, current in the control wave whatever is flowing through that small gap if it you can see if the current tends to increase beyond that points the drop would increase if the drop increases the depletion layer width is wider if it increases then the it will close the channel if it closes the channel current will tend to fall. So, depletion will open.

So, what we are telling is a dynamic equilibrium will reach where channel will come to close almost closing region, but not completely closing. So, that to allow whatever current is entering here to go through that thing. So that means, from here to here, the drop is actually equal to V GS V bi minus V GS plus VDS that will drop across the depletion layer and drop across a depletion layer is just sufficient to close the channel; that means, the total voltage across the depletion layer. Now will be V bi minus V GS plus VDS that should be equal to pinch off voltage VP 0. So, when V bi minus V GS plus VDS becomes equal to VP 0 the current will saturate that is all the principle that is involved here. So, that is idealistic model there were changes in that, but still we can use it as a for long channel devices without any hesitation. So, what we are going to do is quickly see.

So, now what we know is depletion layer widens channel becomes narrower and narrower at the drain end therefore, ID VDd relationship is no longer linear because the resistance keeps on increasing, but when the voltage drop across the channel reaches a certain value that is called a VD sat at that point the depletion layer almost closes this V cannot the voltage cannot increase beyond that point because then the depletion layer if it closes fully current will tend to fall. So, the dynamic at the dynamic equilibrium you reach the VD sat such that the depletion layer at the drain edges just closed just about to close; that means, voltage dros drop across the gate and this channel end is VP 0 which would mean that VP 0 is equal to V bi minus V V GS plus VD sat that is a condition for saturation current you can quickly run through this.

So, now actually this is you take this as a gradual channel approximation because when analyzing and finding the depletion layer width you still use one dimensional equation along this letting a indicating that the 2 dimensional if it is; are not present here in this direction. So, that is called gradual channel approximation meaning the channel thickness changes gradually from source to drain end or the voltage change here is very gradually go along with the channel length or in other words L tp if is in this direction is small compared to that if it in the vertical direction that is like in the case of MOSFET where we also talked of gradual channel approximation.

Now, with this understanding and just quickly run through the derivation not going through the very detailed. So, all that we have to see is use the same equation whatever we are using take a small width same ir V is equal to I into r what we do is take a small width d of x determine what is the drawback across that and at any x x is in the direction at any x take t of x channel length d of x what is the voltage drop across that integrate that from x equal to 0 to x equal to L channel length L and voltage equal to V bi minus vgs.

Here to V bi minus V GS plus VD VDS that will give the idbd characteristics over the entire region from linear to the saturation region. So, what your voltage drop across this for a given ID id into rho into d of x divided by area of cross section, so that rho is of course, the channel resistance which is one by q mu Nd and area is w into d of x I am sorry w into a of a minus fh. So, voltage drop across d of x can be written in this fashion ID into d of x its ID into L divided by sigma that is ID into rho is one by this divided by area; area is w into a minus h of x a minus h of x is thickness w is the width w into a minus h is the area of cross section.

So, you all that you have done is ID into rho d of x divided by area that is a voltage drop across that now what you do is all that you have to remember is a is related to root of VP 0 h minus of x is related to the voltage drop at x across this that will be that will be actually whatever voltage present here plus V of x there V bi minus VGA; V GS plus V of x. So, it should be proportional to square root of that voltage. So, that is what we do here now integrate it from V ori from source into the drain end this x 0 to l.

That is what we did when you do that substitute for a and h of x in terms of the VP 0 and what is the voltage present across the depletion layer we have h of x is a depletion layer at any x net width of that depends how much is the voltage across the depletion layer that is V bi minus V GS plus V of x. So, same thing I have written.

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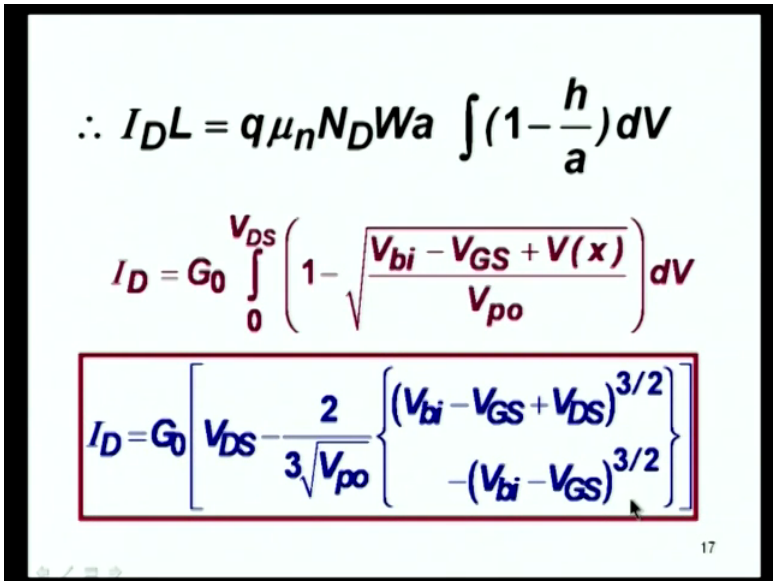

Integrating ID into L with that quantity I have nothing no changes just read it on the whole thing because I can pull all these in front to the right hand side integral left hand side is ID into L right hand side you get this term substituting for h and a in terms of the voltage across the depletion layer is this one at x voltage at across the entire layer or pinch off will be VP 0 all that you did this is G naught I put L down this that is G naught conductance into this quantity integrate that and not go through that quickly that is the integral value.

So, you can see that if this term were not present VDS is this term is negligible I would have got ID verses VDS linear proportional to conductance, but with the gate bias there is

a term which is reducing that. So, if you apply like reverse bias to the gate this value will go down and we saw the linear region that characteristic or like this, just I am skipping going back to show that linear region, but when the drain voltage becomes large enough drain voltage becomes large enough this term becomes smaller and larger and larger. So, for a given gate voltage for a given gate voltage if I increase VDS you can see that that will result in reduction of this term that is it will not increase as much as it would if this were not there it would have increased linearly, but because of this increase in VDS the current will not increase proportional to VDS, but it will deviate from linearity into non-linearity when and when VDS this entire term becomes equal to VP 0 at Vc this at voltage at the drain end of the channel when that becomes equal to VP 0 the current saturates ok.

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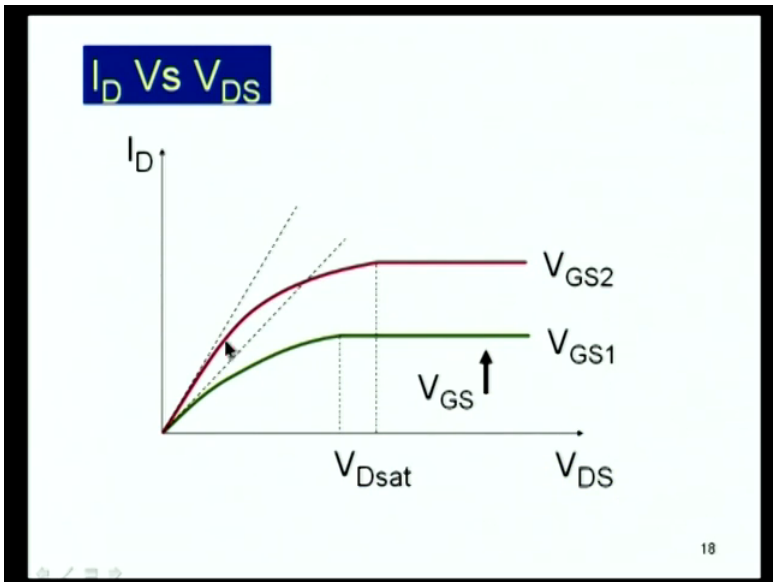

So, you can see that characteristic goes on linear from linearity than when that VD sat; at VD sat this voltage which is the voltage drop across this voltage which is the voltage drop across the depletion layer at the drain end h becomes equal to a actually at that then at that point that is VP 0, then you get saturation.

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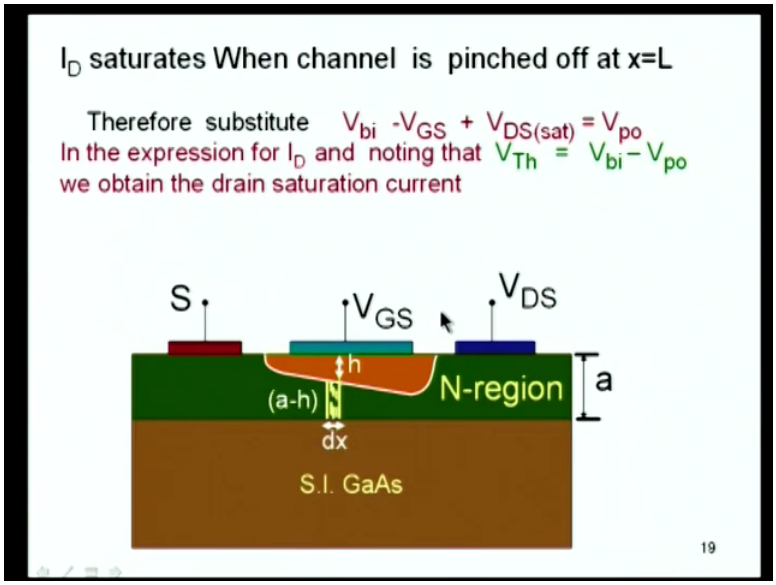

So, that is the situation that you have got. So, ID saturates when the channel is pinched off at x equal to L this almost closes that therefore, V bi minus V GS plus Vb d sat that is the voltage drop across the depletion layer V bi minus V GS is voltage drop here plus voltage drop VD sat. So, when that becomes equal to VP 0 this channel closes that is the drain voltage at which current saturates. So, that is what we have plotted here VD sat is given by this is given by this for a given gate voltage VD sat is rate is determined from the applied voltage gate voltage and the pinch off voltage.

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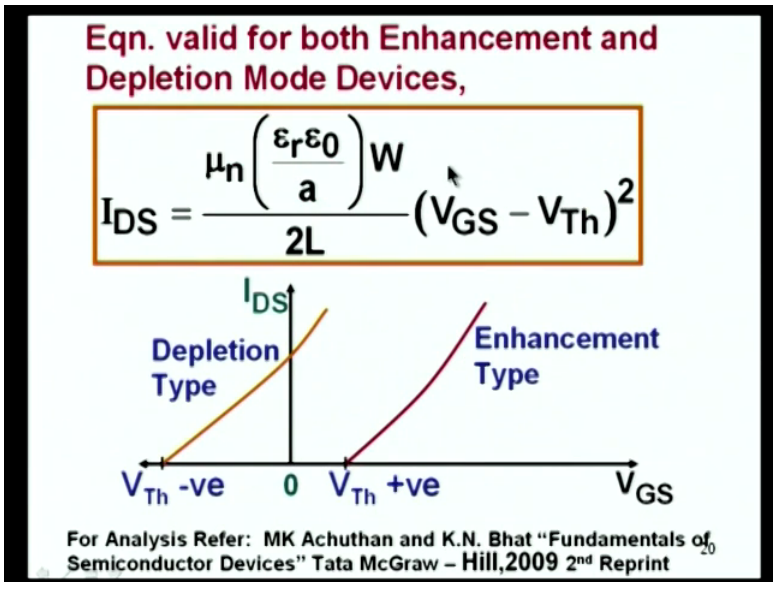

So, you can actually I am not going through that you can actually simplify that and write the whole thing in terms of threshold voltage because threshold voltage actually is actually V bi minus VP 0. So, if I take VD sat I mean this condition VD sat equal to Vb 0 minus Vb i.

I take this write see VD sat is equal to as I write it in terms of the threshold voltage VD sat here is equal to take the whole thing to the right hand side, then you have got VD sat equal to V GS minus V bi plus VP 0 or in other words.

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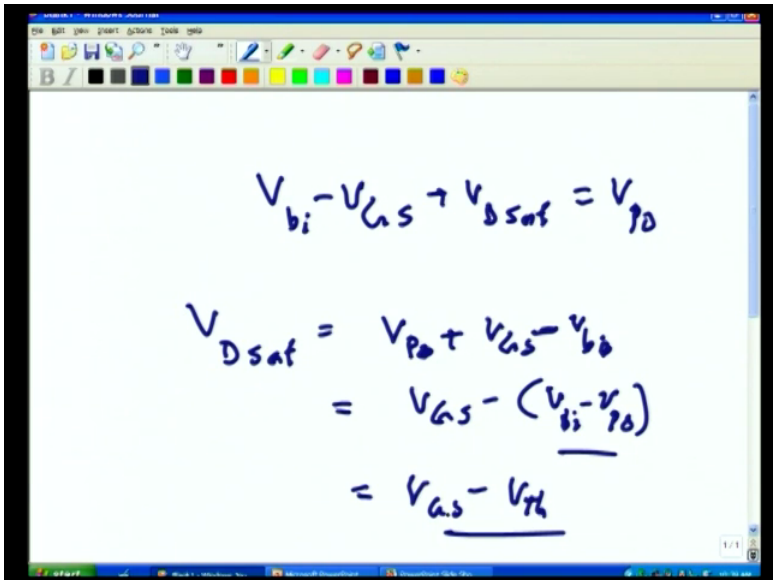

You can see that the V bi minus V GS plus VD sat when that happens that is VP 0 now what is VD sat is equal to VP 0 minus V GS I have taken it that side minus V bi which is actually equal to V GS minus V GS minus this is V bi VP 0 this will be 0. So, what is this quantity that is V GS minus V threshold? So, what you are telling is in the case of MESFET also the saturation voltage the drain situation voltage is equal to V GS minus V threshold voltage when the drain voltage equals to V GS minus V V threshold the current saturates this exactly the same thing.

That you had in the case of MOSFET in MOSFET also the drain current saturates drain current saturates when V GS equal to VDS equal to V GS minus V threshold. So, that is what. So, that is a nice thing about that. So, you can actually by substituting that term here V bi minus V GS VD sat or VD sat is equal to V GS minus V threshold and substitute it here use binomial theorem and simplify you get the ID verses V GS

relationship transfer characteristics exactly same as that of the MOSFET that is a very interesting see this drain saturation current when we use that relationship that is VD sat is equal to V GS minus V threshold which we have found it is to be true in the case of the MESFET also then you substitute in that equation that we derived and some approximations you do.

You will get ids is equal to mu some capacitance into w by twice L at V GS my V threshold whole square this exactly the same characteristics transfer characteristics of the MOSFET in the saturation region what is in the MOSFET ids is equal to mu n see oxide; oxide capacitance per unit area into w divided by twice the channel length into V GS minus V threshold whole square. Here all that you have to do is you can use the same equation as the MOSFET when you are to define threshold voltage as V bi minus V VP 0 that definition of the threshold voltage is different here then.

So, the saturation drain current is related to this V GS minus threshold whole square into this c capacitance; capacitance of the channel instead of c oxide per unit area you have got capacitance of the channel what is this epsilon r is the permittivity of the gallium arsenide epsilon 0 divided by thickness instead of oxide thickness you have got channel thickness instead of oxide epsilon r, you have got epsilon r of gallium arsenide we can see for this even if the mobilities are the same thing if I take the MOSFET if I take the MOSFET. And if the materials are the same thing this will be oxide cap permittivity and this is the permittivity of gallium arsenide which is about four three times larger than that of oxide.

So, for the same thickness as the oxide you will get drain current higher if drain get current higher you will get the trans conductance also higher what is trans conductance delta ID by delta VGS. So, if this quantity is large trans conductance will large, but we are telling is if I use a MESFET you can get the driving capability and trans conductance better than that of MOS; MOSFET because epsilon r is much higher compared to epsilon phi this is we are talking of the same thickness of oxide and same thickness of the channel. Now if I am using instead of silicon if I am using gallium arsenide in addition I have got this term which is much larger than that of silicon plus when I go to short channel MOS devices when the gallium arsenide you will have enhanced velocity enhancement effect due to velocity overshoot effects.

So, that tells you that gallium arsenide is a very good candidate for high frequency

operation. So, this is a nice thing you do not have to remember anything else for saturation region characteristics of the MESFET replace the oxide with the c channel. So, from this point of view if I want to increase that trans conductance or increase the drain current for a given voltage I can achieve it not nearly with the high mobility I can reduce the channel thickness and get that. But notice that if I reduce the channel thickness your threshold voltage will also change just like the MOSFET in the case of MOSFET your threshold voltage depends upon the oxide thickness.

Here also they threshold voltage will depend upon the channel thickness and doping, because threshold voltage depends upon V bi which depends upon the barrier height V bi minus VP 0. So, threshold voltage depends upon pinch off voltage pinch off voltage as you can recall depends upon that is been pinch off voltage depends upon channel thickness thinner the channel thickness smaller will be the pinch off voltage higher the doping higher the doping or.

If you can see for a given thickness or if you see VP 0 is equal to qN D a square by that for a given thickness if I increase the doping for a given thickness VP 0 will also go up, so it is a combination of the doping and the thickness exactly like in the case of the MOSFET increase the channel doping threshold voltage goes up if I increase the oxide thickness threshold voltage goes up same thing holds good here all the things that we talk of for the MOSFET increase holds good. So, the theme here will be to go to thinner; thinner channel thicknesses and maybe go to higher doping concentration when you reduce the thickness because after all the pinch off voltage depends upon the product of n d and thickness square. So, if I change the thickness it has accompanied by the doping if I reduce the thickness it has to be accompanied by increasing the dopping. So, that I get the same VP 0 that will be a bad news because.

If I go to thicker thinner layer if I have to increase the doping concentration which is necessary for that the resistance is less you your VP 0 will go up VP 0 can be controlled, but if I increase the doping mobility will fall. So, that is one thing one must remember now. So, this is a transfer characteristic. So, you can have normal people think that you cannot get in the j FET or a MESFET you cannot get its always depletion depleted mode depletion mode people think that you can see incase a threshold voltage make positive I can make the how can I make the threshold voltage positive threshold voltage is V bi minus VP 0 if V bi is larger than the VP 0 threshold voltage is positive; that means, I have to apply a plus voltage to turn on the device. So, you can get enhancement type of

devices with the MESFET by adjusting the doping or by adjusting the thickness or ultimately by adjusting the threshold voltage, you can get positive if I have a thick layer, then usually it will not be depleted with the built in potential in that case, it will be you have to apply negative voltage to turn off the device.

That is a depletion type. So, usually when they talk of the effect they talk of thick layers of the channel then it will be mostly depletion; depletion type of device, but today in the gallium arsenide integrated circuits they talk of enhancement type of device as the driving device and depletion type of device as the load device is a load resistance or le load device you can operate it at 0 bias by connecting gate to the source you can see there is a point of operation. So, you can use it as a 2 terminal device by connecting their gate and the source and use it as the load resistance and this is the driving resistance. So, n channel devices can be made integrated circuits are be made logic circuits using the gallium arsenide FET no that is we see few things before I close down today few items I want to (Refer Time: 45:51).

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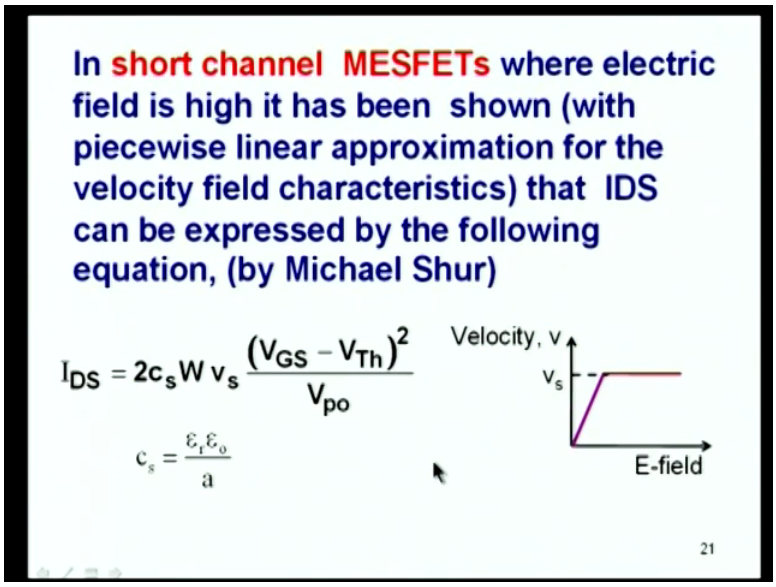

So, this is the characteristics when we using the assuming that the channel drain current saturates when the depletion layer pinches off at the drain end, but if the channel bits are short this can happen even before pinch off takes place because of velocity saturation. So, I will not go into the details of that, but you can approximate by approximating the velocity field characteristics in this fashion he know that it is not like this either it goes then saturates or it goes up and comes down again gallium arsenide.

But Michael Shur in his a paper way back and even in a loop, it is written he has shown that we make this approximation you can convert that particular equation. And you can write it in a form for short channel devices in this fashion ID saturation is you can see all those terms are there w; w is there, this is the c of s that is the capacitance of the channel silicon and L goes up when the velocity saturation takes place as just like in the case of the a MOSFET, because the mobility term gets absorbed in the velocity velocity saturation.

So, you get it is shown that you can write it in terms of this that is ID saturation is proportional to the channel capacitance that is the this quantity thinner that channel higher is the drain current thinner the current channel higher will be the trans conductance that is delta ID by delta IGS driving capability is better provided you have got enough careers there. So, that would actually need to increase the doping concentration also when they make the channel thickness smaller please that is changes slow.

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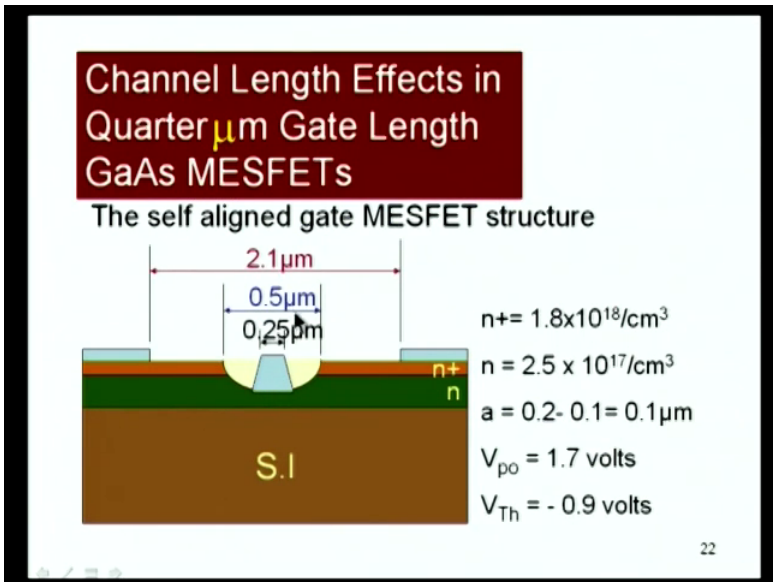

So, this is expression now this is deliberately drawn if I use velocity saturation as 10 to the power of 7 and if when I use this particular term which is a approximation to the entire characteristics saturating like this there is no velocity overshoot etcetera.

It goes on increasing saturates at 10 to the power of seven; that means, if I go to high field it is 10 to the power of 7 if I do that when I make a device do I get dual characteristics what velocities I will get do I get 10 to the power of 7 odd currents I get

what trance condense I get for some experiment people have done. So, to see how the channel length effects the quarter micrometer gate length gallium arsenide MESFETs people have made experiments see for example, here this is the whole thing is the channel length the green color there is the channel n region and this red color is n plus region on the top this is a semi insulating layer. And they have put the metal here ohmic contact is very easy to make ohmic contact on n plus region rather than on n; n region invariably they will have they should have n plus region there. Now I am not going to the technology of this, but what they have done is they have removed this material here ached this material they have ached this material it is a isotope aching removed this n plus layer removed this n layer also.

So, that the thickness of the channel is reduced originally what that; they started had n plus layer one 0.8 into 10 to the power eighteen. So, that even if you put a contact here at the end of this region it is very low resistance. So, when you apply voltage here I am sorry when you apply voltage here that is coming right up to this point because the drop across this region is negligible. So, whatever current is flowing which is collected here similarly whatever current injected here is injected into a channel here, but notice that there is some small gap between n plus and this because otherwise this you cannot have it connecting exactly touching this gate because then it will short. So, there are 2 things that they did it they wanted to study the effect of this n plus layer present.

Here with this n plus layer and without this n plus layer. So, this metal contact distance between them is 2.1 micron the portion where they achieved this n plus layer is 0.5 micron and this is actually the gate which is 0.25 micron is quarter wave it is this is quarter micro meter 0.25 micro meter gate; gate length channel length is more than the gate length means the contact ohmic contact is here n plus layer is here one plus layer here. So, you have a channel length which is more than the gate length 0.25 micron gate length 0.5 micron channel length. So, the thickness of this layer n layer was 0.2 microns, they have h 1 micron from here. So, that actual channel thickness is 0.1 micro meters. So, the pinch off voltage corresponding to this 0.2 micro meter thickness and dopping 1.81 po 2.5 into 10 to the power seventeen doping here is that is by using that formula qN D a squared by twice epsilon r epsilon 0.

You get that is a one point here 7 volts that is the pinch off voltage. So, now, what they did was they made the MOSFET with the n plus layer going all the way up to this point like this. So, in this case channel increase 0.25 microns gate length is 0.25 microns

suppose you h of this n plus layer from this end completely that is n plus layer is absent up to this point only in this point here just below this contact n plus then the channel length is from here to here that is 2.5 one micron. So, that second case is 2.1 micron channel length, but gate length is 0.25 micron. So, here we have got situation where one case channel length is 2.1 microns and in another case channel length is 0.5 microns in both cases gate length is 0.25 micron ok.

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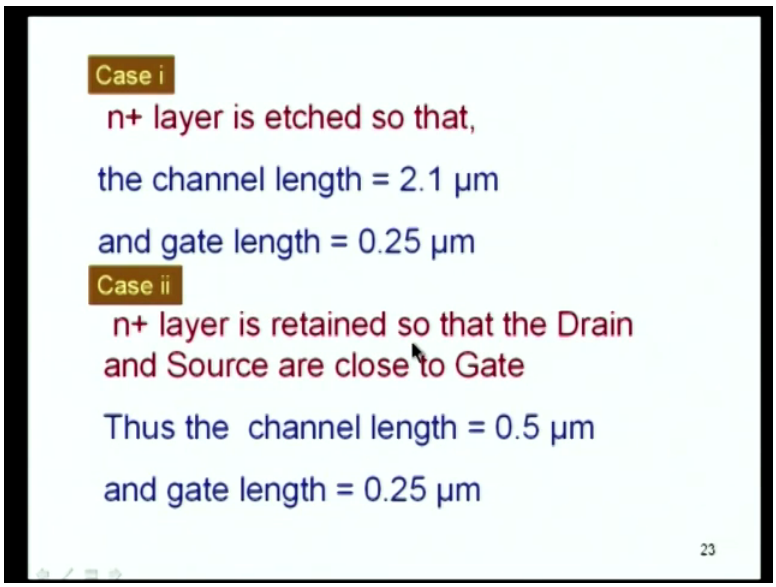

So, that is the situation they have done the case 2 n plus retained is one case is retained you retained n plus and the first case that is removed.

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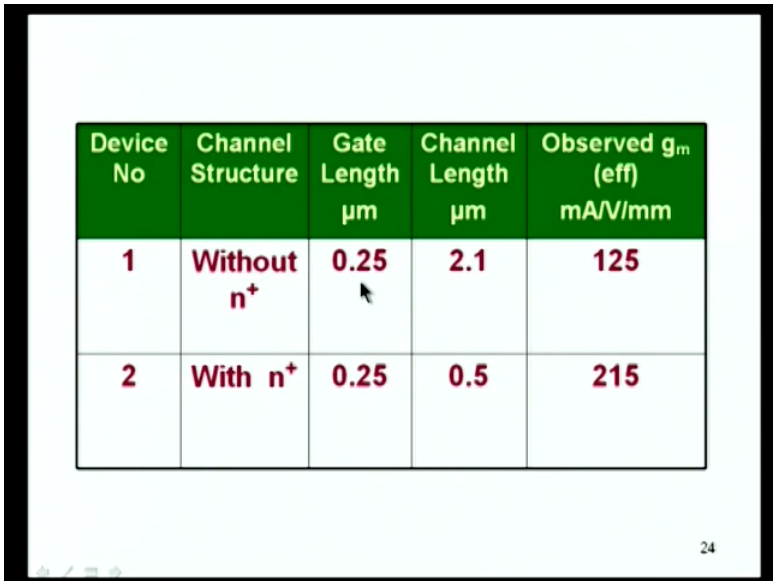

So, they made measurements on that without n plus that is no n plus layer channel length is 2.1 micron and gate length is 0.25 micron, they observed gm as 125 milli ampere per volt per millimeter channel width. Now when n plus layer was present and this layer was present they saw the gm was much higher obvious it just got to be higher because if the n plus layer is not present you have got lot of resistance from here to here as we discussed in the case of MOSFET.

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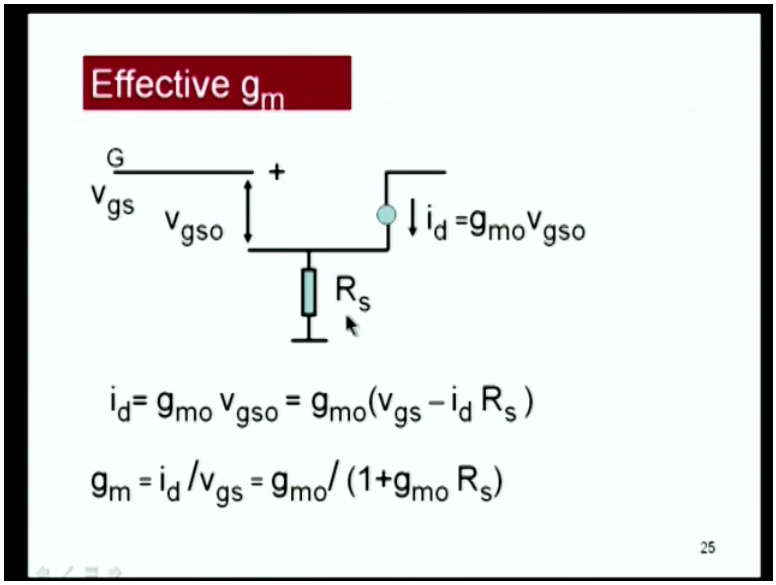

Using this equivalent circuit there is a resistance between the edge of the channel and a

source contact is a gate source contact that resistance is coming from here to this channel length when this layer is present resistance is only be small here when the layer is absent channel length 2.1 micron the resistance is higher. So, that is Rs including that you will have gm will be much smaller come because if the resistance is absent this is gm 0 if the resistance is present it will be gm 0 divided by 1 plus gm 0 Rs, it is consist in case of MOSFET also.

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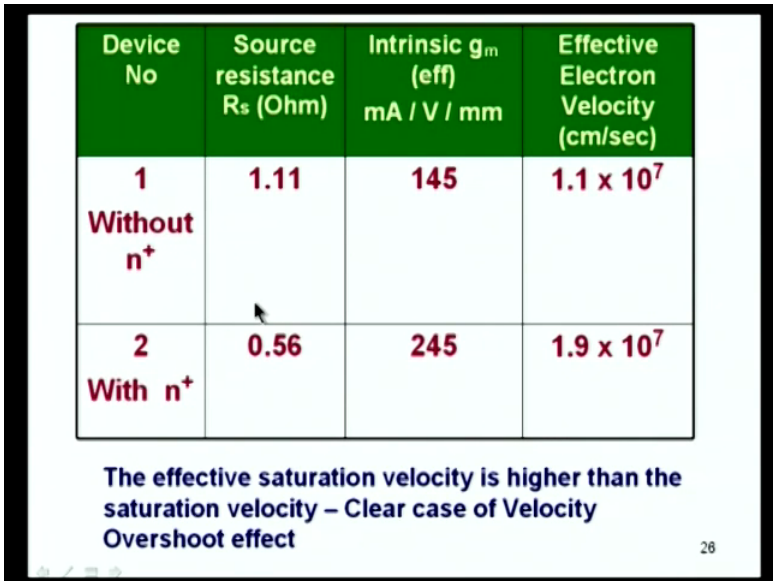

So, by incorporating this correction then they found incorporating this correction.

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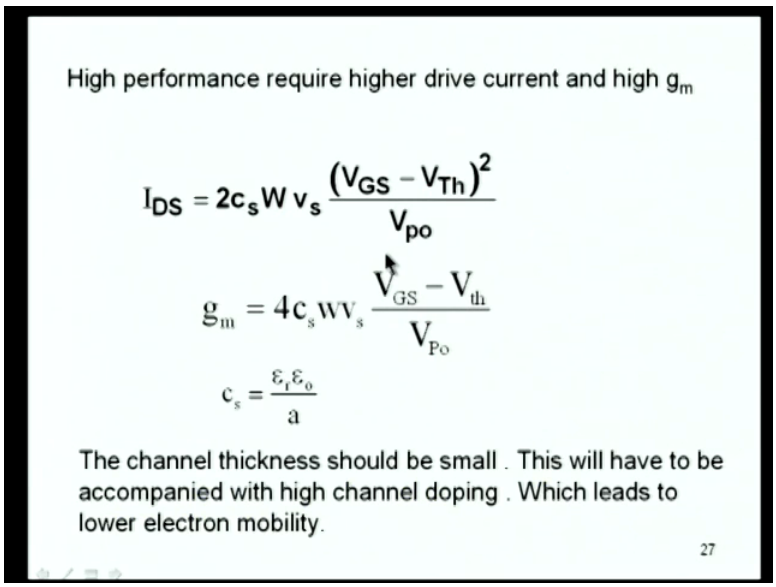

And using this equation gm is equal to this quantity they found of made the corrections and estimated the gm all these terms are known to you V GS V threshold VP 0 everything is known they calculated the V of s saturation velocity. So, they did that they found that without n plus they got velocity of 1.1 into 10 to the power of 7 after making the correction neglecting the resistance they got about 10 to the power of 7 saturation velocity, but with the n plus they got 1.9 into 10 to the power 7 this all that you do is measure gm substitute for all these known quantities VP 0 is known and find out sat velocity from that.

Since you have made correction for the resistor the difference in these 2 cases is when this is present careers are injected straight away into this channel very close by when n plus layer is present careers are injected into the high field region suddenly there they can go through the velocity overshoot effect where as if this layer is not present the carriers are injected here in to the channel by a time, it has reached here it has reached its steady state saturation velocity because there is a drop here.

So, when this n plus layer is not present the channel region here the under the gate region there is no velocity overshoot effect it has already reached the steady state value, but if this n plus layer is present the carriers are injected right here into the gate where the fields are high. So, it go through velocity overshoot effect. So, what we are telling is the result from that is with gallium arsenide if plus force region n plus is very close to the gate region careers get injected into the channel cold right away into the channel, it suddenly experiences the effect of high field and it experiences the velocity overshoot effect. And the average velocity is that effect in the channel is much higher than 10 to the power of 7 centimeter per second saturation velocity is 10 to the power of 7 that is almost twice you get trans conductance almost twice you get velocity it almost twice you get frequency is almost twice all that happens.

So, that is telling you that gallium arsenide devices definitely have the merit particularly when you go to even as small as channel length which are about 0.25 microns you can do that now the question is whether you can get self-arranged structure that has been reported I am not going to discuss that you can get very self-aligned; self-aligned n plus with respect to that you can get using tri layer gate structure bit more complicated. So, I am not discussing it right now because of shortage of time.

So, that is the story now what you are saying these if I have to have in summary gallium

arsenide has got high impact to get high velocity and high performance now if I want to get higher trans conductance you can get that short channel effect and increase the velocity saturation effective velocity it about twice center or 7, but for a given w V GS etcetera. I can increase the gm by increasing the capacitance that can be done by increasing the by reducing the channel thickness, but reduction in channel; channel should be accompanied by increasing dopping. So, that threshold voltage can be adjusted to the required value.

So, the ultimate thing is even here we are haunted by the problem of high dropping effect. So, what is the way to go? Use the modified structure, use gallium arsenide substrate where you can have carriers where there is no doping. That type of structure will discuss that is hetero structure devices and HEMPT. We will discuss in my next lecture.