

Nanoelectronics: Devices and Materials
Prof. K. N. Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture - 27

Germanium MOSFT technology and recent results on surface passivated Ge MOSFETS

So, we have had one session on non silicon based device that is Germanium based device. So, in this module 4, we continue on the germanium base device MOSFET and take a treatment to compound semiconductor materials and devices.

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Recent Results on the Germanium MOS Devices

- 1. Ge MOS cap: ozone oxidation + HfO₂ -Pt electrode (Stanford)-**
IEEE ELECTRON DEVICE LETTERS, VOL. 29, NO. 4, P 328, APRIL 2008
- 2 Ge MOSFET: Thermal GeO₂+ HfO₂ + Fluorine - TaN gate electrode + FGA (National University Singapore)**
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, P 1330, JUNE 2009
- 3. Ge PMOSFET: With 1-nm EOT Al₂O₃/GeOx/Ge Gate Stack Fabricated by Plasma Post Oxidation- TiN gate electrode (The University of Tokyo, Tokyo, Japan)**
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, P 335, FEBRUARY 2012.

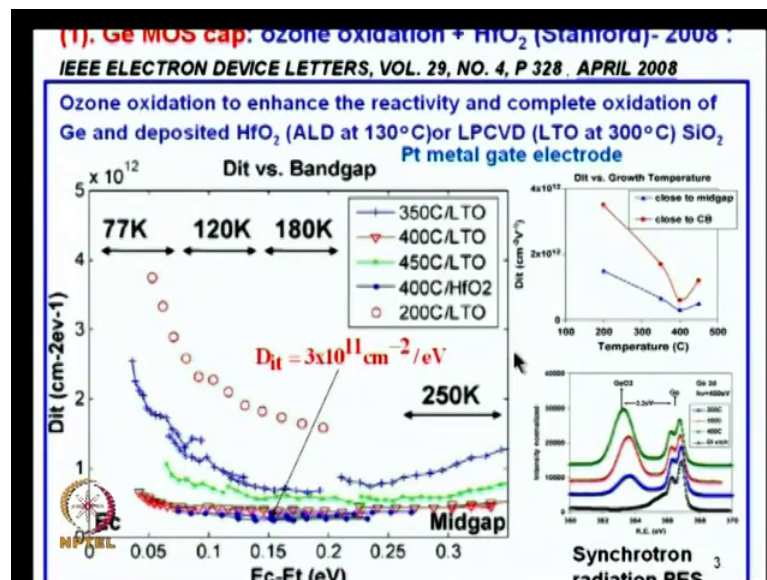
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So, we had seen what problems are involved in using Germanium for MOS devices. The most important thing that was required there was the surface preparation and what dielectric you will use originally it was believed that the germanium oxide should be completely removed from the surface. And then you have to do some passivation techniques like ammonia, passivation and possibly deposit high k dielectric. But later on it was clear, that it was not the germanium oxide which is giving problem. Germanium oxide indeed would help if you do proper stoichiometric oxide growth good quality germanium oxide and then do some passivation and deposit high k dielectric materials to make MOS devices.

In fact, I will show you in today's presentation 3 case studies or 3 approaches which have been tried out fairly successfully to realize p channel MOS devices using germanium. P channel is used because in germanium the effort is to realize p channel MOSFET, because the whole mobility in germanium is the best as compare to the silicon or gallium arsenide or indium phosphide. So, we will take a look at this 3 cases, first one is the one that was done in the Stanford with Saraswat group. Germanium MOS cap using ozone oxidation which I have discussed last time just I will point out today, all that is ensure there is complete oxidation of germanium oxide using o 3 that is ozone. Then use hafnium dioxide, hafnium oxide as high k dielectric, platinum electrode.

Second approach is again thermal oxidation with this was reported in 2009. We will finish the first one and go to second one germanium MOSFET that was from Singapore in 2009. This involved thermal oxidation of germanium oxide, hafnium oxide, use of fluorine for passivation and tantalum nitride electrode and forming gas annealing, we will see that details. Third one is the germanium MOSFET with Al₂O₃ germanium oxide and germanium gate we see them one by one, this one what we seen last time itself.

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Here what we showed was what we had shown by Stanford group was that use ozone, oxidize germanium freshly cleaned surface, oxidize is at different temperatures 200, 350, 400 and 450 and in each case first what they did was 200, 350 and 400, they did

oxidation and deposited low temperature oxide that is LPCVD, Si O₂ at 300 degree centigrade. So, they found this gave MOS capacitance with the D it which went on reducing as you increase the temperature of oxidation 200 at is the D it across the band gap. So valance band gap right up to mid gap went up to 350 still they went on 400, it went on further this red circles.

Now, when they went to 450 that became worse telling you that you can do the oxidation of germanium at higher temperature with ozone, it gives better results with hafnium oxide as the high k dielectric, but the result gets interface state density becomes worse you can see it goes on reducing then above 450 it increases, telling you that germanium oxide begins to decompose at high temperatures. So, you have restrict to 400 degree centigrade.

Now, what they did was choose 400 degree centigrade for germanium oxidation with ozone instead of silicon dioxide use hafnium oxide by atomic layer deposition at 130 degree centigrade that gave them the best interface state density as low as 3 into 10 to power 11 centimeter square per electron volt.

So, these are various technique measured and the lowest interface state density fold it in that there is no MOS effect by itself reported in that report. Subsequently they have reported something, but we will take on some other approach instead of using ozone.

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(2) Ge MOS devices: GeO₂ + HfO₂ + Fluorine passivation

Rullong Xie et al, "Inteface Engineered High mobility High k/Ge pMOSFETs with 1nm EOT" IEEE TED-56, pp.1330-1337, June 2009

- HF (1 : 50) dilution and DI water cyclic rinsing of n-Ge ,
- Thermally **Grow 2nm GeO₂** layer at **400°C** .
- **4.5nm HfO₂** layer at 300°C by ALD using Hf[N(CH₃)(C₂H₅)]₄ precursor and H₂O.
- **Incorporate F** into some samples by **CF₄** plasma treatment in ICP chamber with pressure of 100 mtorr and mixed flow of **CF₄** and **O₂** gases with a ratio of 10 : 1 (varied durations)
- **PDA at 500° C for 30 s** for all samples.
- **Ta** metal electrode formation.
- **Forming Gas Anneal (FGA) at 350°C for 1h** on some

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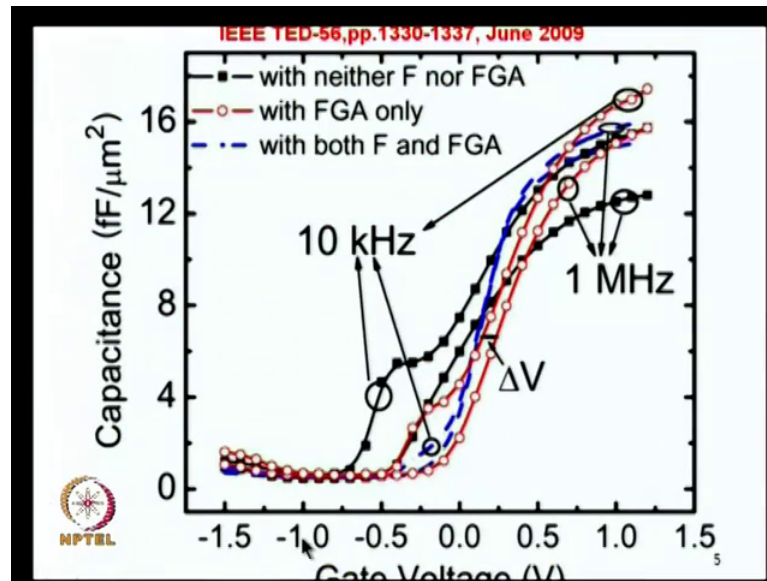
The approach is done by Singapore that is using germanium MOS devices with GeO_2 and high k dielectric hafnium oxide that also atomic layered deposit. But what they used is they use regular thermal oxidation at 400 degree centigrade, because it does not decompose at that temperature. So, 2 nanometer of thermally grown germanium oxide was grown. And then using atomic layered deposition at 300 degree centigrade hafnium oxide layer of 4.5 nanometer was deposited on the germanium oxide ok.

Now, once we have this double layer of hafnium oxide and germanium oxide on germanium. Incorporate fluorine into some samples because they did various experiments in some of them they incorporated fluorine by CF_4 plasma treatment in inductively coupled plasma chamber ICP with pressure of 100 millitorr. And a mixed flow of Freon and oxygen that means, you have fluorine passivation taking place at the same time some amount of oxygen is supplemented to keep the oxidation on and for various duration they did that CF_4 treatment.

Followed in this they did a post deposition anneal PDA at 500 degree centigrade for 30 second for all the samples. So, in some sample they did not do this fluorine treatment, but in some of them they did that followed by the PDA was done on all the samples. Then tantalum nitride metal electrode formation for the gate finally they did forming gas anneal FGA at 350 degree centigrade for 1 hour on some of them. So, forming gas is hydrogen plus nitrogen combination.

So, you can see that there are double passivation that have been done. One is native germanium oxide is present, hafnium oxide has the gate dielectric, then you have got the fluorine passivation and then you have got the hydration and passivation in forming gas, different combination have been tried out. Here are the results.

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These are the capacitance voltage characteristics taken on these devices for example, just only the germanium thermal oxide and hafnium oxide and tantalum nitride and with only PDA, no forming gas annealing, no fluorine passivation. When they did that this black squares show the C-V characteristics at 1 megahertz and this upper curve shows the frequency response in 1 kilohertz.

So, telling you that there is frequency depression of the C-V characteristics as you go to higher frequency, the capacitance falls indicating that there is and when you go to lower frequency capacitance is higher indicating that there is response of interface state taking place to these frequencies. So, the presence of high frequency is indicated by the frequency dispersion as you already know.

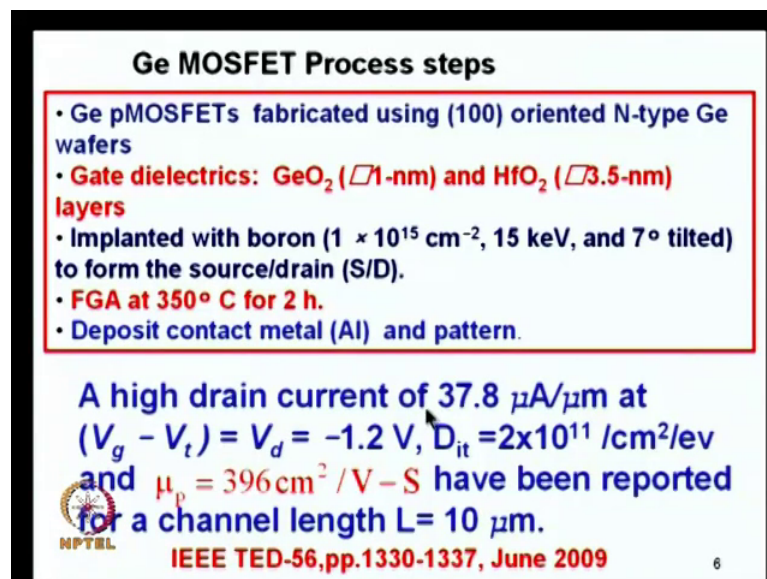
Now, the red curves two of them one at 1 megahertz to lower curve. The upper curve is at 10 kilohertz, this is the 10 kilohertz, and this is at 1 megahertz. So, here again you can see only the fluorine passivation was not done only their forming gas annealing was done; that means, hydrogen passivation was used using the forming gas. The capacitance was higher, it showed better results but still there was frequency response, frequency dispersive. There is some stretch out effect is still you can see when there is no FGA or fluorine the stretch out is more when you use the forming gas anneals stretch out is reduced. Now in both fluorine plasma annealing and forming gas anneal this is stretch

out if you steep stretch out has disappeared indicating that the interface state density is drastically reduced and very little frequency dispersion is seen.

So, combined effect of fluorine passivation with CF4 plasma and hydrogen passivation with the forming gas anneal did the trick for them a really reducing the interface state densities and to get excellent c_v on the p type substrate, I am sorry on the n type substrate. Because in n type substrate when you apply minus voltage just one minute this was actually the starting material was if I have n type substrate and I apply plus voltage it is accumulation, when I apply negative voltage it is depletion. So, this is the inversion this is n type substrate, p channel device inverse at with p channel.

So, I am sorry I am again making a mistake, n type substrate inverted p channel, negative voltage holes are attracted surface, so inversion layer is p. So, you have got p channel device using n type substrate ok.

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Ge MOSFET Process steps

- Ge pMOSFETs fabricated using (100) oriented N-type Ge wafers
- Gate dielectrics: GeO₂ (□1-nm) and HfO₂ (□3.5-nm) layers
- Implanted with boron ($1 \times 10^{15} \text{ cm}^{-2}$, 15 keV, and 7° tilted) to form the source/drain (S/D).
- FGA at 350° C for 2 h.
- Deposit contact metal (Al) and pattern.

A high drain current of 37.8 $\mu\text{A}/\mu\text{m}$ at $(V_g - V_t) = V_d = -1.2 \text{ V}$, $D_{it} = 2 \times 10^{11} / \text{cm}^2/\text{ev}$ and $\mu_p = 396 \text{ cm}^2 / \text{V-S}$ have been reported for a channel length $L = 10 \mu\text{m}$.

IEEE TED-56, pp.1330-1337, June 2009

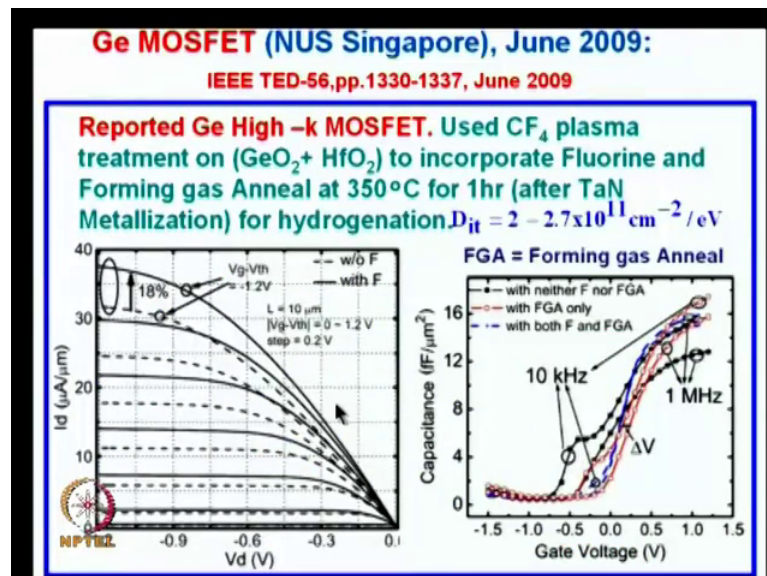
Germanium MOSFET process steps germanium p MOSFET are fabricated using n type germanium as it is a origin state that if you want to make p channel device N-type substrate must be used. So that was the MOS cap or the MOSFET were fabricated by using 100 oriented N-type germanium wafers. Gate dielectrics, germanium oxide 1 nanometer, hafnium oxide 3.5 nanometers layers implanted with boron 10 to the power 15. These are a source drain see gate oxide is grown by germanium oxidation and of course the plasma passivation etcetera and hafnium oxide 3.5 nanometers.

Source drain was formed by for making the MOSFET by implantation of boron, because the p channel MOSFET, source is p and drain is p. Then plasma passivation was done forming gas annealing was done at 350 degree centigrade for 2 hours, 350 degree centigrade. Deposit contact material aluminum and pattern.

So, now a high drain current of 37.8 micro ampere per micro meter at V_g minus V threshold equal to minus 1.2 volts you can see that the gate voltage is negative and you have positive holes in a channel minus 1.2 volts, it gave quiet high den current 37.8 micro ampere micrometer and the interface state density of 2 into 10 to power of 11 per centimeter square electron volt, I do not say that it is negligible. But it is very small that is reported. And the mobility of 396 centimeter square per volt second have been reported for n channel, channel length equal to 10 micro meter.

Now, you may ask how good is this mobility this mobility was at the time it was the best that is reported on germanium. Earlier they got even you know worst mobility because of the high interface state density. But the ideal mobility that can be achieved for p channel germanium MOSFETs is expected to be 1900 centimeter square per volt second we are far off still ok. So now these are characteristics.

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For germanium MOSFET from NUS, National University Singapore June 2009 transaction (Refer Time: 15:44) this picture is taken from there 2009. Germanium high k MOSFETs using CF_4 plasma treatment, germanium oxide plus hafnium oxide dielectric

incorporated Fluorine and finally anneal in forming gas at 350 degree centigrade for 1 hour after the tantalum nitride metallization ok.

The d it of 2 into 10 to the power 11 per centimeter square per electron volt was observed after hydrogenation. We can see the characteristic here without the forming gas annealing, without the fluorine, without the fluorine passivation plasma the dotted line gives the current for $V_g - V_{th}$ equal to minus 1.2 volts. And for the same condition but with fluorine if you are done this fluorine passivation you get much higher current. What was about 30, 32 micro ampere per micrometer went up to about 37, 38 micro ampere or micrometer gate width. In the same way micro ampere per micro meter implication is micro ampere per micro meter of channel length, channel width.

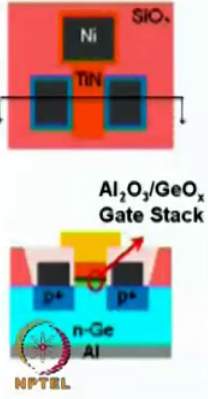
So, this tells us that with this indeed gives us the impact of fluorine passivation to enhance the current, to enhance the mobility. We will see that subsequently for sometime not much improvement has been done.

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(3). High-Mobility Ge pMOSFET: 1-nm EOT $Al_2O_3/GeO_x/Ge$ Gate Stack Fabricated by Plasma Post Oxidation

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, NO. 2, FEBRUARY 2012

Process steps:



- Al_2O_3 layer deposition by ALD at 300°C using TMA and H_2O precursor.
- Plasma Post oxidation by exposing Al_2O_3/Ge structure to oxygen-assisted plasma at Substrate temperature of 300°C.
- Post Deposition Annealing at 400°C. TiN (Titanium Nitride) electrode formation and patterning.
- Source drain Ion Implantation. Activation at 400°C, 3min.
- Nickel G/S/D contact formation. Back contact with Al

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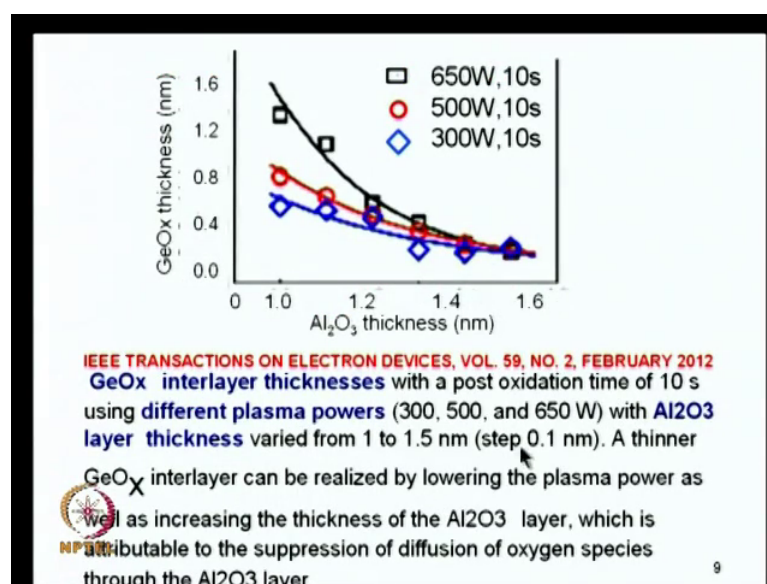
But in the latest one February 2012, there was a report in the transaction in the electron devices. February 2012 a group from Japan they reported the use of instead of hafnium oxide use Al_2O_3 layer as the dielectric. They did not used straight away the thermal oxidation, but they showed that you can grow germanium oxide in between the Al_2O_3 and the germanium by annealing at 300 degree centigrade in a plasma after depositing Al_2O_3 .

So, the way I did was deposited first clean the surface of course that is important. Deposited after cleaning the layer at Al₂O₃, Aluminum oxide by atomic layer deposition at 300 degree centigrade using tri methyl aluminum and h₂O precursor, TMA tri methyl aluminum that is the common thing that used. And then cut the wafer at 300 degree centigrade, subjected the wafer to post plasma oxidation by exposing the Al₂O₃, germanium stack. So oxygen associated plasma at substrate temperature of 300 degree centigrade.

So, what it does is the oxygen from the plasma defuses into the interface and oxidizes the germanium that means you are getting that germanium growing as a intermediate layer and always protected by the Al₂O₃ layer. So, after this deposition they did the post deposition annealing at 400 degree centigrade, titanium nitride electrode formation and patterning that makes MOS structure.

Source then also that is the structure there where there is a oxide, there is the field oxide. Source drain was implanted by p plus implantation activation is 400 degree centigrade for very short duration. We can see a transaction structure here this is the top view, gate, source drain that is the Nickel, gate, source and drain. Nickel, gate, source and drain contacts formation and the back contact aluminum. They got the source, gate and drain. Gate stack is Al₂O₃, germanium oxide dielectric. So, let us see how it works out.

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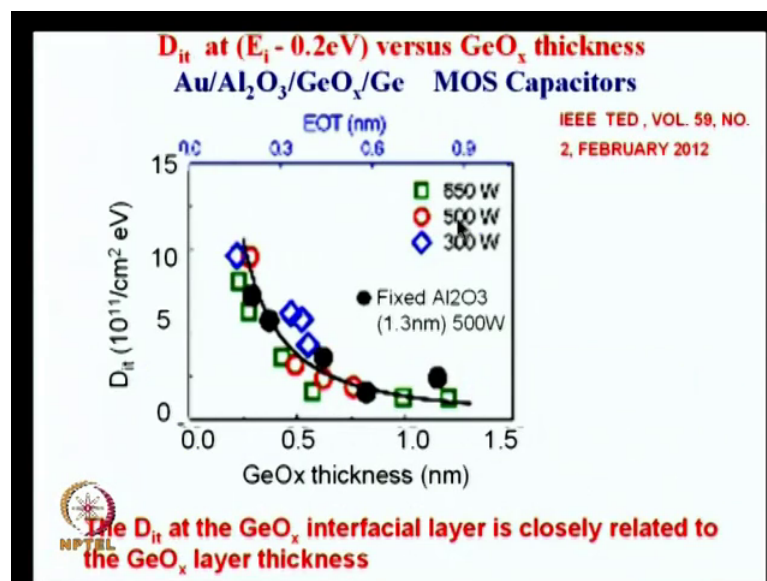


What they saw was they are able to control the thickness of germanium oxide you can vary it from 0 to 1.5 nanometers either by fixing the aluminum oxide for a particular thickness say here fix it at 1 nanometer Al₂O₃. Then subject it to that oxygen plasma at 300 watts you get about 0.5, 0.6 nanometer germanium oxide. 500 you get more oxide, 650 will they get about 1.3 or 1.4 nanometer, so if it 1 nanometer fixed more power you get more oxygen atoms diffuse through the Al₂O₃ layer.

Alternately for a given power 300 watts, you have to make each for each one you have to make different samples you have a thinner aluminum layer. If you have thinner aluminum layer or thicker aluminum layer see this is 1 nanometer, for the 300 watts if we have 1 nanometer aluminum layer you get about 0.5 nanometer germanium oxide inter intermediate layer. But if I reduce if I increase the Al₂O₃ thickness to 1.6 or 1.5 nanometer you can see the germanium oxide thickness is very small much smaller than about 0.1 nanometer.

So, you can have a perfect control of the germanium oxide thickness either by changing the power r f power of the plasma or same plasma or by choosing a different aluminum thickness, thinner thickness of aluminum Al₂O₃, more is the thickness of the germanium oxide so you can get good control. Now what they did?

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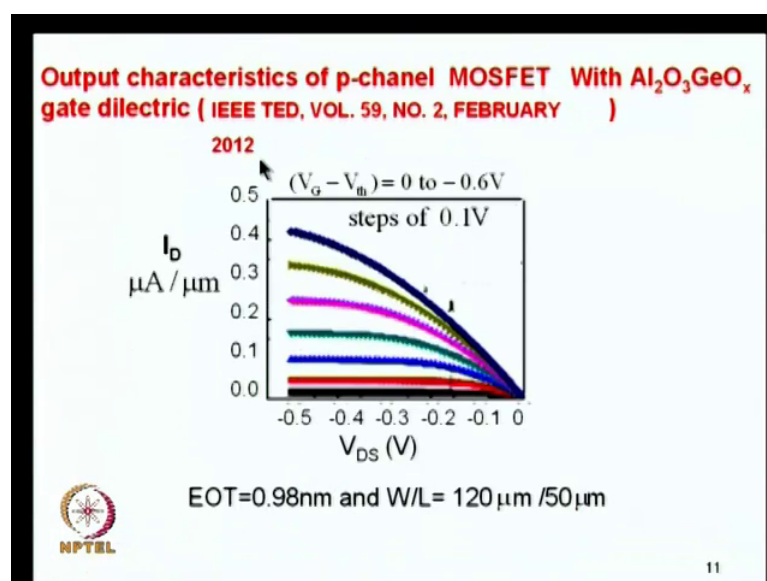
They measured made MOS cap near they got the MOS cap. They made measurements on that and obtain the d_{it} for different germanium oxide thickness of by using the approach.

They made gold Al₂O₃, germanium oxide, germanium, MOS caps and measure the interface state density at 0.2 electron volts below the band gap ok.

Because you can it gives an idea that is the minimum that you get at that location. At that point how much is the d it they got 10 to the power of 12 when the germanium oxide was 0 only Al₂O₃ present. But it went down to well below about 10 to the power of 11 or so by the time you went to 0.5 nanometers, 0.1 nanometer etcetera you went got even below 10 to the power of 11 centimeter square per electron volt. This was done by element Al₂O₃ of about 1.3 nanometers and 500 watts that tells you that you can get best interface state density by introducing inter layer germanium oxide, through the oxidation of the germanium by the oxidation of germanium using plasma oxidation through the Al₂O₃ layer which is deposited already.

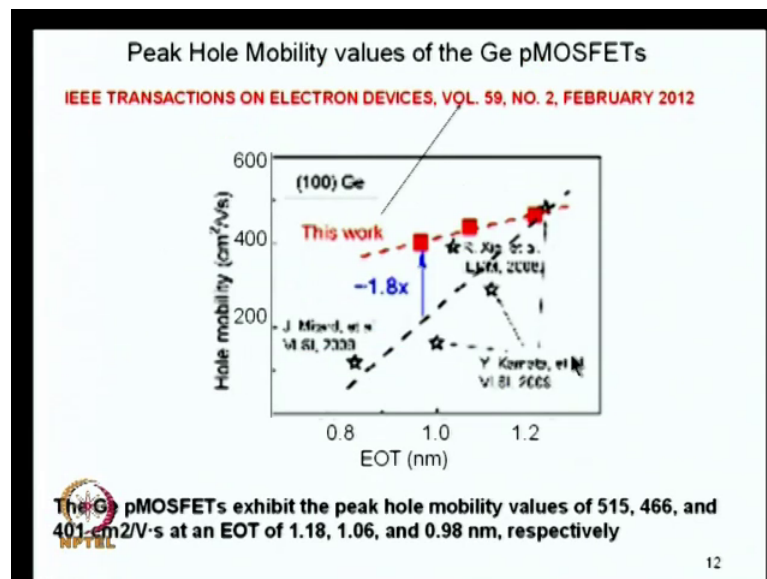
So, that was it also said that there is one to one correspondence between the germanium oxide thickness and d it and germanium oxide thickness controls the d it very much. You should not have if you have very thin layer of germanium oxide you will get or 0 we will get high d it, as you keep on increasing germanium oxide say about 1 nanometer you get very small d it so about 1 nanometer of the germanium oxide is optimum. They have not studied the fluorine effect on this, but they saw the output characteristics of the p channel MOSFET with Al₂O₃ germanium oxide gate dielectric with gold electrode.

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They got very good I V characteristics you can see that $V_g - V_{th}$ varies from 0 to minus 0.6 volts, very low voltage. They have got current of 0.4 micro ampere per micrometer and the drain voltage was 0.5 volts current is saturating yes it is saturating here and steps of 0.1 volts 0, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6 minus of course current from 0 right up to about 0.4 micro ampere per micrometer. So this was EOT effective oxide equivalent oxide thickness of 0.98 nanometer W by L equal to 120 micrometer and 50 micrometer channel lengths.

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And they also measure the mobility from this I V characteristics, estimated the mobility and they showed that the germanium p MOSFET exhibit the peak hole mobility values of 500 and 15 centimeter square per volts second when the EOT of 1.18 is used there. EOT of 1.18 that gives about 515 that is highest ever reported for germanium p channel MOSFET.

And you can see and they used EOT of 466 that was about I am sorry and the EOT was 1.06 that was about 466 mobility. And when reduced to 0.98, that turned out to 400 so as predicted here thicker the EOT you get smaller the d it and thicker the EOT higher the mobility.

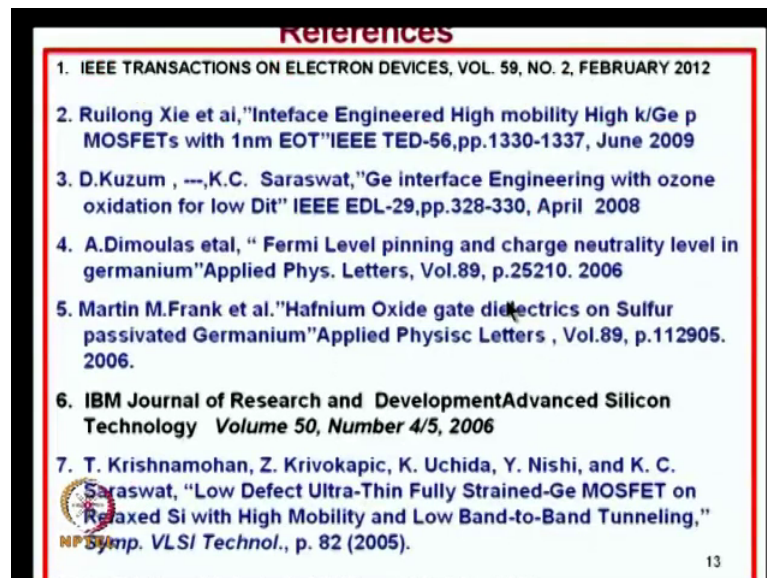
So, the mobility enhancement is correlated with the interface state density that is a implication of that. Obviously, the moment you have the interface state density when you

try to invert it and when you change the gate voltage. The channel charge would change if the interface state density is 0 channel charge would change correspondingly.

But if the interface state density is present, that will respond to the change in the gate voltage. Therefore, the channel charge will not change correspondingly. As a result, the drain current change will not be that much, so trans conductance will be smaller.

So, it is important to have the interface state density reduced drastically. So, this tells you that there is still some interface state density present there. There is still lot of scope to go ahead with that.

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Now you can see that in all these cases it has been this is summary of these references that you have chosen before I closed on our discussion on germanium 2012, 2009, 2008 starting from the entire millennium lot of effort has gone on germanium transistors.

There is still long way good to go and people have not been looking into n channel MOSFET because that is not an issue. Because you can get we can somehow you know you are concerned about realizing p channel MOSFETs with the high hole mobility. So, one can think of combination of silicon and germanium silicon germanium devices or silicon n channel MOSFET, p channel germanium MOSFET combination of those things

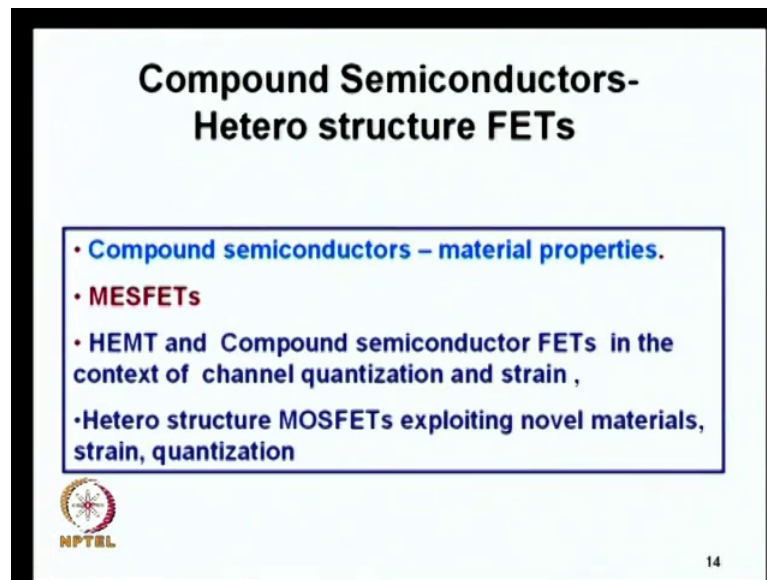
to make my CMOS all sorts of combination can be are force in are looked into recursively by various industry people.

So, one can move from here on not only silicon but not only silicon or germanium which are the elemental semiconductors. One can take a look at compound semiconductors like silicon, germanium for example, it is a compound semiconductor you can look that is the silicon is forth group. Germanium C is forth group. So, silicon germanium is 4, 4; 4 4; group both elements are from forth group, but it is a compound. You can make silicon and germanium in any composition to you can change the band gap from germanium to silicon, germanium is 0.66, silicon is 1.1, electron volt at low temperature.

Now, you can make an alloy of silicon germanium have a band gap of your choice, have a mobility of your choice. When you mix no doubt you get the benefit of better band gap with when you add silicon to germanium but you lose the benefit of higher mobility. So, you may have to hit a compromise then if you are using silicon germanium. On the other hand you can think of germanium which is strained so that a thin layer of germanium. So that you can improve the band gap still have high mobility. These are some other issues which we can look into.


So, if you are thinking of look into compound semiconductors. Now you can see already in silicon you are looking at high k. So in compound semiconductor in germanium in all this devices you are looking to high k dielectric more and more high k dielectric like hafnium oxide or Al₂O₃ by atomic layer deposition are being vigorously tried out in all approaches. Now let which clears therefore take a look at into the move on into the world of compound semiconductors and the hetero structure FETs.

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**Compound Semiconductors-
Hetero structure FETs**

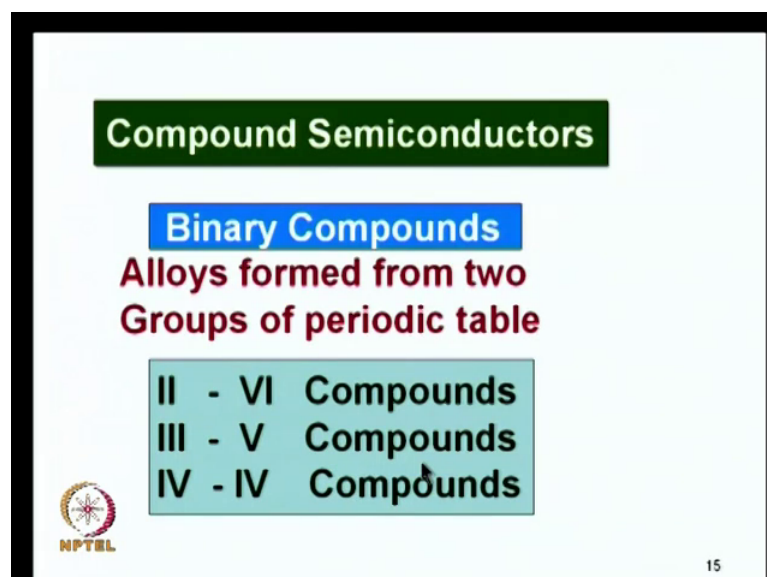
- **Compound semiconductors – material properties.**
- **MESFETs**
- **HEMT and Compound semiconductor FETs in the context of channel quantization and strain ,**
- **Hetero structure MOSFETs exploiting novel materials, strain, quantization**

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So, what you see here will be today quickly take a look at compound. What are the materials and what are their properties. Then take a look at MESFETs very briefly. Then go to high electron mobility transistors and compound semiconductor FETs in the context of channel quantization. If possible I can also look into we can also look into hetero junction by power transistor. Hetero structure MOSFETs exploiting novel materials, strain, quantization.


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Compound Semiconductors

Binary Compounds
**Alloys formed from two
Groups of periodic table**

II - VI	Compounds
III - V	Compounds
IV - IV	Compounds

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Now, as I already mentioned compound semiconductors can be Binary. Binary means there are 2 compounds, ternary means 3 compounds, quaternary means 4 compounds, so you can have combinations. So, binary you can have elements from second group and sixth group they are called 2-6 compounds. Elements from third group and fifth group they are called 3-5 compounds.

Here for example, Cadmium sulphide second group and sixth group. Here gallium and arsenic gallium arsenide first group third group and fifth group. 4-4 silicon and germanium that is 4-4 compounds or silicon and carbon silicon carbide these are binary compounds. Let us take a look at the 2-6 what are they?

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II Group Element (Atomic Number)	VI Group Element (Atomic Number)
Zn (30)	S (16)
Cd (48)	Se (34)
	Te (52)

Compound formed by second group and sixth group. Second group zinc and cadmium, these are the material which have been tried out, zinc these numbers are inside I given you atomic numbers just for some guideline. Because general it has some implications, I will come back it to later. Zinc and cadmium can form compounds with sulfur, selenium or tellurium from the sixth group. You can have zinc sulphide, zinc selenide, zinc telluride, so you can see 3 compounds, then cadmium sulphide, cadmium selenide, cadmium telluride.

These are all high atomic number materials, mostly when they are atomic materials they turn out to be direct band gap semiconductors. What are the implication we will see that later, they are direct band gap means the momentum of electrons at the conduction band

edge and at the valance band edge are same, are equal. There can be transition from conduction band to the valance band, electron transition from conduction band to valance band.

Similarly transition from valance band edge to conduction band edge by the help of photons that is only energy conservation is required for transition. So, directly it can transition can take place with exchange of energy with photons. They are called direct band gap semiconductors.


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II - VI Compounds (Contd)

ZnS	CdS
ZnSe	CdSe
ZnTe	CdTe

All of them exhibit direct Band gap

**All of them have $E_g > E_g$ of Silicon
However, $\mu_n < \mu_n$ of Silicon**

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Now 2-6 compound as already mentioned, zinc sulphide, zinc selenide, zinc telluride, cadmium sulphide, cadmium selenide, cadmium telluride. All of them exhibit direct band gap because of their nature of heavy atoms without getting into the peaks of that the high atomic number elements from their compounds usually they turn out to be direct band gap that is an observation it is all.

All of them have E_g higher than E_g of silicon all this compounds but all of them have mobility lower than that of silicon electron mobility. So, normally we would not like to take a look at them for micro electronics or nano electronics because of this problem. Still it can be useful for up to electron implications.

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III – V Compounds
Compounds formed by III group and V group elements

III Group Element (Atomic Number)	V Group Element (Atomic Number)
Al (13)	P (15)
Ga (31)	As (33)
In (49)	Sb (51)
	N (7)

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3-4 compounds, as I pointed out elements from this third group. These compounds are formed by third group and fifth group elements, they are compounds compute call it as alloys also, but correct term is call it as compound. Third group what are the elements, valance electrons are 3 in them aluminum, gallium, indium, atomic number 13, 31, 49. Fifth group elements phosphorus, arsenic, antimony, nitrogen you can see that these are all fairly high atomic number. Phosphorus is lower atomic number.

So gallium phosphide forms an indirect band gap. Gallium arsenide direct band gap, gallium antimonide direct, gallium nitride direct band gap, these are direct, this is indirect. Indium higher atomic number it forms direct band gap on all of them. Aluminum form direct band gap, indirect band gap most of them, because it is low atomic number or light material light atom that is an observation ok.

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III - V Compounds

AlP (I) AlAs (I) AlSb (I) AlN (I)

GaP (I) GaAs (D) GaSb (D) GaN (D)

InP (D) InAs (D) InSb (D) InN (D)

I = Indirect Band Gap
D = Direct Band Gap

GaAs, InP and GaN have μ_n and E_g greater than Si

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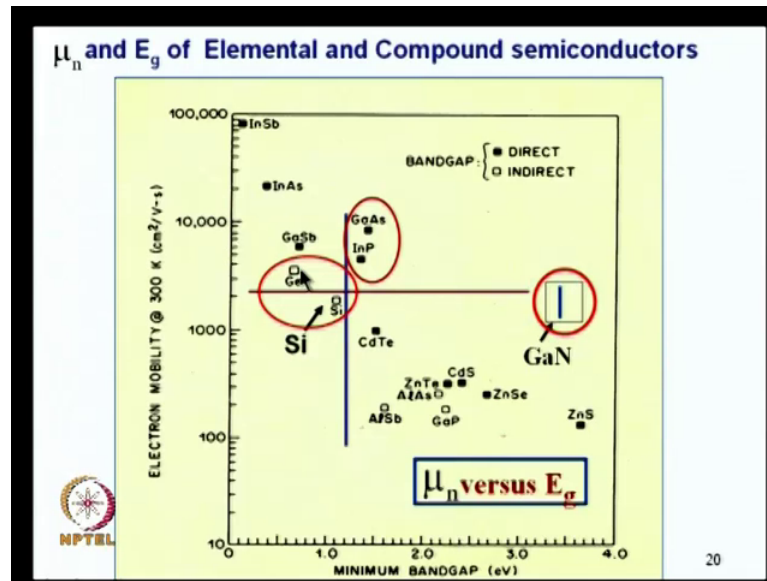
So, sum up aluminum phosphide, aluminum arsenide, aluminum antimonide, aluminum nitride all they are indirect band gap. Because of low atomic number associated with aluminum. Gallium phosphide is indirect because phosphorus is lighter than the gallium arsenide, gallium antimonide, gallium nitride are all direct. Indium phosphide, indium is heavy element all of them are direct, indium phosphide, indium arsenide, indium antimonide, indium nitride all are direct.

And I have circled these 3 materials gallium arsenide, gallium nitride, indium phosphide. They all have mobility and band gap greater than that of silicon. Electron mobility we are not talking of whole mobility, because none of them have whole mobility better than that of silicon, that only germanium can save us.

So, in case when I have to really have high whole mobility one has to look into the base of introducing germanium also into the galaxy of these semiconductors. So I is indirect here, D is direct band gap.

Now, these are binary compounds 2-6 3-5; binary giving a pointer towards gallium arsenide, indium phosphide. Lot of effort has gone into gallium arsenide and indium phosphide material and devices in the 1990s and 1980s and 90s still there is work going on in that. They are been used in the (Refer Time: 41:38) junctions rather than MOS cap. The compound semiconductor people have found a way out to sort out the problem of the high interface state density using hetero structure.

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So, this is the famous graph which gives you electron mobility at 300 Kelvin on the y axis 100, 1000, 10000 etcetera and on x axis the band gap. Minimum band gap meaning actually energy band gap actually, because there are different band gaps but the minimum band gap is that the actual band gap.

So, band gap is given on the x axis because we are looking at an alternates or silicon. So, material that we look forward to must have if possible better band gap than silicon that means to the right hand side of this graph that is better band gap and to the upper half of above this line horizontal line that is higher mobility.

Take a look at Indium antimonide, what mobility it has got 100, 1000 centimeter square per volt seconds. But you can see the band gap something like about 0.1 or 0.11 electron volts, absolutely no way of using it more of micro electrons. What about indium arsenide 20000 centimeter square per volt second, but you can see then band gap is very very small something like 0.3 or 0.4 electron volts no way you can use it.

But take a look at gallium antimonide that I got better mobility. But the band gap is also lower than that of silicon, one can think of doing that prepare it the hole mobility there is better. But actually the hole mobility is there is not good enough, I dont have the plot here right now, I can make it to some other time.

Germanium you see it is band gap is lower compare to that of silicon we already know but mobility is better. In fact which has got better hole mobility that is why I just circled those 2. Take gallium arsenide, higher mobility, higher band gap, indium phosphide, higher mobility, higher band gap compare to silicon. Those are the materials look forward to.


Now, you can think of making there is one more material gallium nitride which has come up the past decade it does catch up like anything, everywhere there is absolute to push gallium nitride. The best mobility that is the predict is about 2000 centimeter square per volt second fine. But look at the band gap something like 3.3 electron volts it can be use for high power high frequency etcetera.

In fact, when you go around you will see that the saturation velocities of electrons are very very high here. If I am looking it high field operations that will be a material one can look into compare to any other material, but it is a very difficult material to work on very costly material right now I am sure this will problems have been sorted out. There is a lot of effort going in this direction.

So, now let us just take a look at this particular thing again once again here. I can have combination of gallium arsenide and indium arsenide, see gallium arsenide has got higher band gap than that of silicon, indium arsenide has got much higher electron mobility I mix them together I can that is, I can replace some of the gallium atoms with indium atoms I get gallium indium arsenide that is ternary. Three elements forming the compound gallium, indium, arsenide that we will have band gap varying linearly from here to there that will be low band gap here. But we can still have a band gap with closed silicon and you can still have much higher mobility compare to that of silicon. So, one can think of or one is thinking of combinations of binary compounds to realize ternaries. Let us see further.

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IV - IV Compounds	
Compounds formed by two IV group elements	
IV Group Element (Atomic Number)	IV Group Element (Atomic Number)
Si (14)	C (6)
	Ge (32)

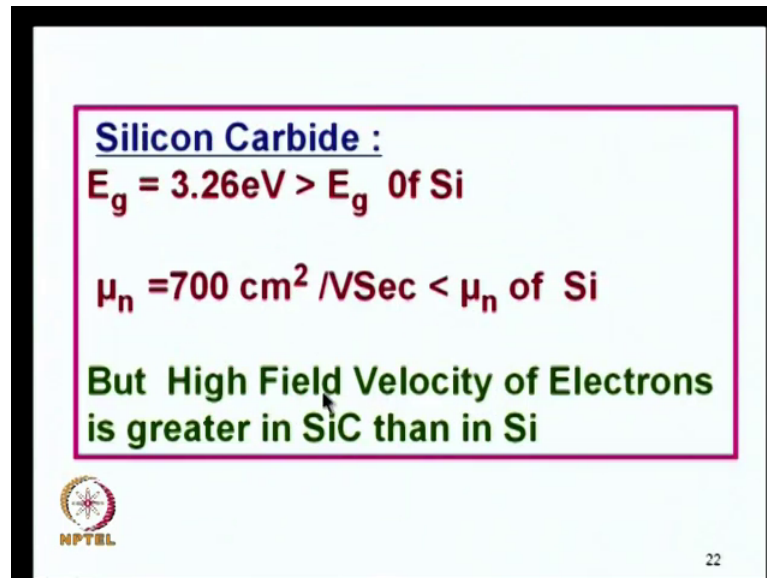


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4-4 Compounds no they are looking into 3-5 etcetera. What are the 4-4 Compounds? Silicon, carbon, germanium, silicon germanium, silicon carbide, silicon is indirect band gap, germanium is indirect band gap. So, silicon carbide silicon germanium both are indirect band gap semiconductors and your band gap will be somewhere in between the 2. Silicon carbide of course, has got much higher band gap about 3.5 electron volts. So, this silicon carbide is a material which has drawn attention of people working on high power devices because of wide band gap.

Similarly gallium nitride has drawn the attention of people who work on high power high frequency devices micro devices.

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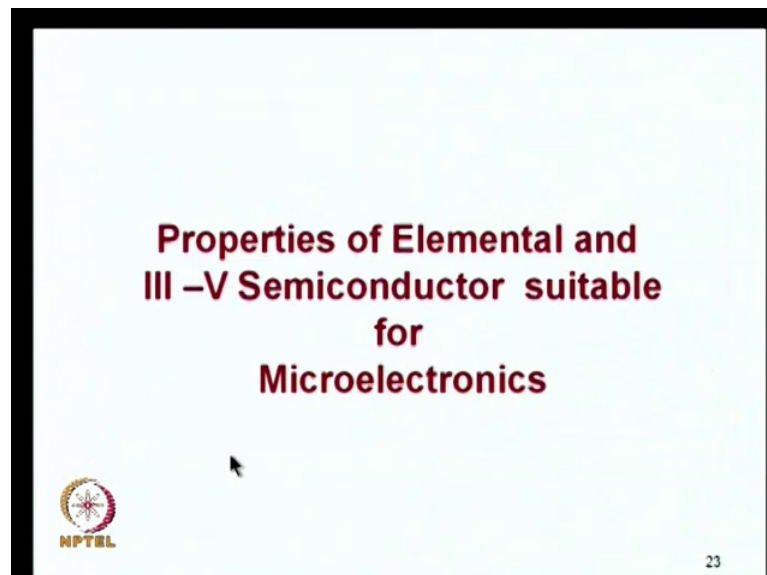
Silicon Carbide :
 $E_g = 3.26\text{eV} > E_g \text{ of Si}$
 $\mu_n = 700 \text{ cm}^2 / \text{VSec} < \mu_n \text{ of Si}$
But High Field Velocity of Electrons is greater in SiC than in Si

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Now silicon carbide 3.26 electron voltage is a band gap higher than that of silicon fine, mobility is very poor even half of that of silicon less than that of electron mobility in silicon. But it will be high field velocity of velocity of electrons will be high at high fields that we will see later.

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**Properties of Elemental and
III -V Semiconductor suitable
for
Microelectronics**

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Properties of elemental and 3-5 semiconductor suitable for microelectronics, so therefore summing up.

(Refer Slide Time: 48:26)

Semiconductor	Si	GaAs	InP	Germanium
Band Gap (eV)	1.1	1.43	1.35	0.66
Electron Mobility at 300K (Cm ² /Vsec)	1500	8500	4500	3900
Hole mobility at 300K (cm ² /VSec)	450	400	150	1900
Saturated Electron Velocity (10 ⁷ cm/sec)	1.0	1.3	1.0	1.0
Critical Breakdown field (MV/cm)	0.3	0.4	0.5	0.1

Some of the properties silicon, gallium arsenide, indium phosphide germanium these are the 3 potential candidates. Band gap I have already mentioned they have better band gap electron mobility best in gallium arsenide and indium phosphide. But germanium is nowhere interfere higher than silicon hole mobility silicon 450, gallium arsenide 400, indium phosphide 150 both are poor no hope for CMOS there. Germanium 1900 efforts are being tried to improve this mobility in germanium.


Saturated electron velocity even we call that as you keep on increase in the electric field and keep on measuring the velocity of carriers it keeps on increasing linearly initially. Then the finally, saturates at particular value of about 10 to the power of 7 centimeter per second that is called saturated electron velocity, that is 1, 1.3 into 10 to the power 7 almost same nothing much to botched off in any case.

Breakdown strength silicon about 0.2 to 0.3 megavolts per centimeter that is 20 volts per micrometer to 30 volts per micro meter depending upon the doping level g-n junctions and gallium arsenide is slightly better 40 volts per micron. Indium phosphide about 0.5 volts micron germanium is poor.

So, if you are taking up 5 voltage device with germanium is not the device. Then you may have to go back to silicon or some of these materials or some combinations. But for nano devices when you talk of low voltage that is not they constrained.

(Refer Slide Time: 50:42)

Semiconductor	Si	GaAs	InP	Germa -nium
Thermal Conductivity (W/cmK)	1.5	0.5	0.7	0.6
Relative Dielectric Constant	11.8	12.8	12.5	16.0



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Semiconductor other property one looks forward to thermal conductivity watts per centimeter degree Kelvin. You can see among all of them silicon has the best thermal conductivity you would be concerned about this when you want back more and more devices. Because the device temperature goes up the chip temperature goes up if the thermal conductivity is high the heat can be taken away by the thermal conduction into the package outside. So, silicon is that way it is better thermal resistance will be smaller like electrical resistance, you can talk of thermal resistance electrical resistance is lower if the electrical conductivity is higher.

Thermal resistance is lower if thermal conductivity is higher so that is best in silicon see other material they all are not as good. Relative dielectric constant not of great importance but almost all of them is there germanium is one having higher.

(Refer Slide Time: 51:56)

**Ternary Compounds
(example)**

$$\text{Al}_x \text{Ga}_{(1-x)} \text{As}$$

Formed by alloying Al, Ga and As
X is the Aluminium mole fraction.

x = 0 gives GaAs
x = 1 gives AlAs

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This just now what I have mentioned ternary compounds, gallium, indium, arsenide you are denoted by this symbol gallium x, indium one minus x, arsenic 1. Usually when you say stoichiometric gallium arsenide there x is equal to 0, x equal I am sorry x equal to 1; x equal to 1 indicates indium is 0 and gallium is 1. So, gallium 1, arsenic 1 that is stoichiometric gallium arsenide in the crystal for each 1 gallium atom there is 1 arsenic atom.

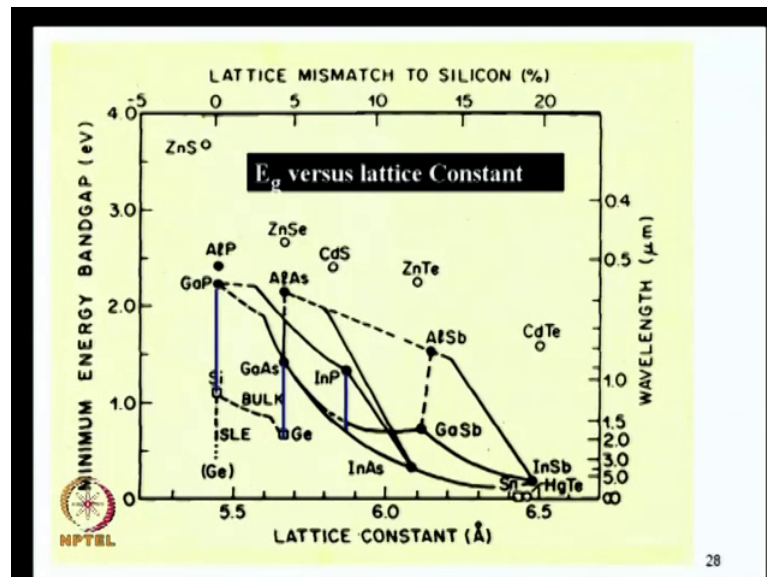
Now, if x is equal to 0.5, gallium is 0.5, indium is 1 minus 0.5, there is 0.5 arsenic is 1; that means, for if there are 10 arsenic atoms there are 5 indium atoms and 5 gallium atoms. If x is equal to 0.3 or 10 arsenic atoms, there are 3 gallium atoms, there are 7 indium atoms a meaning of that that is ternary compound formed by alloying indium gallium and arsenic x is the gallium mole moles fraction I have what I have explained just now x equal to one gives gallium arsenide x equal to 0, gives indium arsenide.

Ternary compound was example is very popular material Al gas. If the gallium arsenide if you do not have time to say gallium arsenide we can say gas, aluminum, gallium, arsenide if you are tired Al gas x equal to 1 gives aluminum arsenide x equal to 0 gives gallium arsenide. So, as x is varied from 0 to 1, you get gallium arsenide to aluminum arsenide you can get this compound ternary compounds.

There are specific reasons for taking look at specifically these 2 ternary compounds. Because after all, if I want to make a hetero structure. What is meaning of hetero

structure? Go different type of materials one over the other make devices you are seeing for a example gallium arsenide on the top of that put another material like aluminum, gallium, arsenide. Indium phosphide on the top of that deposit another material like gallium, indium, arsenide. So these are that is why these are looked into why?

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This graph plot is same as plot right from 1980s people have been flashing this. Let me also flash it to you. When I want to grow or when I want to realize the hetero structure I must be able to grow one material over the other material, if possible without any strain; that means, the next layer that I will deposit on the top must have similar lattice arrangement or similar lattice constant.

So, what this gives is the energy band gap of different material on the y axis and on x axis in the lattice constant. See for example, germanium has got lattice constant of 5.65 angstroms that is 0.565 nanometers. Take a look at gallium arsenide, this is germanium band gap is 0.66 lattice, constant is 5.65, gallium arsenide look at the arrow here 1.43, band gap.

See the lattice constant same as that of germanium like I draw vertical line here 5.65 so that means, one can grow gallium arsenide on germanium without having any lattice dislocations without having any defects introduced we can grow gallium arsenide on germanium. In fact, this had prompted to people to growth thin thin gallium arsenide on germanium to make solar cells ok.

Now, you can see I want to make gallium arsenide and germanium hetero structure I can make I can if I want to make gallium arsenide or if I want to go aluminum arsenide on gallium arsenide I can go because we can see the lattice constant of aluminum arsenide, gallium arsenide, germanium are almost same they are not exactly matching but close. So, aluminum arsenide is a band gap which is more about 2.2 electron volts.

Now if I have in between I mix gallium arsenide and aluminum arsenide I get Al gas. So, I can vary the band gap from 1.43 to 2.2. But (Refer Time: 57:37) remember that aluminum arsenide is a indirect band gap in semiconductor. The dotted lines tell you that they are the indirect band indirect and gallium arsenide is direct. If you go from gallium arsenide to aluminum arsenide what you will get will be direct band gap aluminum gallium arsenide ultimately, it will be indirect band gap.

So, you can grow Al gas on gallium arsenide to realize hetero structure. So, this is shown to possibility of realizing hetero structure devices, Al gas on gas, gallium arsenide on germanium or why did I talk of gallium indium arsenide say this is indium arsenide that is constant is something like 6.1 close to 6.1 and then band gap is very small. I mix gallium arsenide and indium arsenide take about 0.53 of indium I get indium, gallium, arsenide here band gap is something like 0.7 electron volts and lattice constant is matched to that of indium phosphide that is 5.5 6 7 8 above that 5.85 or so you get that. So, you can grow indium, gallium, arsenide and indium phosphide.

So, I just want to point out that, I will come back to this particular slide again. There is there are varieties of possibilities the (Refer Time: 59:07) is limit or choosing the compound material when you use compound semiconductors binary ternary quaternary 4-4 semiconductor everything you can do that.

Thank you very much. We will see in next lecture all these things.