Nanoelectronics: Devices and Materials
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Lecture - 26
Germanium as an alternate to silicon for high performance MOSFETs and the challenges in Germanium Technology

So, we have discussed silicon based FETs or including the metal source drain structures and SOI structures, FinFET and all that. Now, we take a look at non silicon materials like germanium, compound semiconductors. And see how what is the status of that, what were the problems faced by everyone, and how most of it has been sorted out we will see.

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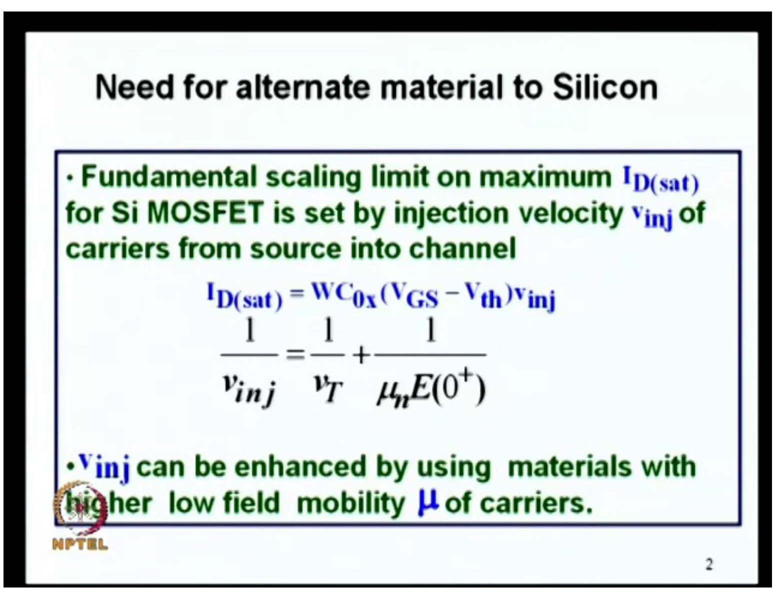

The question immediately comes why do we need to take a look at other materials other than silicon. We have already seen when while discussing the MOSFET that I D sat drain saturation current is channel width, C oxide, per units area V GS minus V threshold into injection velocity when you go to nano scale ultimately. Ultimately the limiting factor is this smaller w then channel length smaller this is a limiting factor.

So, if you want to have higher drain current which is required for driving the capacity loads which are present in integrate circuits you need to have of course, you increase the

C oxide by reducing the thickness of the oxide, but there is a limit to that and you switch out high dielectric door to come that limit.

Now, injection velocity we saw that it depends upon thermal velocity and low field mobility and the electric field at the source end of the junction, trans source end of the channel 0 plus. So, mobility is the one which we keep it as high as possible you will have injection velocity equal to thermal velocity, you can have ballistic transport practically. So, the entire aim is to improve the injection velocity by increasing the mobility.

We have seen how to do that by reducing the doping and by using SOI etcetera. Now if you go over to the material which basically has a higher mobility that is the alternate way. So, that is why one takes a look into other materials.

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Properties of Germanium and comparison with Silicon

Property	Ge	Si	GaAs
Bandgap E_g (eV)	0.66	1.1	1.43
Electron mobility μ_n (cm²/VSec)	3900	1500	8500
	$\mu_n(Ge) >$	$2\mu_n(Si)$	$\approx 6\times\mu_n(Si)$
Hole mobility μ_p (cm²/VSec)	1900	450	400
	$\mu_p(Ge) >$	$4\mu_p(Si)$	$< \mu_p(Si)$
Intrinsic conc. n_i / cm^3	2.5×10^{13}	1.5×10^{10}	6×10^{6}
Melting temp. T_M (°C)	934	1410	1238
	$T_M(Ge) <<$	$T_M(Si)$	

What are the other materials? Silicon all pervasive it is the one which is rolling in the VLSI technology, today because of its availability as you hear often it is a second best available material on the surface of that crust. So, that is available. So, that is cheapest material for suitable, it is very good semiconducting material with band gap 1.1 low intrinsic carrier concentration and melting point is 1400 degree centigrade. So, you can use it for implantation annealing etcetera at temperature like 900 1000 or even 1500 those merits have made people take a look at more and more into silicon, but now on the limit you are hitting towards the limit. Somewhere around 1980s people started looking

at other material like which can give as good performance as 0.1 micron silicon by changing over the material gallium arsenide.

Gallium arsenide can give us good performance as silicon having 1.1 micron, but the gallium arsenide channel length is 0.5 microns or of that order. So, with we do not have to go down in technology they thought we can chose gallium arsenide merit, band gap is higher than that of silicon very good, because of the intrinsic carrier concentration very low. We can go to higher band gap means we can even use it for higher temperatures so; that means, for higher powers, high speed because of the high electron mobility all those things are there everything is meritorious to problems where encountered there, N-channel MOSFET if we want to make fantastic mobility about 6 times that of electron mobility in silicon, but hole mobility even less than that of silicon.

If I want to go c MOS FET gallium arsenide is not the material, the hole mobility is low, but still if we are depending upon N-channel devices like you know hetero junction by power transistors or high electron mobility transistors using electron you can go in for that, people are still looking to that that way. Now, MOSFET with gallium arsenide the lot of efforts depends on gallium arsenide during 1980s even going into 1990s because it does not have an good native oxide, see the best thing that happened to silicon is it band gap is good you can go to 100 125 centigrade it has native oxide thermally oxidize you can excellent oxide which is chemically stable. Means, what is meaning of chemically stable it does not get attacked by most of the chemicals except Hf we can put it in a aqua regia HCL its HNO 3 nothing happens gallium arsenide native oxide is not so stable plus it will have gallium arsenide and arsenic oxide between the tools we can.

It is a compound semiconductor wafer pressure of gallium is different from that of arsenic, arsenic has got high wafer pressure even though melting point is quite good 1 2 3 8 less than silicon, but it is quite good, but if you will go to higher temperatures you lose arsenic because arsenic wafer pressure is high compare to the gallium wafer pressure. So, that was problem in gallium arsenide material itself and oxide arsenic trioxide wafer pressure at 1 atmosphere even at 400 degree centigrade. So, if you lead it 400 degree centigrade you will lose all that arsenic trioxide which is gallium nitride oxide is not a good oxide. So, this was the problem that was faced there.

So, what they are thought was lot of tied out is one thing is in the absence of native oxide you have got surface fascination problems, dangling modes, high interface state density. So, passivation problems were there we come back to this later. So, fascination problem is one thing dielectric what will use dielectric deposited dielectrics high k dielectrics you use. So, now, you can see that high k dielectric technology and passivation etcetera was going with gallium arsenide, simultaneously the silicon people came back thinking if I cannot go to thin oxide like 1 nanometer or below why not I go to high k dielectric see after all the capacitance per unit area epsilon oxide divide by t oxide. Now, I am able not able to reduce the t oxide to increase the capacitance, but I can increase the epsilon oxide by using high k that was idea.

So, it is sort of borrow from here with people who are struggling with gallium arsenide silicon technology people had because they have invested so much money on that they can come back with idea that is go to high k dielectric now. So, lot of effort has gone in gallium arsenide work at least hemt, hebt etcetera happened MOSFET not much success, because not because of MOSFET because c MOS cannot be done, c MOS integrate ic cannot have in the case of gallium arsenide. Now, at this stage the mobility electron mobility is higher here hole mobility is low, at this point thought came back to the original material on which the transistor was invented germanium 1947 in the transistor invented by Shockley Bardeen and Brattain that was germanium and effort was towards making MOSFET with germanium.

But while doing that effort on MOSFET fabrication on germanium accidentally they landed up in bipolar transistor, I will not go into history of that, but that is the history. So, be the original devices were all be bipolar b j t if we are germanium 1950s 1960s if you look at the industries all the germanium transistor b j ts were there MOSFET was not there really. Only when the MOSFET came up with silicon germanium also thrown away because it does not have native oxide, you may ask does it not have native oxide yes germanium dioxide is there, but germanium dioxide is very unstable it can even get washed away with water, chemically unstable heat it to about 500 600 centigrade, you lose germanium oxide it, it convert it to germanium GO2 become GO all that we will see and lot of defects you defects states create in the interface as well as in the oxide so native oxide out of question. Now, borrow from silicon, silicon also you are not using

native oxide you are using the depositor oxide why not use depositor oxide with germanium.

So, here again you have the similar problem that we had with gallium arsenide surface preparation, surface state to be satisfied surface passivation and also deposited dielectrics, what dielectric we will use? What technique we will use for preparation? Those were the things that where that, are to be dealt dealt with germanium. Now, let us take it look at the germanium by itself band gap is low, bad news that are one of the reason why germanium got to back chart so 0.66 electron volts that limits its temperature of operation to high temperatures.

So, if we are not worried about that you may still use that, but if we can increase the band gap by somehow by germanium by quantization you overcome that problem. In fact, band gap can be increased if use very very thin layers of material energy band gap can increase. So, that can be go up, now other problem 1 think thinks of is melting point 934, if you reduce all your processing temperature to 500, 600 degree centigrade you do not have to worry about that ok.

In a ray germanium has tremendous advantages to use metals semiconductor, metal gate MOSFET when you use metal gate you are not doing that n plus poly doping etcetera in high temperature process is not there metal gate can be done at low temperature. Source drain you can use as metal semiconductor metal source drain contact Scotty. But again you have to look into the problems are which are there or creating the ohmic lower barrier height contacts, p-channel MOSFET with germanium.

Therefore, is not an issue because platinum silicide makes very low barrier with germanium to p-channel can be made. And we also seen if you do passivation with sulfur we can reduce barrier height for electrons also. So, both N-channel p-channel can be done with germanium what about mobility, 3900 centimeters square per volt seconds electrons almost 3 times that of silicon may not be as good as gallium arsenide.

But it is not a compound semiconductor, it is elemental semiconductor you have to deal with only 1 element in gallium arsenide you have deal with both gallium and arsenide. So, that way electron mobility is quite good look at the whole mobility 450 silicon 400 gallium arsenide for whole mobility, centimeter square per volt seconds thousand and almost 4 times that of silicon. So, that is the cleaving this what attract germanium that is

what germanium has come back in this millennium, it has come back, because of its high mobility and ability to make ohmic contacts or their low barrier height contacts to the channel, ability to deposit high k dielectrics ability to passivate provolone those are the things key issued to be seen. So, intrinsic carrier concentration is high, you can see that if you make a junction junctions will have leakage unless you are able to increase the band gap.

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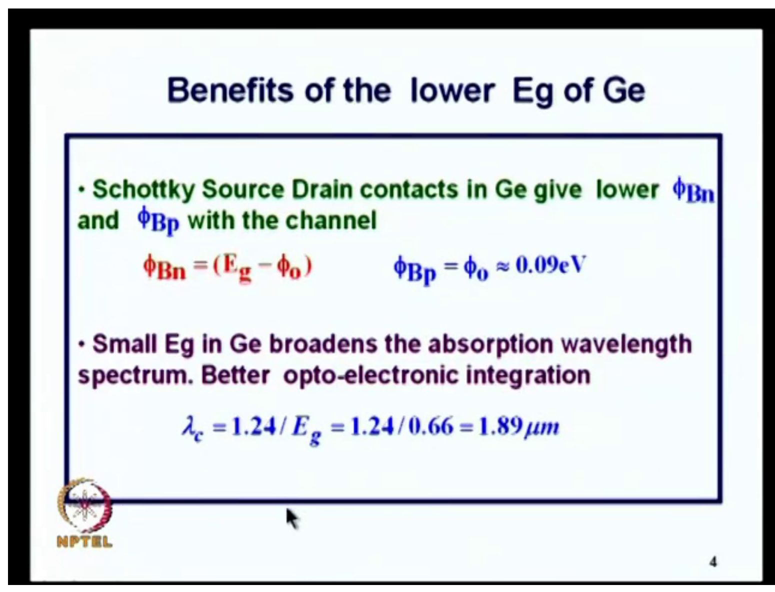

Now, once we have low band gap like 0.66 electron volts they cut off wave length for optics optical absorption is 1.89 microns 1.24 divide this is h nu energies h into nu and nu is velocity by lambda. So, absolute all that you get cut off wave length that is if the wave length is shorter than that energy is greater than 0.66 electron volts. So, if wave length is length less than 1.89 micron micrometer all will be absorbed. Today if you look at the inserted detectors they are all germanium because you can see very long wave lengths can be absorbed by that germanium detectors are used because of that silicon cut off wavelength will be 1.24 by 1.1 it is about 1.1 electron volt micrometer. So, beyond 1.1 micrometer it, it would not absorb ok.

Gallium arsenide cut off wavelength is 1.24 by 0.8 0.1 0.43 that is about 0.8 micrometer, so no not suitable for those wavelengths. So, optical we can have optical devices if you want to have along with the germanium, germanium is very good, because it broadens

absorption wavelength of the spectrum better for opto electronic for opto electronic integration this looking at plus side of germanium.

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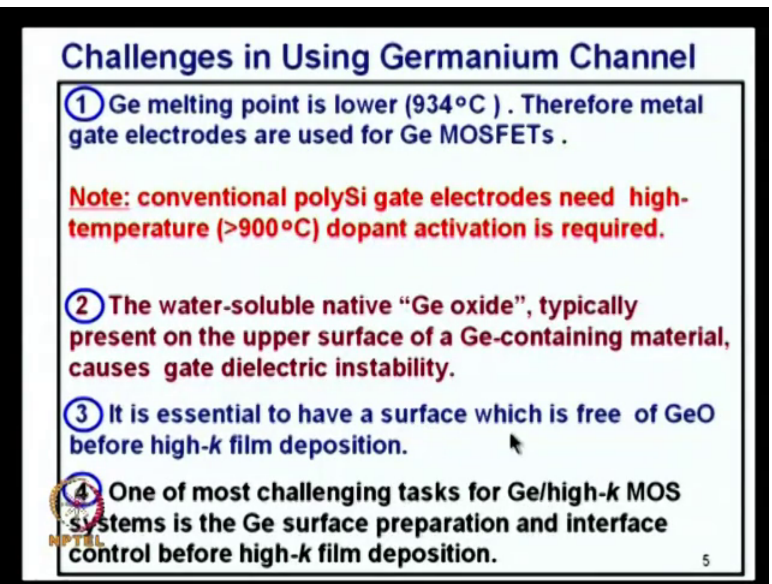

Challenges germanium melting point lower than lower 934 degree centigrade therefore, metal gate electrons are used for germanium MOSFET that is not an issue, conventional poly gate electrons need high temperature and dopant activation. We do not need to do that for a germanium which are using metal gate problem water soluble germanium of oxide typically present in upper surface of germanium containing material causes gate elect gate dielectric instability, chemically not stable.

So, any chemical was will you do it goes off, it is essential to have a surface which is free from germanium oxide because that creates lot of defects (Refer Time: 15:59) germanium oxide that is unstable. So, it is covert it to germanium oxide by reaction with germanium. So, you will have germanium oxide there. So, it is it is quite remove that always that is a problem one that look into you can use high k dielectric no doubt ,there is no native oxide that is there is no native oxide go to high k dielectric, but surface preparation. Most challenging thing is germanium surface preparation and interface control same as what we had with gallium arsenide, same as what we have with silicon high k dielectric, but there at least we can say I can go very very thin layer of native oxide I can satisfy that and then I put the high k dielectric in silicon.

You cannot do that in germanium and gallium arsenide.

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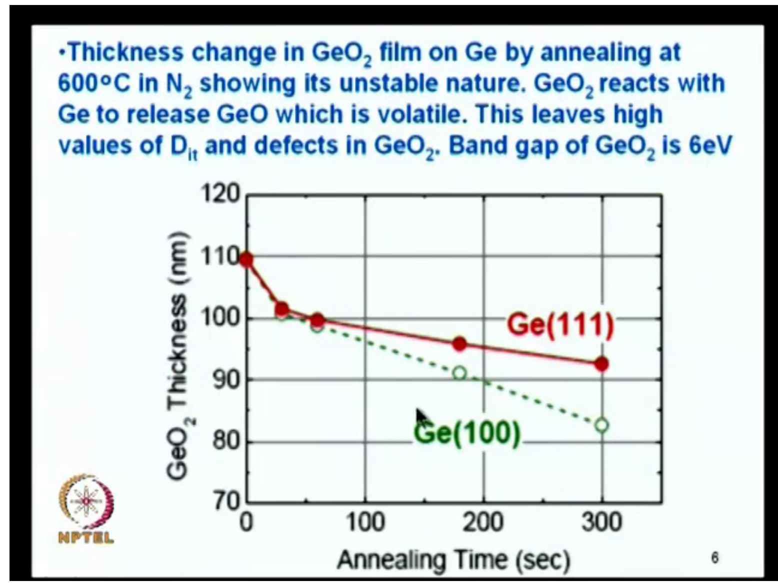

These just to show this one of those wafer oldest wafer which I saw thickness if I have germanium dioxide deposited on that by sputtering technique and if I anneal it at 600 centigrade in nitrogen forget about solubility not water if you need the thickness comes down. Germanium dioxide reacts with germanium to release germanium oxide. So, the germanium oxide is volatile, it comes through a germanium dioxide.

So, you see that the thickness of this germanium dioxide keeps on reducing indicating that it has got converted with germanium oxide which has been lost and when that happens the presence of germanium dioxide and very highly defective germanium dioxide present there presence of along with presence of germanium oxide gives rise to very high values of interface state density.

So, what people have concluded is no good to have germanium dioxide, remove that completely exactly same condition was arrived at in gallium arsenide, no good to have native oxide remove that native oxide completely before you do any chemical treatment so that is the problem of the interface.

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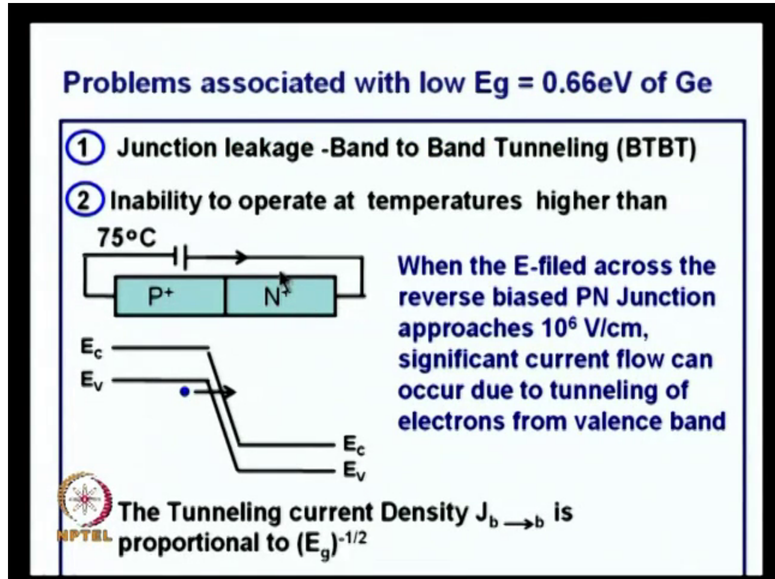

Now, leakage if the band gap is low if you make a channel make a MOSFET with silicon you saw when we make a you dope the channel heavily, for a thing do not you will not going for a SOI etcetera you make that heavy doped channel so; that means, the drains is n plus channel is also heavily doped. So, the energy band diagram between the channel region and the drain region will be like this, this is the P-type region plus here minus here energy band diagram bends here. Look at this diagram you may say I have got 0.66 electron volts of the energy band gap, but when it bends, it bends parallely the gap between the conduction band and balance band if you go vertically is 0.66.

But since its barrier width is very small if you go from here to here that width is very small. So, you may have vertical band gap 0.66 electron volts, but horizontally that thickness is very small. So, it the distance between the violence band and the conduction band here will be very small, there are enough states available in the conduction band of n type material there are enough electrons available in valence band they can tunnel through that. So, when you apply reverse bias of the order of about 10 to power 6 volt per centimeter which very easily can reach in the drain voltage of couple of volts when the doping levels are that high you will have tunneling here. So, from that point of view silicon do not have that much if problem because band width gap is wider. So, this gap between these 2 is not as slow as in silicon.

So, inability to operate at temperature higher is one problem higher than 75 degree centigrade because band gap is low junction leakage band to band tunneling, BTBT you will hear the jargon use BTBT problem that is band to band tunneling problem for valance band conduction band tunneling problem. So, that is there. So, that is present here all these lead to high j band to band is which is proportional to there is a formula for this it is inversely proportional to Eg square root, less the band gap more will be the current less the band gap that gap is reduced this is what is one of the problem that is encountered then.

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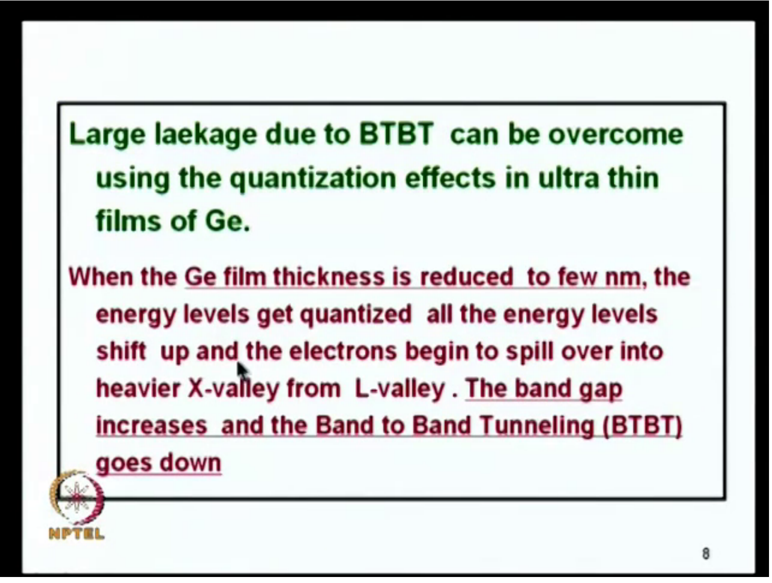

Large leakage current due to band BTBT can overcome the can be overcome by the quantization effect ultra thin films of use that is a solution.

So, the band gap increases and the band to band tunneling BT, BTBT goes down this general physics we know that if you reduce the thickness there will be transfer of carriers from one valley to other valley and the band gap becomes higher. So, you would not be having that problem instead of 0.66 if it goes even to 0.7 you have overcome the problem because root of Eg.

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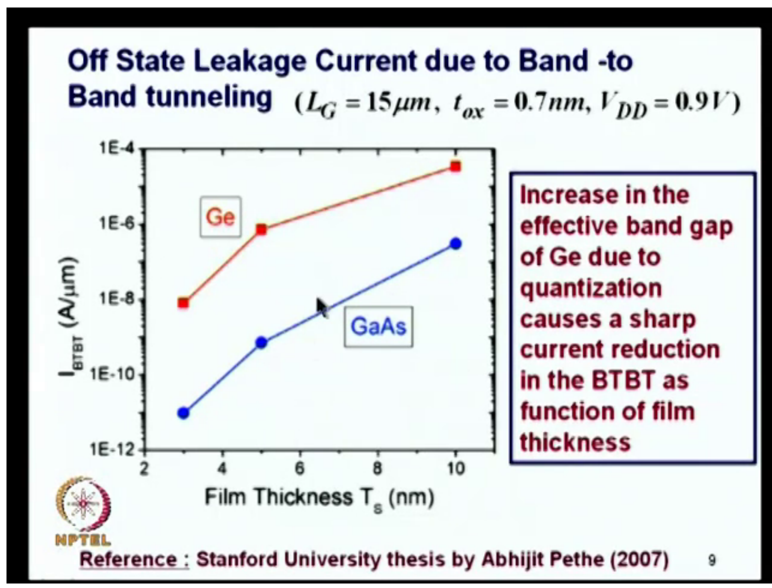

So, this is one if the result which was reported in the Stanford university thesis way back in 2007 this we got through a professors who had come over here who give a talk he was this is his slide. So, it is say where if you make gallium arsenide thickness is very very thin you have the band gap we have the I t BTBT current gets reduced drastically same with germanium.

If you make thinner and thinner from 10 nanometer to about 2 nanometer 3 nanometer if you go down whatever current which was about 10 to power minus 4 amperes per micrometer width of the channel goes down to 10 to power minus 6 several orders of magnitude you can reduce because band gap is Eg is reduced. So, this is what makes it, this is a favorable condition for germanium; that means, if you have to if you want use germanium better you sit in very thin films. So, it is better suited for thin devices like SOI, but you cannot call it as SOI it is no longer silicon on insulator, what is it then? GO I germanium on insulator it may not be oxide it is an insulator. So, people talk of GOI there. So, such devices are the 1 which are you have get a pointer to do a in this application of germanium. So, with all that positive attitude one has move forward.

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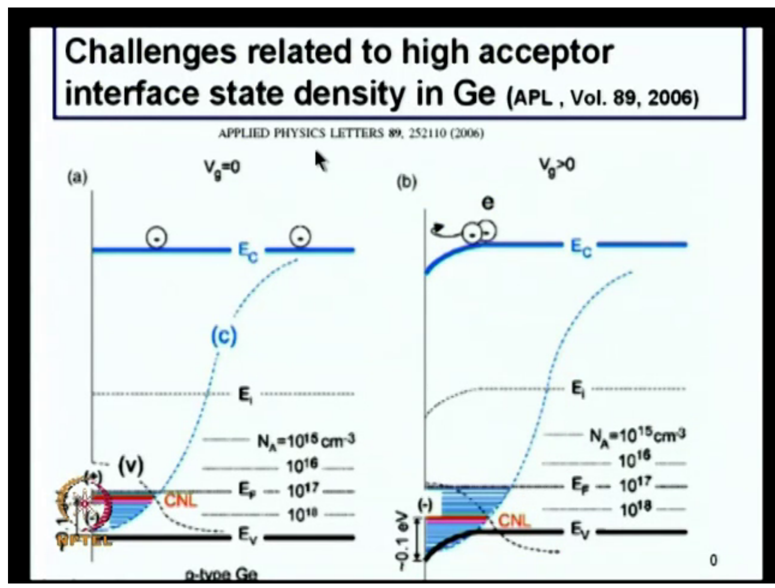

Take a look at what happens now.

So, positive things are all there if you suitable we handle to take care of interface state density and also take care of improve in the band gap, challenges related to the surface state density. If you take the free surface of gallium arsenide this is the conduction band and this is the valance band E V and E C gap is 0.66 electron volts and the neutral level is somewhere here I given as 0.09 or so. Just some places they were round of saying 0.1 0.1 electron volts is neutral level suppose the doping in the. If it P-type material and if the doping is adjusted such that Fermi level is coinciding with this level actually 1 can calculate and show that if the doping is 10 to the power of 17 acceptors in germanium a Fermi level will coincide with the neutral level.

This is a neutral level charge neutral level CNL is charge neutrality level say they use to call it as neutral level earlier have been using that terminology. Now, people call is CNL do not have time to say neutral level CNL charge neutrality level. So, if it matches with that you know that this charge a Fermi level coincide with that net charge is 0 all the acceptors are not occupied, charge is 0 all the donors and surface are occupied charge is 0. Now, what is plotted here ce is the acceptor densities that is starting from conduction band edge that is the way the density of states is DIT high near the conduction band lower lower somewhere it is lower and it is becoming practically 0, because it is compensated by this dotted lines here they are a donors. Say normally we assume in that

analysis DIT is same all through the magnitude is same 10 to power 12, 10 to power 12, 10 to power 12.

This may be 10 to power of 14, 10 to power of 13, 10 to power of 5 time 10 to power 12, 10 to power 12, 5 times 10 to power 12 that is small. Same way donors 10 to power of 13, 12, 11 like that. So, it is varying across the band gap, in silicon also it is like that you usually plot a some u shaped density of distribution it is not really used in some arbitrary shaped like this minimum barrier, but it is true that at the neutral level both of them cancel each other at 0, they match above that acceptors. So, this is a situation I will go back to this.

Afterward, this is if you have will see this later on this is actually one of those wafer which very famous wafer for germanium be also gave the schottky barrier height in that in the previous when we discus schottky barrier and showed that neutral level is somewhere there, 2007-6, because once germanium become popular people start to look into that ok.

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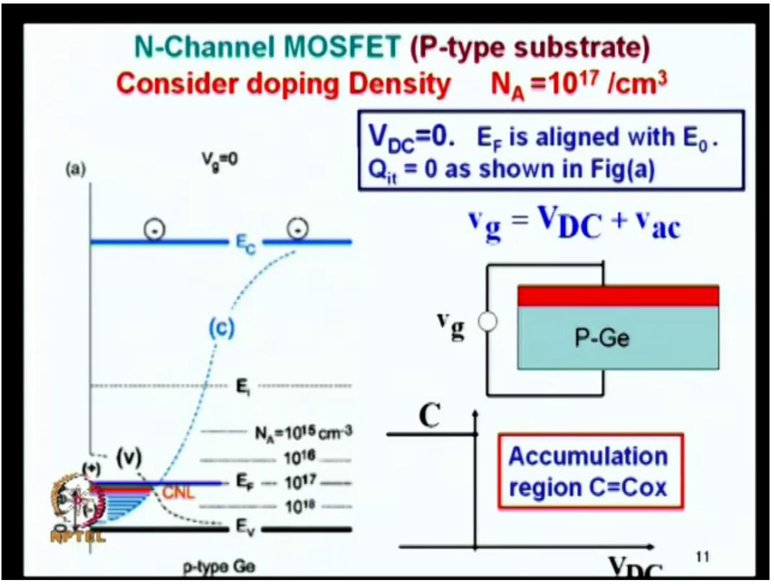

So, we have seen that if the doping level is 10 to power of 17 pair density is 0. So, if I take a P-type semiconductor and do not apply any voltage to the gate Fermi level is there if I apply plus plus voltage to minus voltage to the gate accumulation that is almost there itself. So, capacitance in the accumulation region will not be effected by the interface state, then there is no interface states they are all neutral because Fermi level is coincide

if it is doping is 10 to power 17, but if the doping is other than that suppose if the doping is higher than you will have some acceptors coming into picture here and if you doping is lower you will have the other effects we will just take this that is why we have a material like that you have no problem accumulation.

But what happens see I just put V DC plus V ac where the way you measure the capacitance is bias it with a particular DC super impose ac you measure the current actually the ac current. That is how you measure the capacitance, at a given bias how much is the ac current that is flowing through the thing that is the idea. So, you sweep the DC and measure that is easy current flowing through that as sweep it very slowly that the semiconductor has enough time to come into equilibrium with the voltage applied voltage. So, you sweep it very slowly, if you sweep very fast you will see the results will be different. So, this is a accumulation. Now if I apply a plus voltage to that ideally what will what you if the interface state density was 0.

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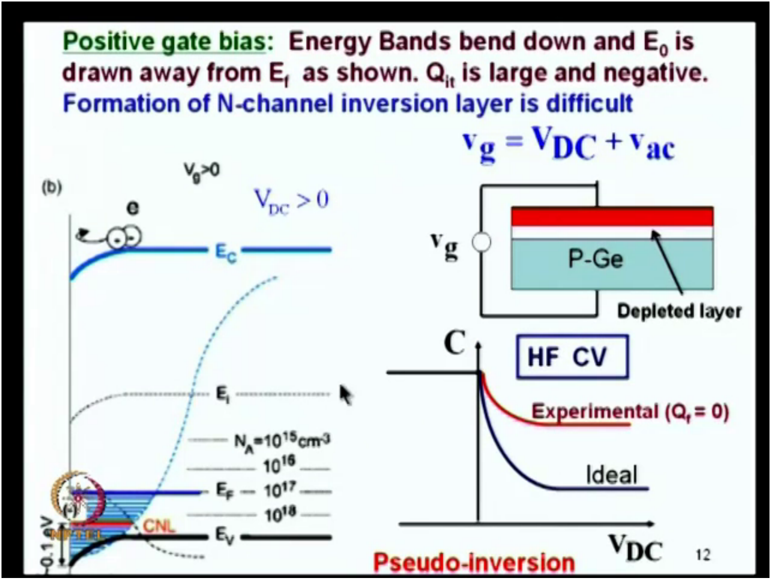

You would have got it like that, capacitance it will deplete it will invert and you have got this high frequency capacity like that, but the moment you apply plus voltage go from 0 to plus voltage V g is V DC plus V ac you see is for measurement what happens to that plus begin to deplete. The mobility depletes you can see in the bulk Fermi level is still align with neutral level it is distance between the Fermi level and the valance band the energy distance is same the neutral region, but in the surface it has got depleted Fermi

level is slat if it has depleted it has become less P-type. That means, the energy distance between the Fermi level and the valance band has increased. So, energy band has bend down here, now the neutralized level is described with respect to the valence band edge. So, on the here it is the bulk, but on the surface the neutral level is appoint 1 electrons above the valence band.

So, all the donor levels are occupied there is no problem, but because the Fermi level is above the neutral level here now being the surface all these levels are exposed, that is these acceptor levels are below the Fermi levels; that means, as the energy band diagram bends keeps on bending when you increase the plus voltage more and more acceptors get you know they are below the valance band more and more electrons occupying this acceptor level. So, all the levels here will be occupied by electrons, and they are taken from the either from the depletion layer partly from the plus voltage that we apply, combined effect is the plus voltage that you have applied to the gate has got 2 types of the negative chargers, one coming from depletion layer other one coming from the interface state.

So, if the interface states where not there for a given voltage that is why I am here for a given voltage the depletion layer width would have been let us say w naught and you would have got particular capacitance. Now, for the same gate voltage because the band bending takes place not only the negative charges are supplied from the depletion layer native charges are from supplied from the interface state also. So, the depletion layer width they let us say there are 100 electrons are required in the absence of interface state density all the 100 comes from depletion layer when the interface state density is there that is a half of it comes from interface half of its from depletion layer. That means, same 100 electrons are supplied by the combined effect of interface state and the depletion layer.

So, less depletion layer width, lesser depletion layer width is sufficient because part of the charge come from the interface state; that means capacitance will be higher. So, for the same voltage plus 100 charges are at the gate I am just giving an example, 50 from interface 50 from depletion layer. So, depletion layer width usually you require 100 all the 100 will come from depletion layer, now depletion layer is required supply only half of it.

So, depletion layer width will be half of that, if the depletion layer width is half of that capacitance will be higher. So, the capacitance does not go down all the way down you will not have inversion, but you will have flat region here you will not have inversion if the interface state density are able to response to high frequencies usually those interface state densities may not respond to that low frequency, but they respond to high frequencies.

So, what happens now is whatever capacitance is there after that depletion layer width widens sufficient amount of charge comes from the interface state density because that is high. So, almost everything the there is no more widening of depletion layer width. So, the capacitance will be C oxide in 0 it is depletion layer width which was which has occurred at this point it is not inverted at for inverting the voltage drop must be equal to 2 phi f it is not 2 phi f there is no inversion layer. But it looks to you when you measure it at high frequency it looks to you that capacitance has flattened. And if you take the C oxide by c inversion you can get the depletion layer width from there you will see that the depletion layer width is much smaller than the corresponding to 2 phi f. So, one of the indications of high interface state density is this thing. Now if you keep changing the frequency you will have the freq frequency dependence or the capacitance are will come into the picture ok.

So, this is called pseudo inversion that is pseudo inversion it looks as if there is inverted because it is saturating, but there is no inversion. So, will make a MOSFET with that what will happen? Nothing no current all that when we change the gate voltage the fellow which responds is that interface state channel there is no charge. So, MOSFET will not work these exactly the similar thing that Shockley's etcetera observed when that try to make MOSFET on germanium by depositing oxide they did not deposit oxide. They put a mica sheet on germanium they did not have time to or patience to see how to go about let us put a tale tick on the top of that, put a metal, apply voltage see whether the capacitance changes nothing, put a contact on source and drain no current that is time at which they came up with the theory of interface states.

Bardeen who are the group member came up with the theory for which he got the Nobel prize along with Bardeen Brattain Bardeen of course, got another Nobel prize later on in 1964 ITC wafer conductor high temperature wafer conductor. He was one of those person who are got two Nobel prizes right. So, this is a problem. So, you are unless you

are remove the interface state densities you have no chance with N-channel MOSFET, let us see whether you have a chance for p-channel MOSFET, because we are looking for p-channel devices, because we have got very low barrier height there.

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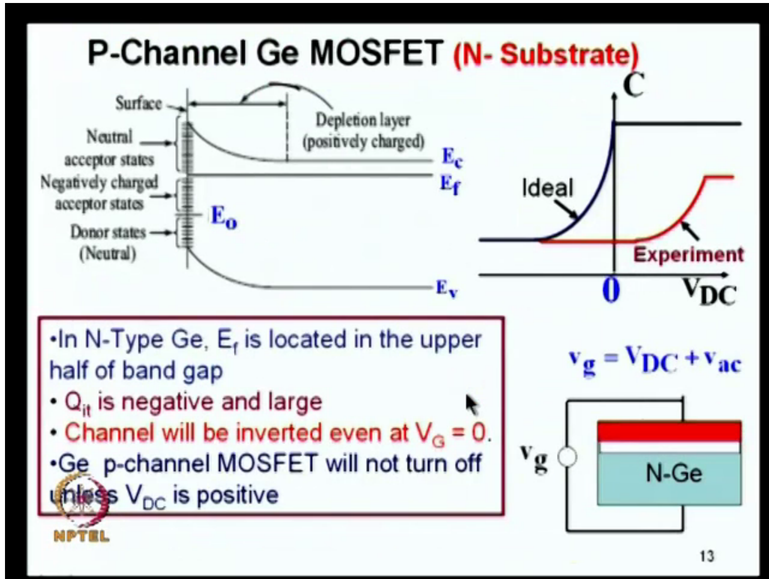

Take n type semiconductor if it is troubling a p-channel it will be N-channel in troubling in p-channel also, p-channel MOSFET substrate will be n type what will happen look at that here Fermi level is much above that.

So, this is the neutral level 0.1 electron volt above the valance band I have shown this magnified these are all the acceptors. So, all these are acceptors above the neutral level which are below the Fermi level are occupied by electrons; that means, if it is n type let us take this free surface no metal there, they are taken away from this semiconductor donors. So, there is a depletion layer.

Now the interface state density can be. So, high 10 to the power 13 of that order then what will happen band bending will be. So, much that it will be inverted already. So, even before put in the metal it is inverted you go put some high k dielectric are there nothing happens, interface states are there put a metal on the thing it is inverted even at 0 valance it is inverted. So, ideally you would get this characteristic for p MOS plus voltage accumulation negative voltage depletion and inversion.

So, even without applying you will have because of that depletion too much of depletion it will be inverted people have observed this thing. So, if I have to come out a depletion and go to accumulation what will we have to do, apply large plus voltage all those minus charges which are there will be can be taken by applying plus voltage. So, that charges or this depletion layer comes out of depletion layer. So, plus apply you will have the, you know now what happens free surface plus charges that a electrons comes from here.

Now, you divert that electric entire field length from this direction to that direction see electrons have got donated here leaving behind plus charges electric field plus minus in that direction, I put an oxide and I apply a plus charge there plus voltages to the gate plus minus come here. So, these donors which are donated to electrons they have to donate it comes plus charge come from that gate.

So, depletion it comes out of depletion you can there is a chance for you to go to accumulation, still you may not get actual accumulation that will again give you pseudo accumulation that is you will not be able to come out completely thorough the depletion layer. These are like in fact, those worked on gallium arsenide had seen exactly similar effects are assign you seen in germanium n type germanium E f f is located are upper half of the band gap q I t is negative and large channel will be inverted even at V g equal to 0 germanium free channel MOSFET will not turn off unless V DC may positive, even there the capacitance is lower indicates what it is not true accumulation.

There is still some depletion layer see when you apply a plus voltage to a gate what happens here is it is able to bring it out of inversion, but it is not still able to bring it in to accumulation. So, you there will be oxide in series if the depletion layer. So, you will have that capacitance there lower than that of you have turned out a device all right, but you do not get the oxide capacitance this again will be frequency dependent.

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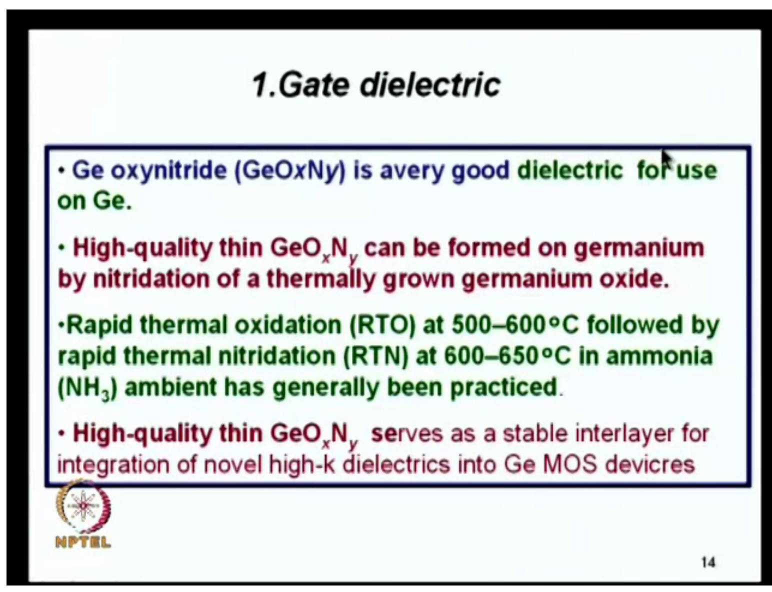

Now, let us take a look at what are the things that you can do, people have liked games, enjoyed making various types of things first thing is a what guide gate dielectric will use not g, not ge o. So, they thought let us see I will just go through quickly what people have tried because that is intersecting.

In fact, when you go through that sometimes you also see there is something available for you to think as I thought because when you want to do some research that is why I am going through that germanium oxynitride, they found that that is good dielectric. High quality germanium oxynitride can be formed on germanium by nitridation of thermally grown germanium oxide grow germanium oxide how do nitridation do, what do you do is rapid thermal oxidation oxidize germanium do not allow that to evaporate, do not allow that react with germanium 500 600 degree centigrade in few seconds, rapid thermal processing oxidation followed by that rapid thermal nitridation for you must have a system.

Where you have oxygen and ammonia pass ammonia through that 600 650 degree centigrade you have got gallium oxide then gallium oxynitride OxNy that is quite stable, high quality thin gallium arsenide serves as stable inter layer over integration of novel high k dielectrics you can do that put high k dielectrics there, that is what was the thought.

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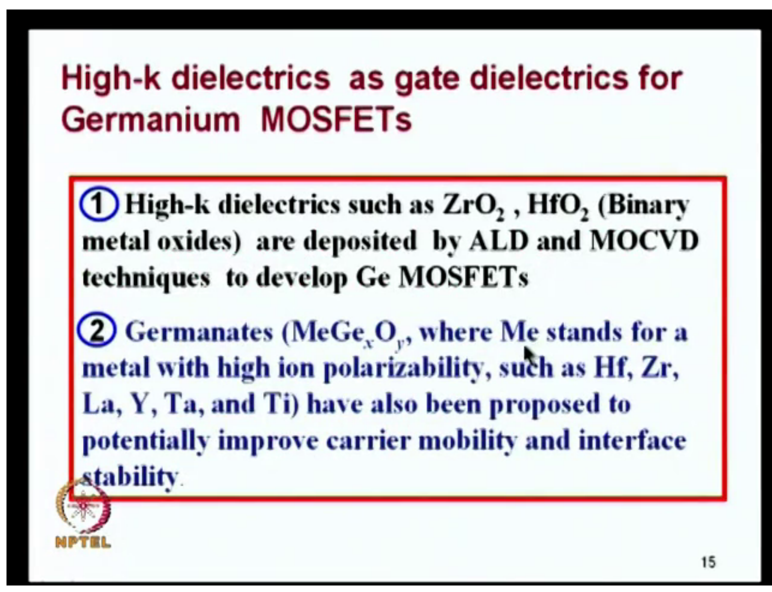

So, what is high dielectric that came is. So, you not only not want have that interface is gallium oxynitride follow it up the high k dielectric, same thing that use for silicon hafnium oxide or any other oxide, lanthanum, yttrium all those things, but hafnium oxide zirconium oxide. They are the once people have being using mostly you will see that for high k dielectric use for germanium is also hafnium oxide one thing people have bought their hands on by the silicon high k dielectric they can do that ok.

So, let us see how things have happened with the ammonium with gallium oxynitride and high dielectric.

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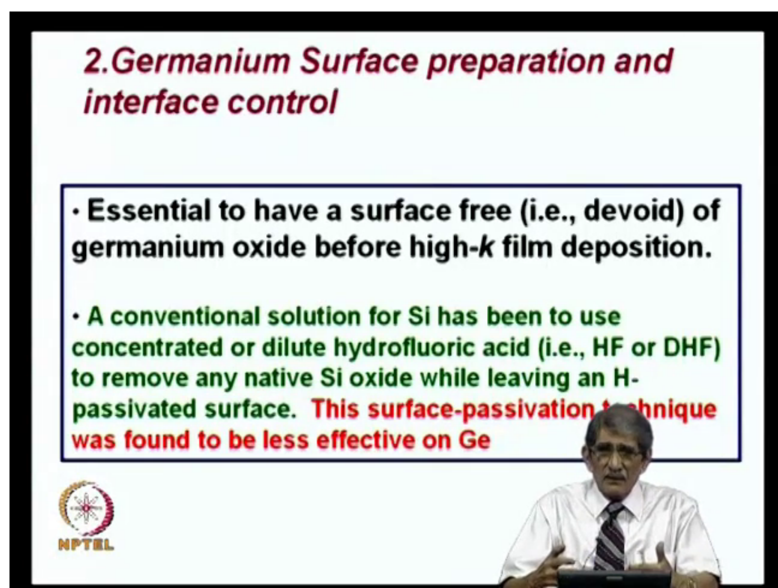

But there is one more thing that people want to think of let us say without that can you do without that germanium oxynitire can you do a surface preparation and put hafnium oxide, there are two interfere one is interface passivation other one is high k dielectric. How do you use germanium oxynitride then high k dielectric or give some preparation that is essential to have surface free of all the germanium oxide before you put a higher dielectric, conventional solution is Hf that is not good enough in germanium we can see that.

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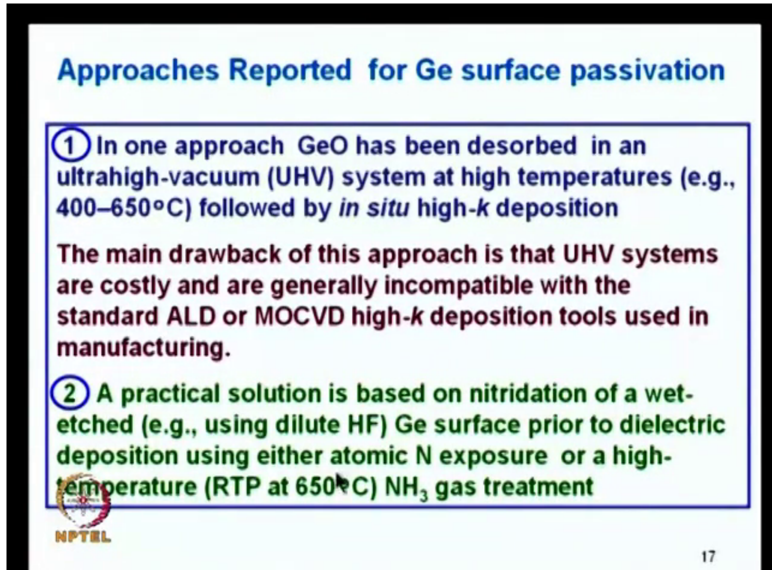

What they have done is in one of the approaches germanium oxide has been desorbed see what do you want is do not want germanium oxide germ GeO 2.

So, what they did was this is will tell you how much work has gone into this in this past 10 years or 10 to 12 years, have the germanium native oxide is present put it in a high vacuum heat it, remove it and then deposit high k dielectric. That is one approach to some degree of success with atomic layer deposition they deposited at the high k dielectric like hafnium oxide did not get much success, but partly I think and also it did not accept, because of the cause involved in all these things people were looking alternatives, did not really catch up with people. Practical solution is based on nitridation wet etching you do, do nitridation with ammonia then deposit high k dielectric that is what I mentioned earlier RTP.

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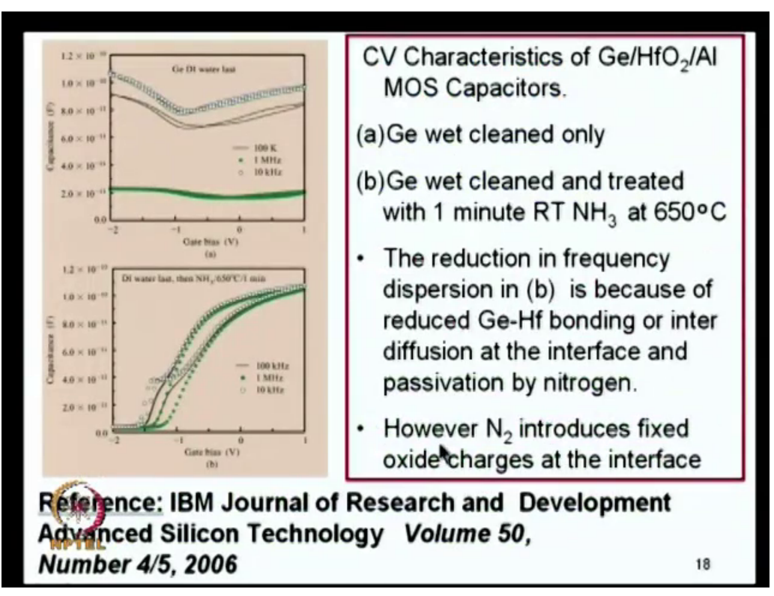

So, now let us see how it is.

So, this are the result you can see how horrible CV gap CV is almost flat CV characteristics of germanium hafnium oxide aluminum one case germanium cleaned only with Hf, just clean with Hf other approach would be of course, float in the high vacuum we remove all the oxide etcetera, remove the oxide deposit hafnium oxide apply whatever technique atomic layer deposition and then put aluminum, CV is flat; that means, there is no it is a still problematic. Other approach was germanium wet means Hf treatment, wet treatment cleaned treated with 1 minute with ammonia. So, 1 is only give

wet treatment then hafnium oxide did not butch, other approach is Hf dip remove the oxide because we do not want the oxide.

Then RTP rapid thermal processing at 650 degree centigrade with ammonia that whatever little oxide is there it gives germanium oxynitride then put the high deposit hafnium oxide, that give some CV that is increase cv. That means, what we are telling is you have germanium oxynitride by RTP then deposit hafnium oxide, you get some at least response to the d c, I am sure that people had overjoyed by seeing this, but there is lot of its still did not give the expected values of CV telling that still there are some problem, issues in this they dint make MOSFET on this only CV you will see most of things are on CV, but MOSFET have been made now, ok.

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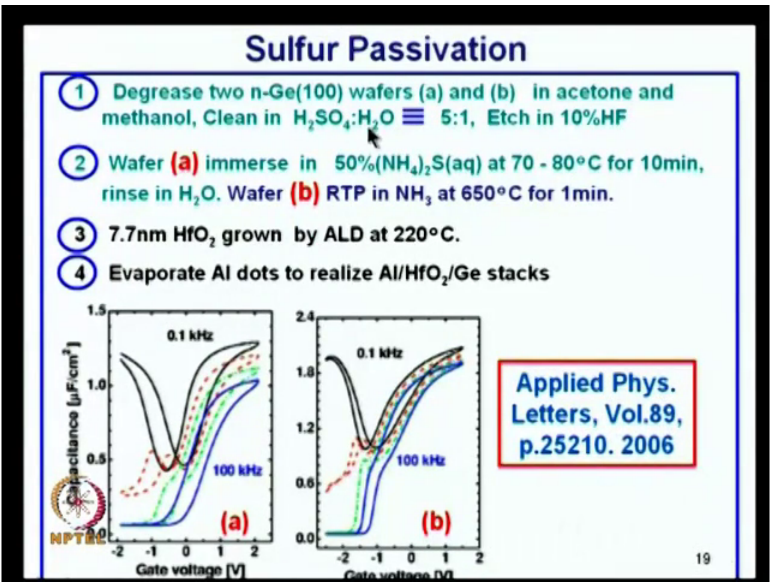

Then what next sulfur, people came up with sulfur passivation. So, here what is done is again you have to compare the surface degrees all that I if I p a and all those things done 2 approaches, 1 approach a and b clean in. So, first you clean with sulfuric acid h 2 O.

And then Hf it that is suppose to give clean surface like what do you do in silicon, but sulfuric acid it will remove some surface also and then whatever little oxide is there hopefully it has gone in h f, they did not do that oxide nitridation with 1 approach approach a after this wafer cleaning they immerse it in 50 percent dominion sulphide, 70 to 80 degree centigrade that is sulfur passivation which I discussed in the last

presentation, sulfur passivation sulfur attaches on to germanium it passivates through gangling modes it at least shifts the neutral region. So, it is passavant suppose to be.

So, you do that in another approach take that the RTP approach. So, we are comparing now one is that nitridation with ammonia other 1 is with sulfur with chemical treatment, sulfur treatment that is very simple to that chemical treatment sulfur treatment put the more deposition hafnium oxide see always high k they have chosen hafnium oxide. So, they got the CV with hysteresis and everything, but you got the this high frequency and low frequency low frequency also was hysteresis is there telling that there are still some interface states series are there they estimated the interface state density one with sulfur, other one is ammonia.

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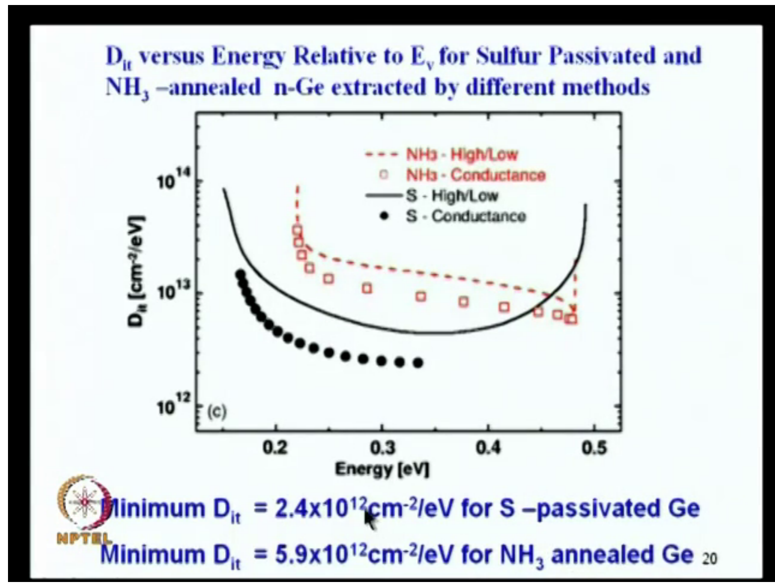

They found sulfur was better there are different methods used one is conductance method other one is high frequency low frequency method.

This sulfur passivated gave about 2.4 into 10 to power 12 centimeter square per electron volt that is the minimum that they got whereas, ammonia treated nitro hydrate 1 gave slightly higher, telling both of them are good or both of them are bad not good enough. Now, came the interesting results at this point all this were only the CV and this was in 2006 again that is the time people were doing the chemical things.

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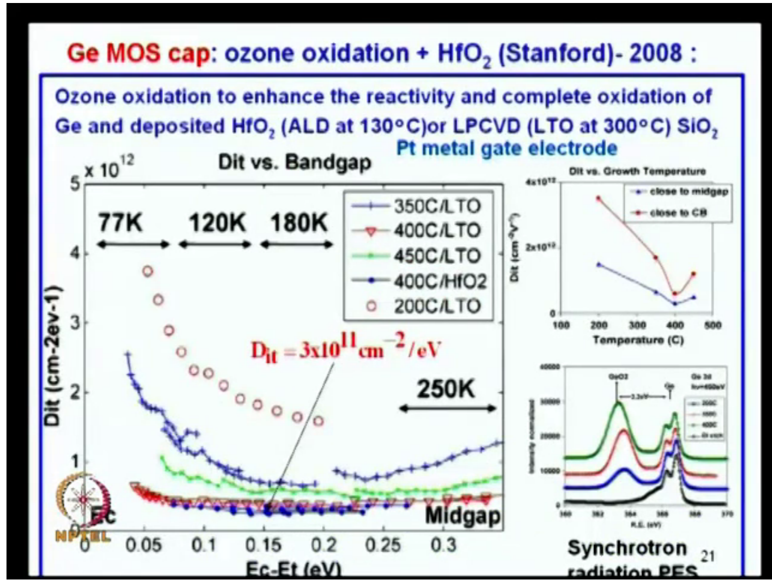

Then came in 2008 we are coming closer, 2008 Stanford university (Refer Time: 49:19) through they publish a paper, excellent interface state density down to down to about 10 to power of 11 something like that.

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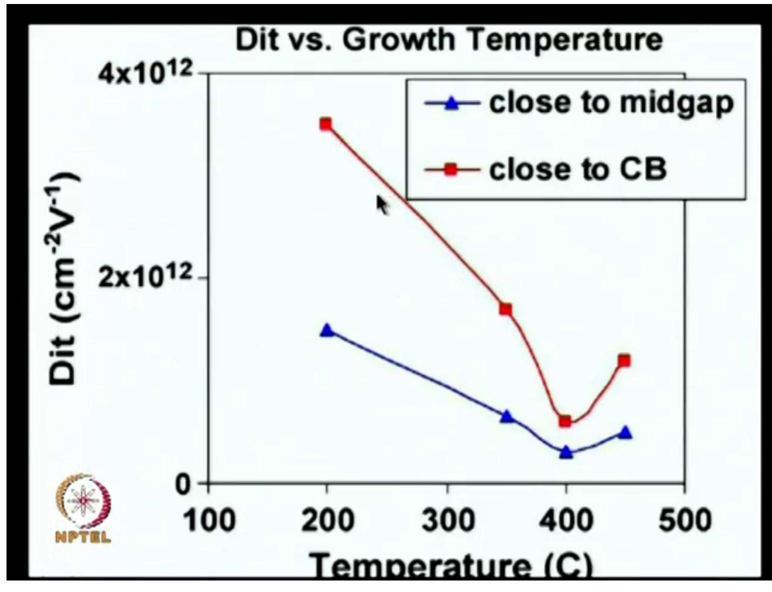

I have noted somewhere DIT 10 to the power 3 10 to the power of 11 ok.

What they did was this is very interesting see what you have to worry is the native oxide walks upon people were worrying, but the what they have shown is native oxide by itself plus GO2 is do not allow the GO2 to react with germanium, to release germanium oxide.

If GO GO2 and GO the non stuck schematic GO is dangerous, that gives rise to state interface state density that gives rise to defects in the GO2. So, prevent heating it to high temperature. And when you do that oxidation on germanium you have to go to higher temperatures RTP you do still you have go into higher temperatures, there will be some incomplete oxidation. So, what they did this is the very novel idea ozone o 3, o 2 is oxygen ozone was o 3 at there is available, ok.

They use ozone for oxidation they did oxidation as different temperatures 200 degrees 350, 400, 450 very short time they did the oxidation and then this ensures that relatively complete oxidation of germanium takes place you have got GO2. So, on the top of that germanium GO2 they deposited in 1 case low temperature oxide is Si O 2 CVd 130 degree centigrade low temperature oxide you can do that is there is a process which you can do at 300 degree centigrade silicon dioxide per plasma it is low temperature low pressure plasma can damage the interface. So, they did that. So, all this samples through at 1 which have done grown at 200, 350, 400, 450 they did low temperature oxide.

Now, first they made their study, this is a low temperature oxide Si O 2 itself and they saw do it a 250 degree centi 200 degree centigrade the DIT across the band gap from the valance band edge right up to the mid gap, let me not worry about what method they were used they are all the same. So, they got interface state density at the valance band edge always it is high you have to worry about near the mid gap that was this is 10 to power 12, 1.5 10 to the power 12 admit gap at 200 that. So, that oxidation was not complete they did at 350 degree centigrade deposited the low temperature oxide Si O 2 made then they put the platinum as the metal gate that is the MOS CV.

So, they got for to 350 degree centigrade that graph this is the one interface state density fell down drastically below 10 to the power 12 telling that oxidation has taking more oxidation taking place it is the direction to go, they mean to 400 degree centigrade even down it went. It went down to almost like 3 into 10 to power 11 more ambitious 450 they went the interface state density went up what could be the reason the germanium dioxide started reacting with germanium releasing germanium oxide interface state density went up. So, as you went on increasing the oxidation temperature 200, 350, 400 it went on improving, but when went to 450 the interface state density started going up.

So, what they did was, let me stick to 4 400 degree centigrade that gives me best interface. So, instead of depositing Si O 2 atomic layer deposition at 130 degree centigrade this is a very slow process as you know you have seen it in our laboratory we can use some precursors layer by layer we can deposit aluminum and oxide aluminum oxide you can put. I am sorry hafnium and oxide a l d you can put, but hafnium oxide. Recently in 2012 they have reported the aluminum oxide also we will see that later. So, today we will just see hafnium oxide think they deposited see then it is did further became better. So, that high k dielectric we do not know what happen there interface is density went down further.

So, this is the interface state density mid gap close to the conduction band, close to mid gap mid gap here this is close to 3 into 10 to power 11 mid gap is somewhere is here 0.66, 0.3 this is the mid gap here, but 450 was higher. So, conduction band is always you see valance band if you go closer it gets up as you see its always like a u curve there is when you go towards the conduction band DIT goes up valance band edge is goes up, but we have to worry about is in the middle because when we go to inversion etcetera it is near that point. So, long as you are able to reduce the interface state density lower value to reduce the interface state density around the mid gap we are in business. So, conduction band edge they showed this that is i, but even that comes down quite a bit telling that almost over the entire band gap they interface state density has got reduced by this process.

When you do the oxidation at 400 degree centigrade, deposit by atomic layer deposition. In fact, whole thing is because this process is even done at lower temperature, this is done at 300 degree centigrade absolutely no chance of reaction of gallium dioxide with the silicon germanium. So, you get excellent interface density there, right through the band conduction band to mid gap all the way it is very low.

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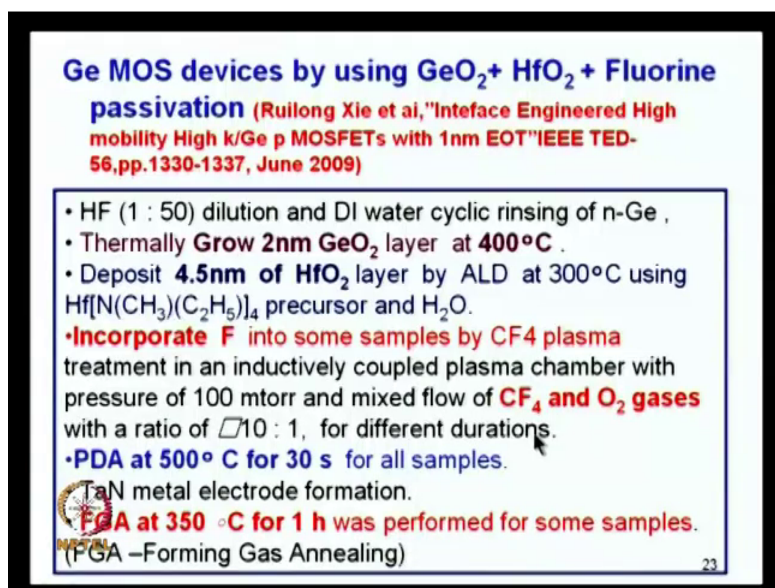

So, I will just go into 1 more thing here this is the one that has been done in 2009 here they did not do that the ozone because it do not have the ozone. So, they did not do that this is the any national university of Singapore, people from Stanford to Singapore we come back closer ok.

So, what they did was Hf treatment they did usual thermally grow 2 nanometer oxide was 400 because they this that results from Stanford give clues at 400 seem to be all right, but may not be oxidation because we are not using ozone look at GO2 2 nanometers that oxide you grow and then deposit 4.5 nanometer of hafnium oxide layer, but atomic layer deposition same, but they did 300 degree centigrade using some other cursor. So, there is hafnium oxide deposition, then after that see they did not use it as it is, they used a metal tantalum hydrate metal that is all a material that is one that they have chosen from work function consideration etcetera. So, they did that metal deposition, but before that they did some other treatment like florin.

See if the key thing that they did will not go through today I will take it up next lecture, but the key thing that they did was they did the thermal oxidation and they did hafnium oxide deposition at 300 degree centigrade they incorporated florin into interface by using in the CF 4 plasma that florin did some passivation of those un dissatisfied interface state and then they did the metallization then they did the forming gas annealing which gave some hydrogen so they got very good results.

I will discuss that in my next presentation. To sum up the key thing to do here is the interface state treatment proper and proper high k dielectric you can get good MOS capacitors here which are where we can make the MOSFETs. That MOSFET aspect we will discuss with some more results for of this type the next presentation.