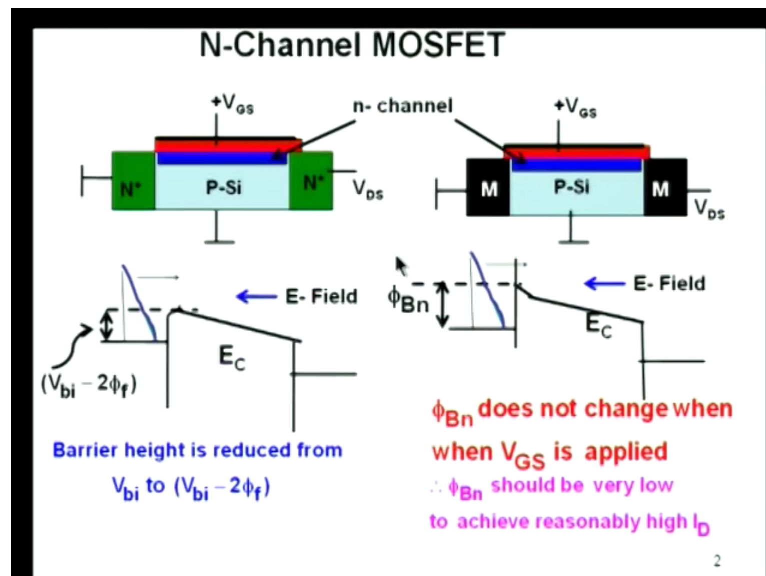
Nanoelectronics: Devices and Materials
Prof. K. N. Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture – 25
Effect of Interface states and Fermi level pinning on MS contacts on SI and passivation techniques for MS S/D MOSFETS

So, we continue our discussion on the metal semiconductor contacts and metal source drain junction MOSFETS.

(Refer Slide Time: 00:24)



So, we discussed last time that in the case of the MOSFET with junctions, P N junction as the source drain, contacts; when you apply gate voltage, the entire barrier height at the source end, reduces by twice phi f. So, because of that electrons are able to inject across that; that is electron distribution in the N plus region. Whereas, in the case of metal semiconductor contact; the metal; the barrier to the metal phi Bn, does not change. When I apply voltage across that; by applying gate V G S plus. In fact, it is this potential barrier V t is changing on the silicon side, not this one. So, as a result this number of electrons which are available for transports from the metal to semiconductor limited; to the those electrons which have energies above the phi Bn; that does not change.

Whereas, in this type of; when there is a N plus P junction that barrier itself changes by two phi f; that is the difference. So, what we see is; if we will not have a large supply of

electrons here, the phi Bn should be small; barrier height should be small. That means, make ideally its make an ohmic contact on to this channel. And of course, the electrons which are injected here; can be rolling down in this because of voltage drop in the channel; it will be connected.

The current will be limited by the supply available here. So, you need to reduce the barrier height phi B n. So, what one immediately think of is phi M minus chi on N type material will give you high barrier height; phi M greater than chi. But if phi M is small; then it will give ohmic contact ideally.

(Refer Slide Time: 02:25)

Summary of the Experimental Results

ϕ_{Bn} can be expressed by the relation

$$\phi_{Bn} = \gamma(\phi_m - \chi) + (1-\gamma)(E_g - \phi_0)$$

Where $\phi_0 \approx \frac{E_g}{3}$ for GaAs and Si ; and it is equal to 0.09eV for Ge. γ Is the *Pinning Factor* and it varies between 0 and 1 , the value depends upon the Surface condition.

(i) γ = 1 expected from the first order theory.

(ii) γ = 0 with freshly cleaved S.C surface.

(iii) γ <1 with chemically prepared S.C surface.

3

But what we have seen is the metal semiconductor contacts, the barrier height on to the N type material; phi Bn is given by this relationship; experimentally one could fit it into this type of curve. So, here you can see; when the gamma equal to 1; what is gamma, we will see shortly. When the gamma equal to 1; the gamma is between 0 and 1 and the gamma equal to 1; the second term is 0. And the gamma is equal to 1; phi Bn is phi M minus chi; that is ideal.

So, if you vary the phi M; you should have the variation in phi B n, but you are not getting that. In some cases, we get phi Bn constant independent of phi M; when the freshly cleaved surfaces. So, this phi naught is actually the; we discussed earlier the neutral level, it is the energy difference between the neutral level and the valence band; for silicon and gallium arsenide that is E g by 3.

And in germanium, it is equal to 0.09; electron volts, band gap is 0.66 electron volts, this is very close to the valence band; this phi naught, we will see it more about that now. So, gamma is called the pinning factor and it varies between 0 and 1. The value depends upon surface condition; gamma equal to 1 expected from first order theory; phi M minus chi; phi Bn is phi M minus chi we saw, if gamma equal to 1; that is ideal. Gamma equal to 0 with the freshly cleaved surfaces; gamma equal to 0 means (Refer Time: 04:09) it will independent of phi M; freshly cleaved surfaces, we saw that phi Bn is constant independent of work function. And you can immediately correlate that; in a freshly cleaved surface, the surface state density or interface density is very high.

So, you could guess that the entire deviations from the ideality is due to the presence of surface states, which we did not take into account in ideal theory. Gamma is when it is between 0 and 1; that is the chemically prepared surface; you get some variation with phi M, but not as much as phi M minus chi.

(Refer Slide Time: 04:50)

Effect of Interface state density on ϕ_{Bn}

•Surface is never ideal and has density of states D_{it} /cm^2/eV due to the dangling bonds on the surface.

•A thin layer δ of material (mostly native oxide) exists between metal and the S.C surface

• δ and D_{it} values determine γ

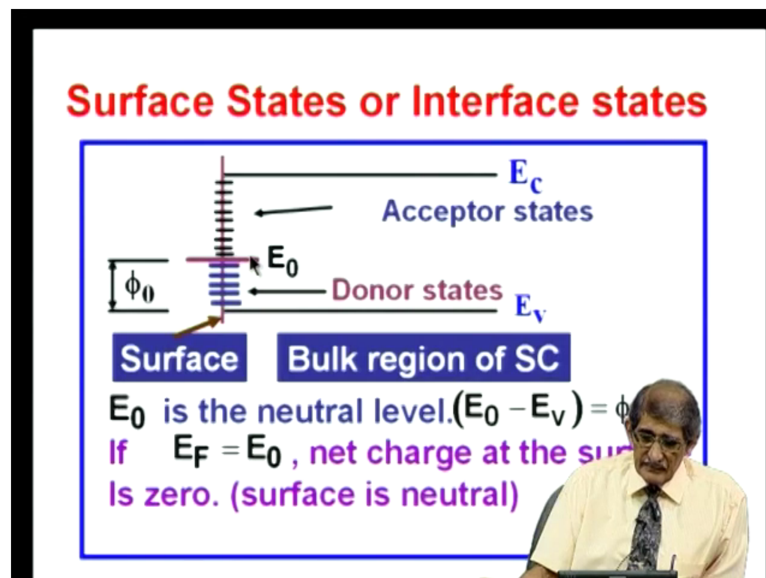
4

Now, let us take a look at what happens here. So, evidently because you get when a freshly cleaved surface gamma equal to 0 or phi Bn independent of the work function indicates that; it is due to the surface state or interface state density. Surface is never ideal and has density of states, which we call represent by D i t; per centimeter squared, per electron volt due to the dangling bonds at the on surface.

Also there is always a very thin layer of native oxide or some absorbed layer; mostly native oxide between the metal and the semiconductor surface. So, if you take a freshly cleaved surface or semiconductor surface and put a metal, that is not directly in contact with the silicon; there is some small gap between them which is a native oxide or some absorbed layer; and that we will call it as delta; may be in nanometer or fraction of a nanometer; of that order. So, D i t and delta t values determine gamma.

So, deviation from the idealities; some thin layer presence and interface density, those who were responsible for giving rise to this gamma. Ideally delta is 0, D i t equal to 0; you will get gamma equal to 1 and you get phi M minus chi; this we have seen in details and I do not have to go through that. So, recap; remember what we have discussed.

(Refer Slide Time: 06:26)

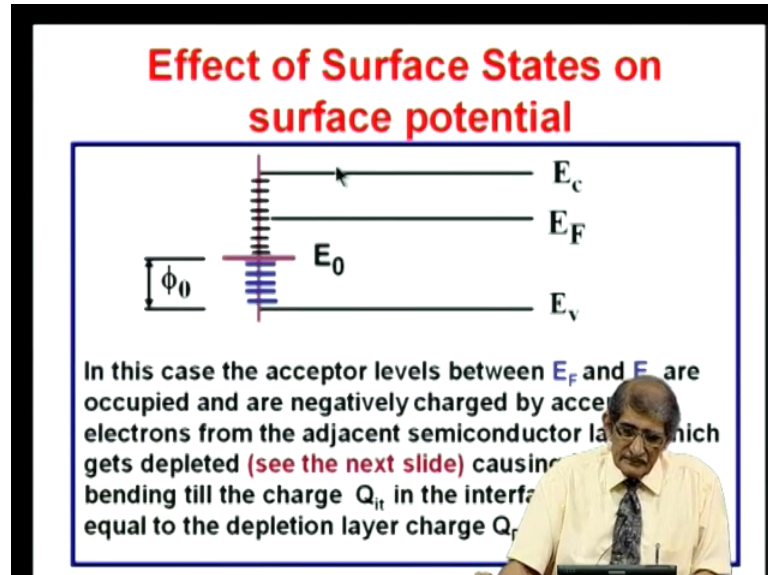


So, if we take surface of a semiconductor, there are lot high density of interface states; unless it is passivated. And they are all donors below a neutral level E naught; above that they are acceptors. If the Fermi level go insides with the E naught due to the doping in the bulk; if the Fermi level go insides with E naught, all the charges donor levels are occupied; that is neutral, all the acceptor levels are not occupied; that is neutral, that is why called; that a neutral level.

And usually we represent the distance between the energy gap between the E naught and valence band at phi naught; that is the phi naught which was coming in that expression. E naught is neutral level; E naught minus E V is phi naught, if E f is equal to E naught; net

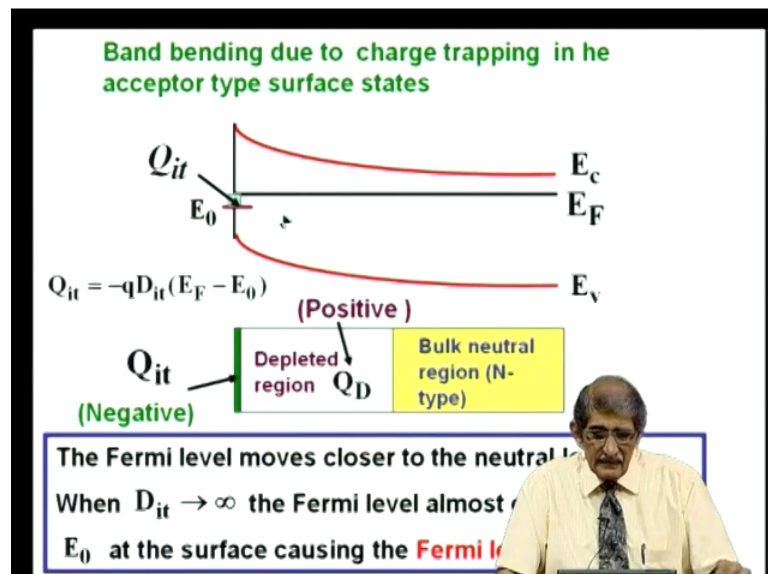
charge on the surface is 0, surface is neutral; this is what we have done. Now in a N type semiconductor Fermi level is there.

(Refer Slide Time: 07:28)



So, all the levels below this Fermi level between the E f and E naught are occupied electrons, they are negative; they are acceptor levels, above the neutral level they are acceptors; when electron occupies that it is negatively charged. And those negative charges have been taken from the bulk of the semiconductor, as a result is it is depleted. So, the actual diagram will not be like this; that will be like that we have seen that.

(Refer Slide Time: 07:56)



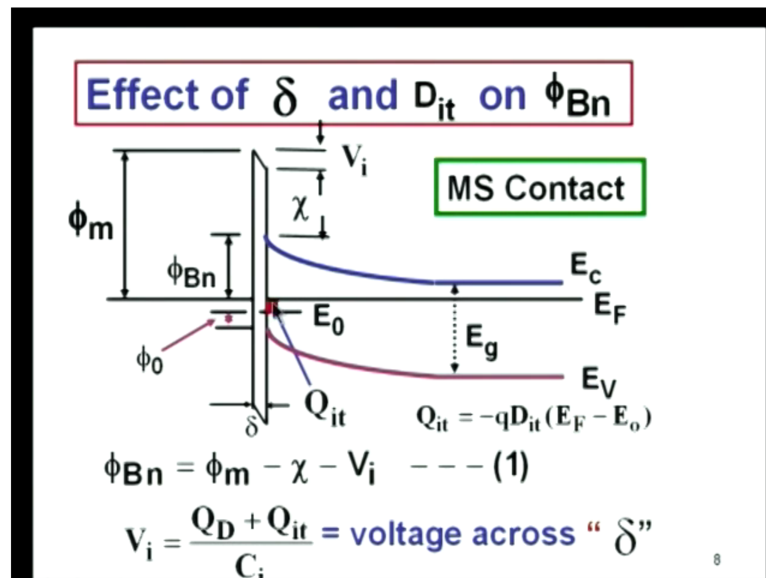
Because the electrons in this surface have been donated from this depletion layer, so here you can see even if you do not put the metal there, the electrons transfer has taken place and Fermi level is getting closer and closer to this neutral level; E naught. And the charge in a interface here for a free surface is equal to Q into D i t; where D i t is per centimeter square, per electron volt. So, this number of acceptors present between E f and E naught are; E f minus E naught into D i t.

So, charge is negative there which is minus Q; D i t into E f minus E naught. So, that charge has come from this depletion layer; so, Q i t is magnitude is equal to the Q D in the depletion layer; which is Q and D into W; W is the depletion layer width. So, you can see that Fermi level more closer to the neutral level E naught. Suppose in the D i t standing to infinity; infinite with a very small gap between the E f and E naught, we will get the required charges from the depletion layer. It can never coincide with the E naught, but it will look at closer and closer.

If D i t is tending to very large value, E f minus E naught tends to 0; that in the sense Fermi level more closer and closer to this E naught. So, you say D i t is very very large, the Fermi level gets pinned to the invert level; that is called Fermi level pinning. So, if Fermi level is pinning, you can see that; this is coinciding with that and the gap between this top layer and this Fermi level, there is a phi Bn; when I put a metal.

So, now that particular formula that you have put there, this one has been derived way back in 1960's still holds good; Cauly and Sze; they have derived that equation for that live using; the assumption that the derivation; just quickly run through that.

(Refer Slide Time: 10:03)



The assumption is that; there is always a thin layer delta and there is always a density of interface states D i t; across the band gap. So, this is that may be simulated oxide, this is the band gap of the conduction band of the oxide, valence band of the oxide. And this is a silicon; you can see that there is band bending here and ultimately on thermal equilibrium, there is Fermi level is flat like this between the metal and the semiconductor it is N type.

So, let us see what happened? This is the Fermi level and that is a vacuum level; that is phi M. Now, this layer is very thin for the electrons have energy above they can tunnel through that; 1 nano mater or less. So, this is still the phi Bn, where the conduction of band is coming to this point. There are large density of states available here; electrons here can cut across into this, they can cross.

Similarly electrons can cross from here to here, when we discuss Schottky barrier theory; we said there is 0 there and it was just a barrier was straight away available there. Now on this side of the semiconductor, there is a depletion layer, which has a charge Q D. And in the interface, there is a charge between the Fermi level and the neutral level acceptors.

So, that is Q i t, this band diagram I have drawn like this; because if I assume that plus charges are there, minus charges are there; there is voltage drop plus to minus there. This can be corrected by the noting the charge afterwards; so, there is a electric field in this direction from plus to minus here and there is a voltage drop equal to V I. What is the

voltage drop across the oxide usually? Whatever charge is here beyond the oxide; surface divide by C oxide; in this case I call it as C i; C interface. So, you have got the voltage drop equal to Q D; there is a depletion layer charge per centimeter square plus Q i t, whatever charge is present in red mark that I have shown between the Fermi level and E naught. So, Q D plus Q i t divided by the C i is the voltage of across of that. This may be small drop, but that effects 0 barrier height phi Bn; see when this layer was not there, we said phi Bn is equal to phi M; minus chi.

Now, it is phi M minus V i minus chi. so, instead of phi M minus chi, we have got a term V i which is the drop across oxide. So, phi Bn is that quantity; so all that we have to calculate is what is V i? Voltage drop across the oxide that is this; Q D plus Q i t by C i; Q D is positive here, Q i t is actually negative. So, if it is negative it may in that way, if Q D is not there; if total charge is negative, the voltage drop will be instead of plus here minus it may go other way; drop will be raising from that that direction.

So, now I have taken this is whole thing is positive; then I put it marked like this. So, I have written this V i; What is V i now? Q D of course, once you know the surface potential, you know what is a depletion layer width is? What is the charge is? But when the interface state density is very high, it will be this term which will be dominating compare to that. Let us see Q i t is this quantity; Q D i t, where D i t is interface density into E f minus E naught; what is E f minus E naught?

Take a look at this band gap, I have assigned this quantity as phi Bn. And this quantity; below this E naught is equal to up to this point is phi naught; E naught below E naught to that band; that is phi naught and that quantity is phi B n. So, we have got E G; minus phi Bn, minus phi naught is f minus E naught. So, from the total band gap here; I subtract this quantity and that quantity I am left with this quantity.

So, this charge in that gap is equal to Q D i t; E f minus E naught, I am putting it as negative because they are acceptors, so that I put it as negative. So, if I do not have Q D; if this is negative, this drop will be minus here and plus here. So, field will be in the opposite direction; upward, so that is taken curve by this sign.

(Refer Slide Time: 15:50)

Expression for ϕ_{Bn}

$$\phi_{Bn} = \phi_m - \chi - V_i \quad --- (1)$$

V_i = voltage across "δ"

$$= \frac{Q_D + Q_{it}}{C_i} \quad --- (2)$$

$$-Q_{it} = qD_{it}(E_F - E_0) = qD_{it}(E_g - \phi_{Bn} - \phi_0) - (3)$$

Q_D =charge /cm^2 in the depleted region of S.C (positive in n-type s.c)

C_i =capacitance of interface layer/cm^2 = $\frac{\varepsilon_r \varepsilon_0}{\delta}$

9

So, that substitute for this V i as minus Q D i t; E f minus E naught by C i. So, what we are looking at is what is phi Bn now; phi Bn is phi M minus chi minus V i, what we wrote written there and V i is Q D plus Q i t plus C i. And Q i t minus is Q D i t; E f minus E naught, that is q D i t E g minus this is what we have just now seen. This is what we have just saw it in; Q i t band gap minus phi naught, minus phi Bn.

See here band gap minus phi naught minus phi Bn; that is the, what is left out is E f minus E naught. So, Q D is charge per centimeter square in depleted region of space charge layer positive in N type silicon; C i is capacitance of the interface layered layer per centimeter square epsilon r, epsilon 0 by delta standard.

(Refer Slide Time: 16:49)

From equations (1),(2) and (3)

$$\phi_{Bn} = \phi_m - \chi + \frac{qD_{it}}{C_i}\left(E_g - \phi_{Bn} - \phi_0\right) - \frac{Q_D}{C_i}$$

Rearranging,

$$\phi_{Bn} = \gamma\left(\phi_m - \chi\right) + \left(1 - \gamma\right)\left(E_g - \phi_0\right) - \frac{\gamma Q_D}{C_i}$$

$$\gamma = \frac{1}{1 + \frac{qD_{it}}{C_i}} = \frac{1}{1 + \frac{qD_{it}\delta}{\varepsilon_r \varepsilon_0}}$$

10

Now, let us go back and see the phi Bn. So, phi Bn is phi M minus chi plus V i; this whole thing is V i that is because this is plus Q D i, that is minus Q D i by C i; this whole thing is minus.

So, this minus stays with that plus charge; this charge is negative, so that becomes plus. So, q D i t by C i it is what I have just now written, this is a V i; due to D i t. Due to Q i t this is that quantity; Q i t by C of i; that quantity. Now, I will not go through that thing; you can actually work it out yourself. This rearranging the whole thing, you can see there is phi Bn here phi Bn here; take them to left hand side and right side, I can write it as phi Bn is equal to phi Bn on to that side, you will have phi Bn into 1 plus q D i t by C i; going to left hand side.

So, you will have phi Bn is equal to gamma times phi M minus chi, where gamma is actually 1; 1 by 1 plus q D i t by that; that is by rearranging that all that you do it take this on to that side. So, you got phi Bn into 1 plus phi; Q 1 plus q D i t by this silicon, let us not worry about that.

So, we get rearranging at gamma phi M minus chi; 1 minus gamma E g minus phi naught, phi Bn outcome back side. So, only E g minus phi naught is there and this term is there that is that gamma term comes in to this particular quantity; because gamma is this quantity. Because when you take it out there, you are dividing right through by 1 plus q D i t by that quantity; that is gamma.

So, now you can see if gamma equal to 0, when will gamma will be equal to 0? D i t is very large when D i t is very large infinity; finite gamma will be equal to 0. So, gamma equal to 0 means, this term is equal to 1 and this is equal to 0; that is equal to 0. So, when the D i t is very very large, phi Bn is equal to E g minus phi naught; independent of phi M because gamma equal to 1; that falls in that supports the equation that we have written there, that is this gamma is related to delta and D i t; C i is that, so it depends upon delta D i t.

(Refer Slide Time: 19:43)

Particular cases

(i) $\gamma = 0$ when $D_{it} \rightarrow \infty$

$\phi_{Bn} = E_g - \phi_0$ Bardeen's limit of φ_{Bn}

This is independent of ϕ_m

(ii) $\gamma = 1$, when $D_{it} \rightarrow 0$ or / and $\delta \rightarrow 0$

$\phi_{Bn} = (\phi_m - \chi)$

This is the Schottky limit of ϕ_{Bn}

11

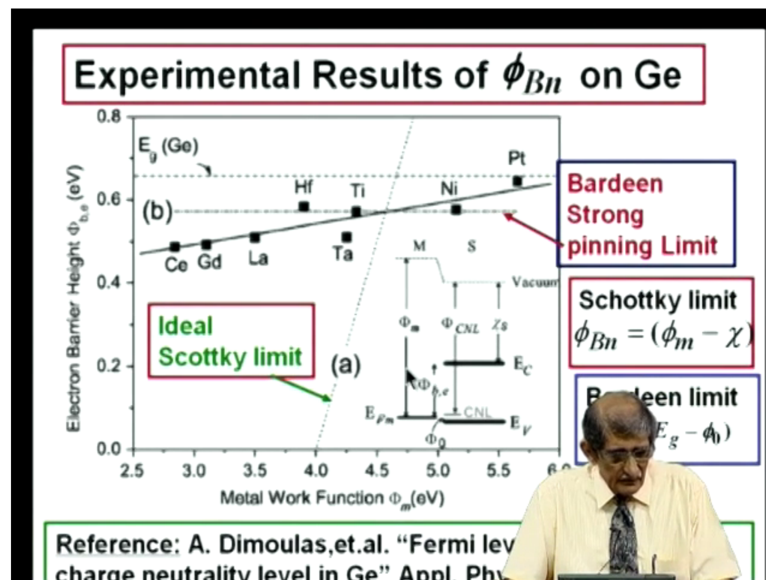
If delta is 0 of course, you will not get anything. So, gamma equal to 0 when D i t equal to infinite and phi Bn is E g minus phi naught, this is called Bardeen's limit of phi Bn; this is independent of phi M. Why do you got Bardeen's limit? The surface states where proposed by Bardeen; who is one of the (Refer Time: 20:06) who invented the bipolar transistor.

In fact, when the MOSFET did not work as expected, he proposed the theory of surface states, interface states and explained the whole thing and that is why those surface state theory is called Bardeen's theory of surface states; over this limit is called the Bardeen's limit, high D i t phi Bn is E g minus phi naught. Gamma equal to 1, D i t equal to 0 or delta equal to 0; ideal phi minus chi that is called Schottky limit because Schottky and Bethe; they give the theory of this Schottky divot and a barrier saying that phi M minus chi is a barrier.

So, ideally Schottky limit on the extreme end, Bardeen's limit. Now you can see if it is ideal then you can vary the phi M and vary the phi B n, but it does not happen. But in the worst case phi Bn is equal to E g minus phi naught. So, what is the result of that? In silicon; phi naught is E g by 3. So, what will be the phi Bn in silicon? For most of the semiconductors, it will be E g minus E g by 3; that is two thirds of E g. So, 1.1 is the band gap; so, you will have the barrier height of a 0.75 electron volts, it will be always be rectifying because its barrier height is high. If the barrier height is low, you would have got ohmic contact. So, if you get rectifying in the case of N type material.

If you make in the P type material; again Fermi level pinning will be there. What will be the barrier height phi B P? Suppose, if this is two third of E g, for the P type material barrier height for holes will be E g minus that. See that is two thirds that is barrier height for electrons, this is barrier height for holes. So, if this is two third E g that is one third E g; so, barrier height for holes will be smaller. So, it will be easier to make P channel devices with metal semiconductor contact because it make semi contact with holes or P channel.

(Refer Slide Time: 22:36)

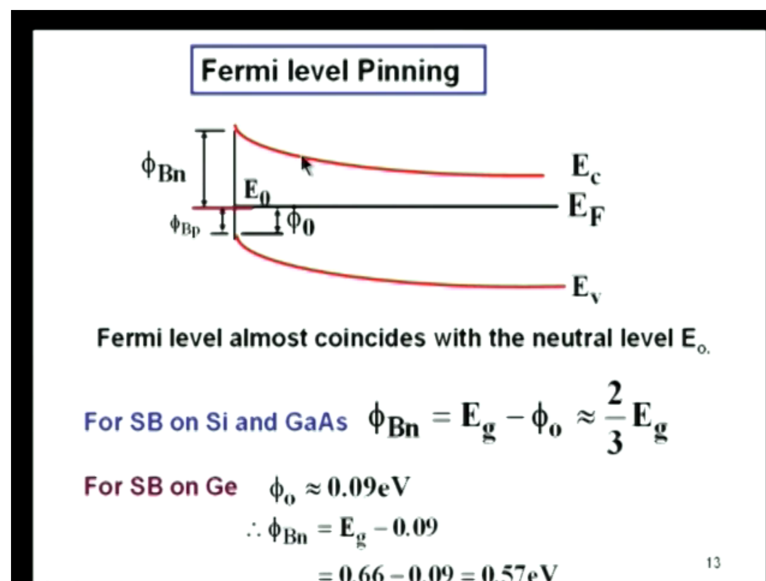


So, this is what we showed for germanium; germanium you see the barrier height for electrons was something like that 0.66 is the band gap and it was very close to the band gap there and the phi M is varied, very little change in the barrier height.

So, in germanium it is a hopeless situation to make a N channel MOSFET because it will form a barrier height which equal to; very close to the band gap. Band gap is 0.66, phi naught is 0.09; so, very close to 0.6 electron volts. So, it will be very bad situation to make N channel device, but anything you deposit on germanium, you will make ohmic contact. Because barrier height is very small for holes, so you will have; it will be very easy to make P channel MOSFETS with metal semiconductor at contact in germanium.

That is good news for people who want to make germanium P channel MOSFETS. So, if you want to get N channel MOSFET to germanium or silicon, you have got to do something else. So, that is just see what are the situation there.

(Refer Slide Time: 23:56)



So, this is a Fermi level pinning which I am talking of; in the case of gallium arsenide etcetera; it is two third of E g phi Bn. In the case of germanium, phi naught is 0.09; therefore, phi Bn is about 0.57. So, rectifying always you put a metal on these semiconductors, it will make rectifying contact. So, it is very very easy to make Schottky barrier divots from on N type N type materials and it is very difficult to make ohmic contacts that.

(Refer Slide Time: 24:26)

Effect of Fermi level pinning

Almost all metals form rectifying contact on N-type Si and GaAs: They form lower barrier height contacts (Ohmic Contacts) on P- type Si and p-type GaAs.

It is easier to realize P-Channel SB S/D MOSFETs than the N-channel SB S/D MOSFETs on Si , GaAs and Ge

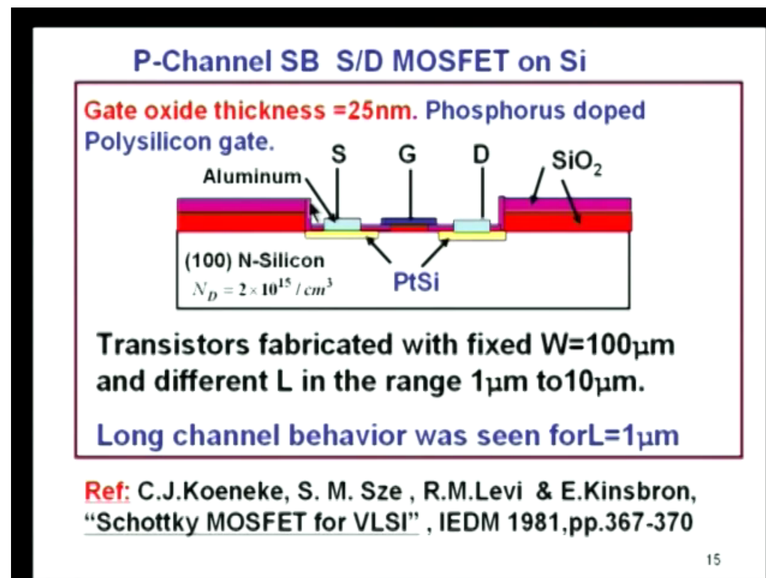
- Almost all metals tried so far have formed ohmic contacts on P-type Ge ; they form high barrier contacts on N-type Ge.
- It is easy to realize P-channel SB S/D MOSFETs on Ge ; but it is difficult to realize N-Channel SB S/D MOSFTS on Ge

14

So, effect of Fermi level pinning almost all metals formed at rectifying contact on N type silicon or gallium arsenide and also on germanium. They from lower barrier height contacts; that is ohmic contact on P type silicon and P type gallium arsenide. Therefore it is easier to realize P channels Schottky barrier or source drain MOSFETS than N channel Schottky barrier source drain MOSFETS on silicon snd gallium arsenide and germanium.

Because N channel make it a high barrier height, so number of electrons which are available for supply into the channel; will be limited by this; go back to this one if you see; see this barrier height is high here number of electrons which are available, which can cross the barrier are reduced less; that is a problem. So, normally when you put a metal; it become rectifying unless you take care of do something to this surface to unpin that Fermi level.

(Refer Slide Time: 25:46)



Now, let us quickly go through some of the thing that are there; like the P channel Schottky. First of those; way back this was done by Sze and Koeneke, platinum silicide; metal semiconductor contact at the source this is not N plus or.

So, once you see that you can make easily ohmic contact on to the P type materials, if it is a P channel transistor platinum silicide can make ohmic contact on to that; that is low barrier height for holes. So, people thought of making let us see P channel Schottky barrier source drain MOSFET on silicon. They made that; same approach gate oxide about 25 nano meters, we are talking of 1981.

So, gate oxide 25 nano mater and phosphorus poly gate, I shown it as a metal, but it is phosphorus doped; polysilicon gate, they have used that. And then what they did was they transit a width of W and a channel length was L; 1 microns to 10 microns, various lengths, long channel behavior seen in for L is equal to 1 micron.

(Refer Slide Time: 27:23)

Process steps for PtSi S/D MOSFET

- Phosphorous doped Gate polySi was deposited, patterned and its sides were protected by deposited SiO_2.
- SiO_2 was removed from source and drain areas.
- Approximately 15 nm of Pt was sputtered and then sintered at 625°C for 30 minutes in Argon to form 30nm of PtSi over all the previously exposed silicon region. PtSi forms $\phi_{Bp} = 0.24eV$ with holes in Si
- The un-reacted Pt was then removed with aqua regia

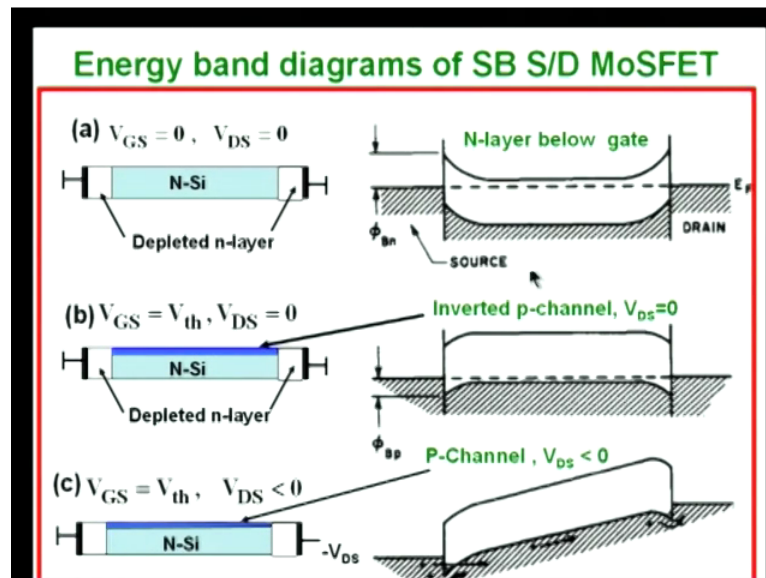
16

So, N type silicon 10 to the power of 15; I will just go through quickly phosphorus doped gate polysilicon was deposited patterned and its sides were protected by deposited SiO 2; first the gate was decided, sides are protected SiO 2 was removed from source and drain regions, where you want to put this contact SiO 2 was removed. Approximately about 16 nanometer of platinum was sputtered and then sintered at 625 degree centigrade for 30 minutes; in argon to form platinum silicide.

In fact, it consumes silicon that is why it is shown here as getting inside into silicon, it consume silicon and you get about 30 nano meters of platinum silicide. Over all the previously deposited silicon region; wherever it is a exposed you will get that platinum silicide, other places it is no silicon there is no platinum silicide. So, what you do is the unreacted platinum was removed by aqua region or you can use some reactive plus match in.

Phi B P; the nice thing about that is phi B P is very low with holes or with P channel that is barrier height is low; that is about 0.24 electron volt, this is close to the Fermi level pinning type. So that means, actually you can make transistor working transistor because barrier height for holes is very very small, there are supply of holes is very much.

(Refer Slide Time: 28:58)



Now, let us just quickly take a look at it; the energy band diagram, if you like that is the N type silicon; there is a platinum silicide contact here, there is a depletion layer here. So, N type is bend no gate oxide or no voltage applied to the gate that is a depletion layer, that is a N type region, that is a conduction band, this is a valence band; this you to show the valence band.

Now, when I have a metal oxide over that and if I apply a plus voltage to that, this surface here the surface if take the energy band diagram; that will be inverted. N has become P; this is very interesting diagram please take a look at that, there it was like that. I have not applied any drain voltage still it is thermal equilibrium situation there. So, that is the Fermi level and here this metal semiconductor contact, there will be depleted layer here just in this; P and this metal and P channel it is like a metal and P type semiconductor; its equivalent of that because there will be depleted layer there small layer will be there; there is a divot it is a P channel with a metal semiconductor contact; metal and P all most equivalent of that, you have got a slightly depleted layer.

This is energy band diagram; now if I apply voltage to the drain; a P channel device I want to collect the holes, negative voltage to drain. If I have a 90 voltage to the drain; this energy band diagram is not in the bulk, it is here in the top. Here it is still N type; from the top only I am drawing the diagram. So, what happens to diagram? Minus here plus here.

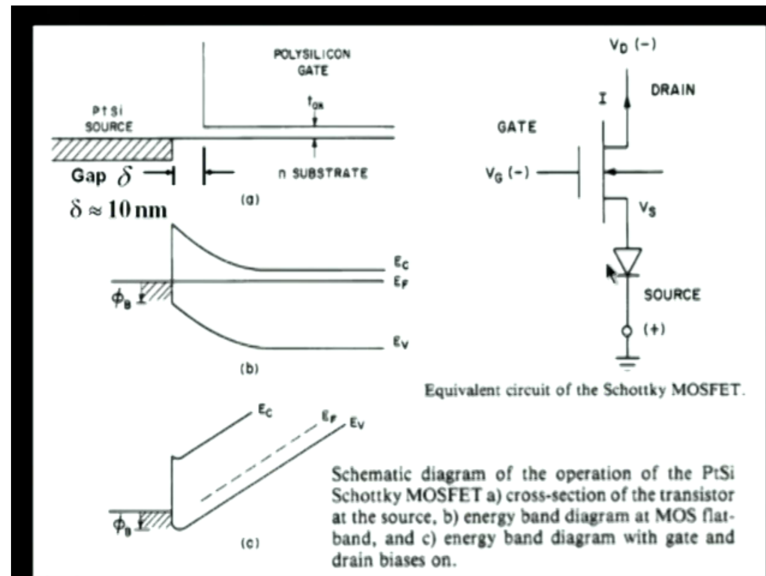
So, across this shaded region is actually the inverted P layer, there is a drop plus to minus. If there is a plus to minus here; there is a small depleted layer there, there is a N P divot; energy band diagram bends; you know it is more difficult to take electrons from plus to minus; that means, the energy band diagram will be higher on this side. So, it bends upwards from the left hand side to the right hand side.

So, indication is minus there and plus here now whatever holes which are injected band and go through this. How much is collected here it, depends upon how much is a volt taken on the channel and if this is small that can supply that; if this barrier height is large, it cannot be supply that; current supply will be limited. That is why this sort of device has worked, but what they saw was; the output currents in a Schottky barrier in MOSFETS were found to be smaller than those for conventional MOSFET.

If this were P plus region, you would have got more current than that. The whole thing is because from part of the applied voltage goes into this one, see this divot if you recall I do not know whether you are able to recall that. When I have no bias across that; the whole injection from here and here will be cancelled in each other. If I have net hole injection from here to here, I must reduce the barrier, I must reverse bias that. That is minus here plus here; so, part of the apply voltage will go to this junction plus minus here, so that this barrier is increase this is brought down there.

So, when we have a I do not know whether you were remember; see if you go to this one, N type if you take see if I do not have some drop here; across this layer there, here it is plus and minus the electron injected from here and here is the same thing; I must have a plus voltage here, so that this is metal N type region is reversed biased. So, that this is brought down a bit, so electrons cannot be injected from here to here. All these (Refer Time: 33:27) are transfer injected backward. Same argument holes could for the case of P channel device, instead of plus minus it is minus plus. So, part of the apply voltage will go into this junction; so, the full thing is not available for that; for a current trans volt.

(Refer Slide Time: 33:52)



So, now; so you get equivalently you can put this as this is a inverted diagram this is before emersion, this is after inversion the whole injection from here to here is possibly; there is some reduction or the barrier on this side. So, this portion you are putting it as a divot; in fact, what happens is the applied voltage minus here is appearing across the some part, it goes into this region minus here and plus here means its reverse biased..

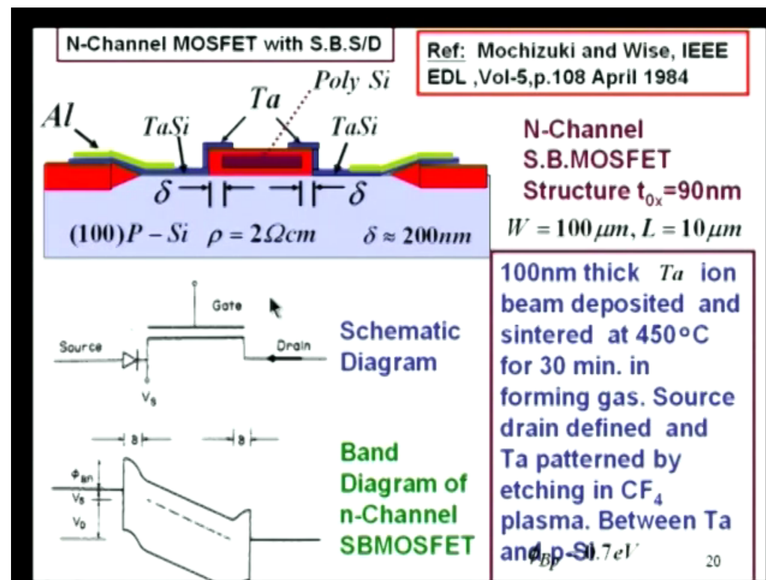
The divot when it is reversed; see that most important concept in Schottky barrier is if it is a N type material, it can inject electrons from the metal to semiconductor if it is reverse biased. When it is forward biased, injects electrons from the semiconductor to the metal. The P channel device, it can inject holes from the semiconductor to the metal if it is reverse biased. If it is forward biased if it can inject electrons holes from the semiconductor to the metal; so, this will be reverse biased condition minus plus. So, applied voltage gets shared between this and this; so, part of the voltage goes there, more and more voltage is get reverse biased more and more carriers can be injected across the barrier. So, I think that is you bring one of the barriers; this barrier is not changing only this barrier we can reduce; that is you can bring it down.

So, that the electrons which are distributed above that; their level is brought down. There is no injection from the right to the left, but this barrier is not changed; so, there will be electron injection carriers from here either holes or electrons. So, in either way a reverse

biased voltage would appear across; which comes from the drain itself. The part of the voltage will go to that, so current available for conduction will be reduced.

Or devoted in more emphatic way, number of holes available here is depends upon the how much lower the barrier is; less the barrier, more holes are available. So, the current in these cases also was observed to be lower than what it is. So, the key thing in these devices is to reduce the barrier height; the P channel.

(Refer Slide Time: 36:22)



Now, let us see whether people have tried to do something about the N channel devices. So, what they did here they fabricated N channel devices; they used a tantalum; phi Bn is phi B P is 0.7 electron volts; the phi B P is large there; phi Bn is small there.

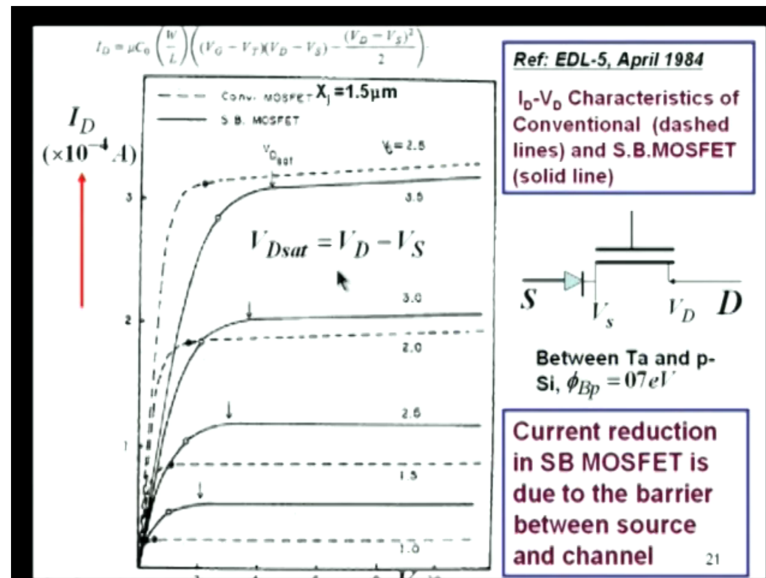
So, they were hoping that they can just have some sort of Schottky barrier. So, they made its a same way they have done the thing, you can see that the N channel Schottky barrier MOSFET structure t oxide 90 nanometer; L 10 micron meter, they are not worry about short channel effects etcetera. 100 nanometer thick tantalum ion beam deposited on and sintered at 450 for 30 minutes in forming gas.

Defined by etching in the; to define this portion after forming this gate region polysilicon, exactly same way before you open a contact; tantalum, sputtered, annealed in forming gas; that forming gas annealing has slightly passivated those interface states. So, because of that they could get some sort of MOSFET action. So, that is what; so you

can see now when you invert it and if I apply plus voltage to drain; that is the energy band diagram; conduction band, valence band.

I hope you understand this in the previous case you had the band diagram going up there because plus to minus, here it is minus to plus take this plus; the N channel device.

(Refer Slide Time: 38:18)



So, same problem they had ideally if you can get the MOSFET characteristic like this; they got same equivalent circuit the MOSFET with the divot, which is the source channel divot. In the previous case it was, P 2 metal in that case it is metal to N; divot is reversed that is a divot. Now you can see when I apply plus voltage, plus minus, plus minus this is a reverse biased. When it is reversed biased, it enables electrons we injected from the source to the channel, but for the electrons we injected from source to the channel; that must be a reverse biased across that, that comes from this applied voltage. So, part of the applied voltage goes into this divot that is why in the ideal MOSFET, you may get the characteristic like that.

But ideal means the source and drain defused in the metal semiconductor contact, there is for the same current you have to go apply higher voltage because part of voltage has gone to this V S because that is a V D minus V S is double. So, you can same equation that you use for the MOSFET. So, they did get MOSFET action, but lower currents or you apply more drain voltage for that; this is to the barrier between the source and this channel; this thing that they observed.

(Refer Slide Time: 39:55)

•The diode is formed at the source – channel edge and the Schottky barrier. V_S is the bias required to accommodate the current I_D

•Once the lateral voltage drop V_S is established at this diode, current will flow as for a reverse biased metal n-Silicon Schottky diode.

• Barrier height can be calculated independent of I_D

$$I_D = [A A^* T^2 e^{-\phi Bn / kT}](1 - e^{-qV_S / kT})$$

$$I_D = \mu c_{ox} \frac{W}{L} [(V_G - V_t)(V_D - V_S) - \frac{(V_D - V_S)^2}{2}]$$

A is the effective area and A* is richrdsons constant

22

Now, you can write the equation I D; so, you can see the drain current, we can write in sums of the potential drop across a channel. What is the potential drop across a channel? V D S minus that V of S; source is not 0 because part of it gone to that. So, V D S minus; so in the linear region you will get mu c oxide W by L; same as MOSFET equation into V G minus V threshold into V D S you write.

But V D S in this case V D minus V of S; V of S is the top across the divot that is the Schottky divot which is between the channel and the metal. Minus V D S square by 2, but V D S is V D minus V of S. So, you can see this entire thing is smaller than what you will see for a given V D. And just notice, this is the current which is collected by this voltage across the channel; V D minus V of S. So, whatever current is flowing through a channel is supplied by the source. What is a current supplied by the source? The reverse biased current of the divot correct because across the barrier. So, that is why the reverse bias volt keeps on increasing as increase that and it supplies more and more current. But at each point; whatever is the V of S is the reverse biased voltage across the divot. What is the reverse current across the divot? A; A star T square, this quantity into 1 minus this quantity; when V S is very very large that goes down to 0 and you get the I naught.

So, maximum that you can get is the I naught of the divot. So, I naught of the divot will be unlimited if it is ohmic. If the barrier is very small, you can have large I naught. So, whether it is controlled by this Schottky divot reverse current or by this MOSFET action

depends upon the barrier height. So, lower barrier height is a key thing for this entire MOSFET thing. So, just let me quickly go through some of the thing that latest things which are there, before I wind up these thing. So, they have tried verities of materials.

(Refer Slide Time: 42:32)

Silicides of other Materials for N-channel Schottky Source Drain Transistors (SSDT)

- P-Channel SSDT (P-SSDT) with PtSi as S/D (hole barrier $\phi_{Bp} = 0.24 - 0.28$ eV has been reported with quite acceptable $I_{ON}/I_{OFF} \approx 10^8$
- N- channel SSDT performance has been rather poor due to the high barrier height for electrons
- Materials with low ϕ_m are required for achieving low ϕ_{Bn}

Material (silicide)	Erbium ($ErSi_{2-x}$)	Dy ($DySi_{2-x}$)	Ytterbium ($YbSi_{2-x}$)
ϕ_m (eV)	3.12	3.09	2.59
I_{ON}/I_{OFF}	10^5	10^5	10^7

23

You know desperation on this thing because to get down to this because it has several advantages. Silicides of other materials for N channel Schottky source drain transistors have been tried. For P channel devices platinum silicide is very good, way back 1981 itself demonstrated tried to give this 0.24 to 0.28 phi B P for P channel devices, you get I on off about 10 to power 8.

So, P channel devices indicates of silicon is no problem, from the same token what about P channel devices in the case of germanium? What will you say? What is the barrier height there? Here is 0.24 and the Fermi level pinning is there in the case of P channel device or P types of state, it is 0.09 is barrier height very very small. So, excellent ohmic contact you can get for germanium, excellent P channel MOSFET can be made with germanium; that means, very good news for germanium people.

Because germanium has got whole mobility, much larger than that of whole mobility in silicon, so, you can think of germanium P channel MOSFETS. But then if you get low barrier height for holes on the same token you will say that barrier height for electrons is high very difficult make N channel devices.

We will get done to those things either in this lecture or when we go to germanium devices. So, here with silicon was the desperation they have erbium metal reaches phi M of that quantity, they got fairly good ion of ratios, ytterbium gave much smaller barrier height. So, ytterbium was the one that they advocated for N channel, P channel no issue; P channel platinum silicide; ytterbium silicide.

(Refer Slide Time: 44:25)

Reference: Shiyang Zhu, etal " N-type Schottky Barrier Source /Drain MOSFET using Ytterbium Silicide" IEEE Electron Device Letters, vol.25, pp51-565-567, August 2004

- $ErSi_{2-x}$ SSDT resulted in poor film morphology formed by solid –state reaction of deposited Er and substrate Si and has shown poor On/Off ratio . It also showed two slopes in sub-threshold region and high electron barrier height $\phi_{Bn} = 0.37eV$
- $YbSi_{2-x}$ resulted in better surface morphology , with on/off ratio of about 10^7 and $\phi_{Bn} = 0.27eV$

24

So, those are thing which they have tried out and ytterbium gave about 5 Bn of about 0.27 some sort of accepted devices, they were fabricated there of course, they had to make some passivation using that forming, gas annealing etcetera, but not enough you have to get better.

(Refer Slide Time: 44:47)

Summary Of SB S/D MOSFETs on Silicon

- The principle feature of SB-CMOS technology is metal S/Ds.
- Metal S/Ds are inherently lower resistance and atomically abrupt, providing a long –term scalability advantage.
- The metal S/D junction to the channel forms a SB, which provides improved I_{OFF} leakage control. It further enables lower doping in the channel region, which results in higher channel mobility.
- SB junctions eliminate parasitic BJT action and latch up and are much less sensitive to radiation effects that induce soft errors.

25

So, in summary of these about these things quickly go through because I have few more things to discuss. The metal source drain are inherently lower resistance; these are all we have discussed already; low resistant you can get when you use metal source drain, metal source drain junction to the channel from Schottky barrier, its forms all these. Schottky barrier junctions will make parasitic BJT; we have already discussed that, this is not summary of my talk, but again advertisement for this Schottky barrier devices.

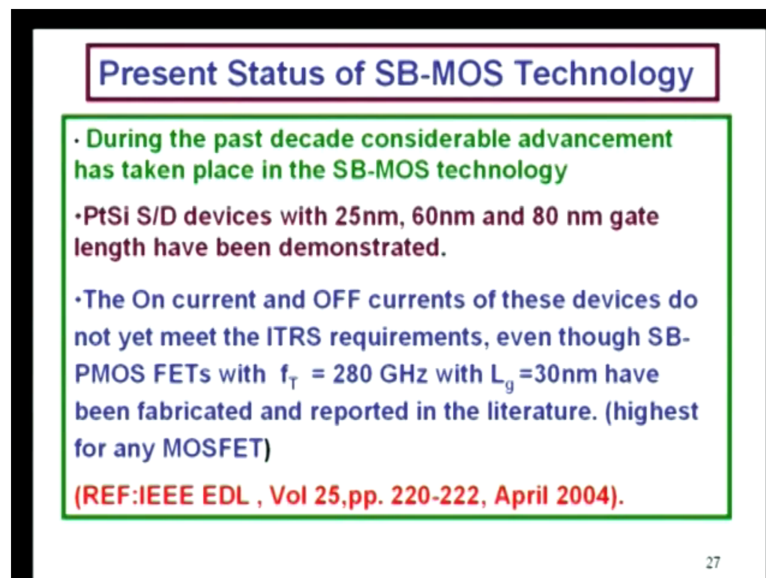
(Refer Slide Time: 45:24)

- Low-thermal budget process enables integration of performance- enhancing materials such as high-k gate dielectrics, metal gates, and strained silicon , all of which lead to other substantial advantages such as reduced gate leakage, lower power, and higher effective carrier mobility.
- Together , these features and benefits make SB-CMOS technology an attractive candidate for scaling to sub-25 nm gate lengths- coupled with SOI approach promises scaling down to 10nm

Also low thermal budget to make the metal contact on to the source drain, you do not have to have high temperature diffusion. And if it is low temperature, Schottky it is excellent to make high-k dielectrics; that is why people are looking at metal semiconductor source drain. High-k dielectric when you put you may realize that gate etcetera, we can even go for metal gate then afterwards source drain you do not want to do diffusion, you want to do at low temperature.

We can use that metal semiconductor contact, so that is why people are looking more and more into that in nano scale devices. Together these features and benefits make Schottky Barriers CMOS technology and attractive candidate for scaling to sub nanometer below 25 nanometer; coupled with SOI approach from results down to 10 nanometer.

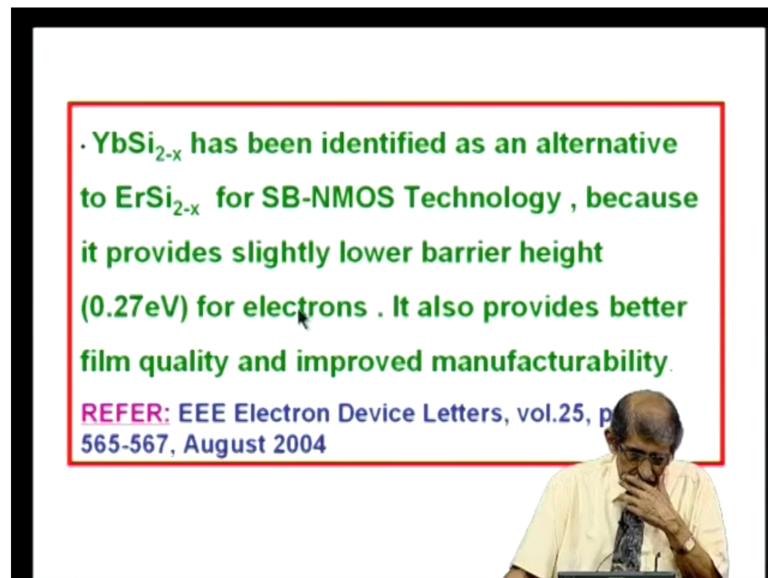
(Refer Slide Time: 46:22)



Now, present status I just have some of the things from 2004; right up to recent ones. Considerable advancement has taken place in Schottky Barrier MOS theory for the past decade. Platinum silicide, source drain devices with 25 nanometer; all those things have been demonstrated mainly for P channel. The on current and off current of these devices do not admit the requirements ITRS requirements, even though Schottky barrier MOSFETS with 280 gigahertz.

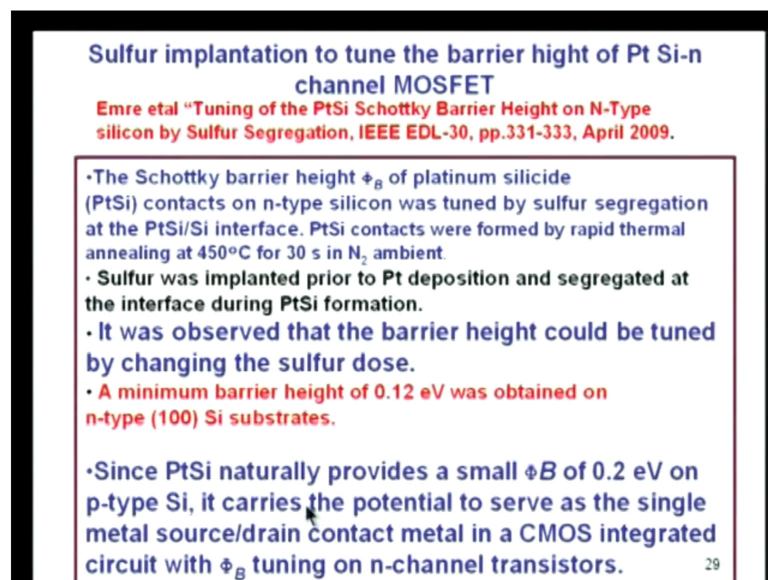
30 nanometer gate lengths have been fabricated; even as early as 2004; P channel devices have been fabricated highest for any MOSFET because of that low resistance etcetera; P channel not N channel.

(Refer Slide Time: 47:24)



Ytterbium silicide has been identified as an alternative to other materials because barrier height is low.

(Refer Slide Time: 47:47)



So, that is one of thing people have been looking at to some degree of success. Now there is a small etch, you may be able to make N channel MOSFETS with ytterbium with 0.27 phi Bn. But if you use the same approach for P channel device; phi B P is large because phi Bn, if it is small phi B P is large because you know that phi Bn plus phi B P is E G. So, you will end up with large barrier height for the P channel.

So, you should not make C MOS, you must have the ability to overcome this problem not by adjusting the work function. You must have the ability to have both phi B P under your control and phi Bn under your control.

So, if I am using platinum silicide as contact, I can make P channel MOSFET without any difficulty because barrier height is very small; 0.24 electron volts, even in germanium I can make it very small because this is very very 0.09 Fermi (Refer Time: 49:07). So, the Schottky barrier height phi B of platinum silicide contacts on N type silicon was you can tune that.

If you can tune that barrier height by sulfurous using sulfur as a passavant or implanting sulfur, you are in business because you; let us see how this is done. The contacts on N type silicon was tuned by sulfur segregation, at the platinum silicide silicon interface. Platinum silicide contacts were formed by a rapid thermal annealing at 450 degree centigrades or 30 seconds in nitro ambient.

So, what is done is take N type substrate to study this if you want to make N channel you have take P type and implant sulfur. Sulfur was implanted to prior to platinum deposition first implant sulfur and segregate at the interfere during platinum silicon formation. You implant sulfur, deposit platinum, anneal at 450 degree centigrade; rapid thermal annealing.

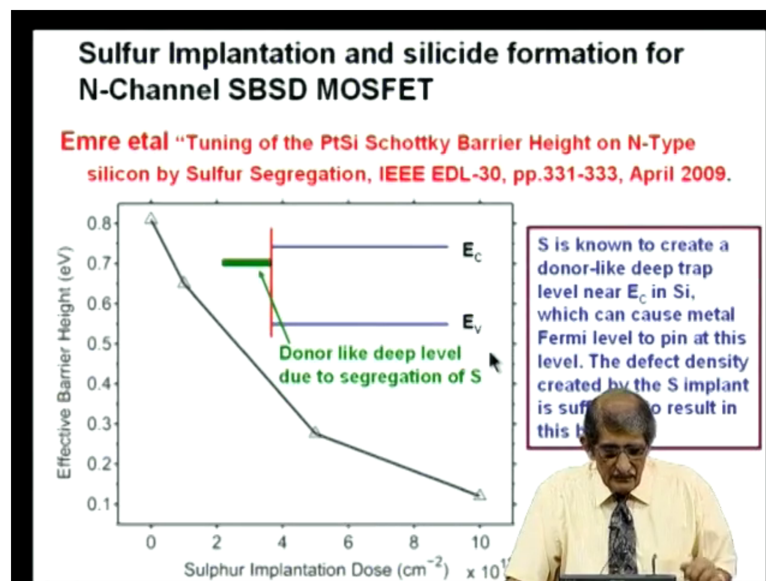
What is rapid thermal annealing? Take the temperature very quickly; spike 30 seconds bring it down. If you keep long enough in at 450 degree centigrades, the sulfur may come out. Now what happens is its just segregating into interface; platinum silicide is formed it is just segregating. Segregating means it is getting cluster sulfur at the platinum silicide silicon surface.

It is observed that barrier height could be tuned by changing the sulfur dose. A minimum barrier height up to 0.12 electron volts was observed on N type 100 type of interface; that is very good news. See if you do not implant, you get a barrier height of how much; 1.1 minus 0.24; so, about 0.8 or so, 0.6 or so, barrier height, but on P type you get 0.24 or 0.2 to 0.24 electron volt low barrier height, on N type I can adjust the dose and get the low barrier height.

That means, I can make N channel devices on that. Since platinum silicide naturally provides a small phi B P; this phi b as (Refer Time: 51:39) phi B of 0.2 electron volts; on P type silicon, it carries the potential to serve as single metal source, drain contact metal on CMOS integrated circuit, I hope you understand that. Same platinum can be used in the regions where you want to make P channel MOSFET; do not implant sulfur.

You get a barrier height which is phi B P low for the P channel; 0.2 electron volts. In the region where you want to make N channel devices, you implant sulfur; you can control that barrier height by controlling the dose of sulfur. So, you can make low barrier height for N channel.

(Refer Slide Time: 52:24)



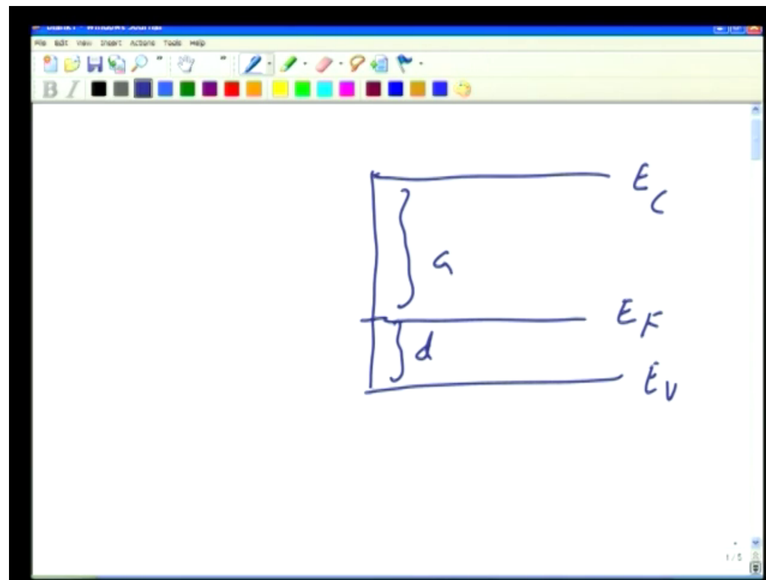
So, what happens there? Why this sort of (Refer Time: 52:28)? You are moving the; changing the location of that pinning. So, this is one of those papers which appeared in 2009; N channel Schottky Barrier Source Drain MOSFET; Sulfur Implantation and silicide formation for N-channel devices During of platinum silicon Schottky barrier; height on N silicon by sulfur segregation.

So, sulfur implantation dose per centimeter square 2 into 10 to power 13; 4, 6, 8, 10; 10 to the power 14 per centimeter square. Barrier height originally is 0.8; if you do not implant, if you take N type material and make platinum silicide; it is about 0.8. But for different doses barrier height is reduced even very small, you can reduce that. What they have observed is sulfur is known to create donor like deep trap level near the conduction

band of silicon. See this is actually what I have shown as a density, a clustered region of sulfur donor levels.

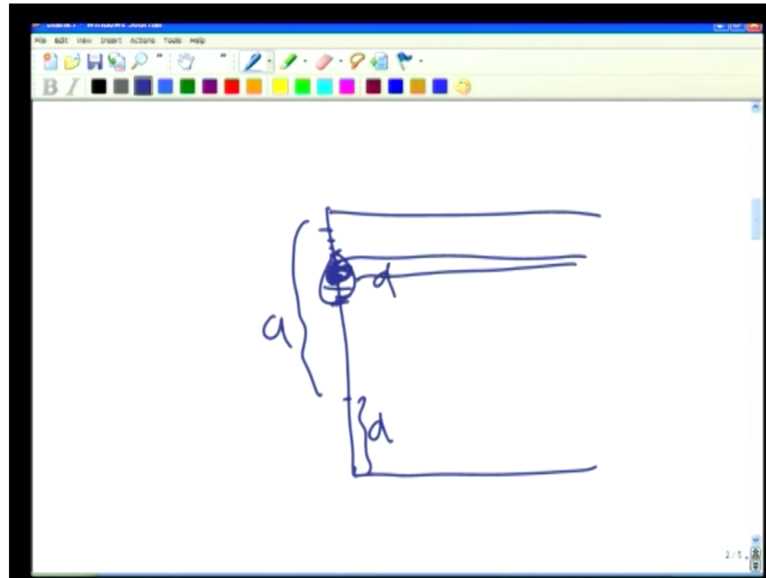
Here, see if you take usually what you do is; you have the energy band diagram like that conduction band, valence band.

(Refer Slide Time: 54:06)



You have the neutral level here, you have all these are donors, all these are acceptors. The Fermi level always tends to get pinned to the neutral level; to balance everything. So, that is why Fermi level goes here; in this portion that is a E F gets through pin to that, but now in this case what you are doing is; you are what you do is.

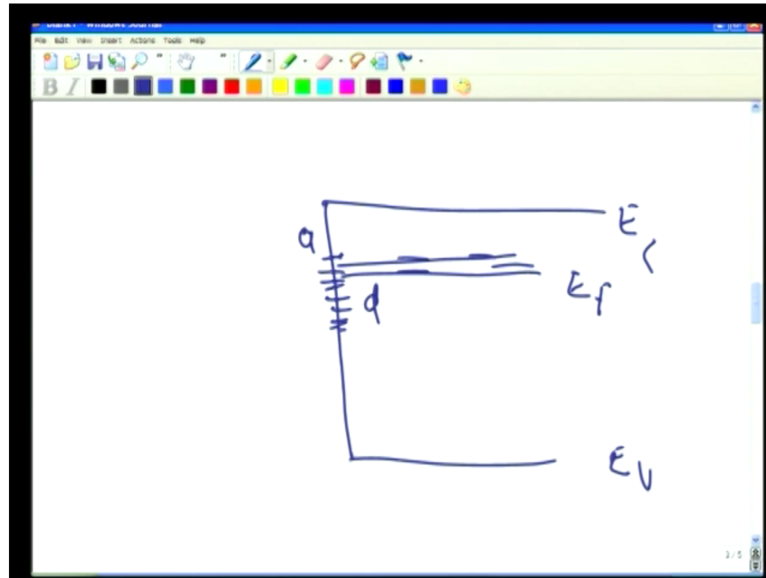
(Refer Slide Time: 54:52)



You have this energy band diagram like this, you have large density of sulfur which are donors there. So, you have got originally you had all donors here and all acceptors there, now there is a large density of donors here; much more larger than that 10 to the power 14 etcetera are implanting. So, Fermi level gets pinned on to this portion how much this is actually not like that; in fact, it will be distributed like this donor levels.

So, Fermi level gets pinned on to this portion where density of donors are very large; even compensating all these things. It is equivalent of saying, you have got donor levels here the acceptors here and donor levels here. So, Fermi level go into that portion let me put it down again, it may put it more clearly.

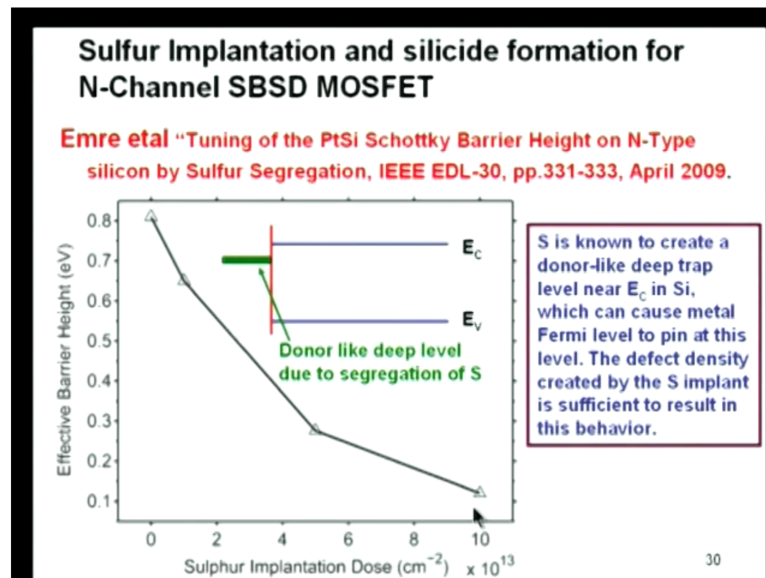
(Refer Slide Time: 55:55)



That is the conduction band and that is a valence band, then you have got donors large density of donors here; they are acceptors. So, you can say that neutral level is actually somewhere here; this is much more than this donor which are present. So, your Fermi level actually gets pinned down to this point that is; how much it is there depends upon how much sulfur implanting.

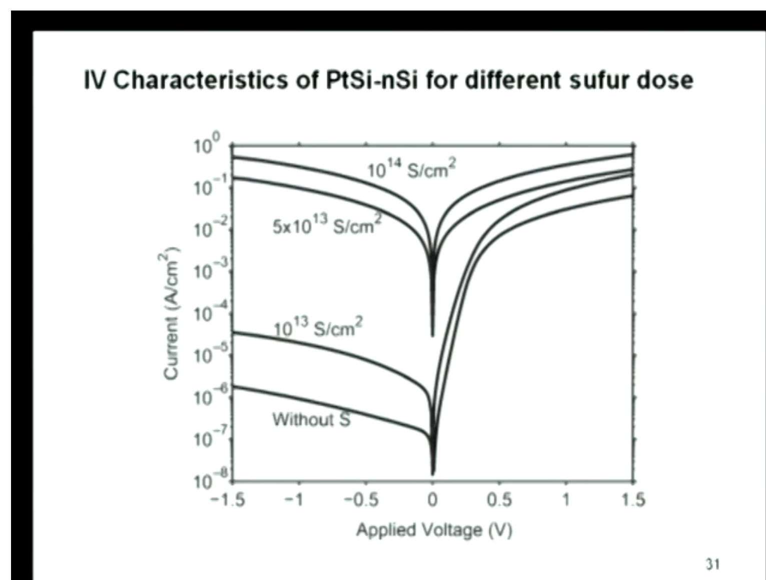
More you implant displaced more and its moves up here. See from the Heisenberg theory or the note two levels can exists; simultaneously if you more implant more sulfur; more number of (Refer Time: 56:44) they cannot exist in the same place, it will spread out. So, that is why it is moves up there and you got the Fermi level closer to closer conduction band.

(Refer Slide Time: 56:55)



So, you are able to reduce this barrier height by putting more and more of those; I think I should take this off more and more of those sulfur atoms.

(Refer Slide Time: 57:16)

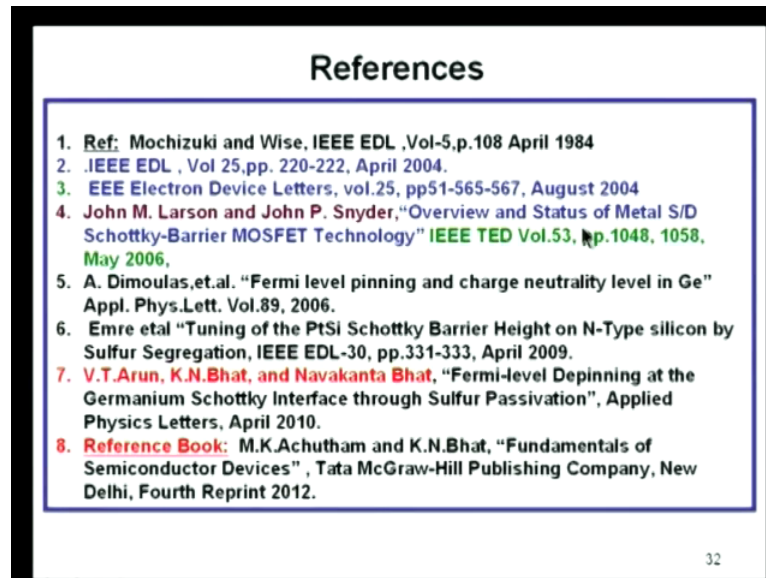


So, this is the I V characteristics of those Schottky barrier divots; see when without sulfur, this is lave scale please remember 10 to the power of minus 6; ampere per centimeter square that is the forward characteristics; sulfur 10 to the power 13 reverse current has increased, forward also has increased 5 into 10 to the power 13; reverse

current these 0; lave scale large reverse current, large forward current, large 10 to power 14 very close to ohmic contact.

Now though ohmic contact will be symmetric on lave scale, the linear scale it is like that. So, this is what will happen in this case.

(Refer Slide Time: 58:05)



So, what I am trying to point out here is; the sulfur passivation has been the key thing people have been trying out. In fact, even in germanium it can be tried out; so, lot of references are there, which have come over the years 84 and all 2004. In fact, some work has been done here also on sulfur passivation.

One of our M S students Arun (Refer Time: 58:32) Navakanta Bhat; Fermi-level Depinning at the Germanium Schottky Interface through Sulfur Passivation that has not implantation that of by chemical treatment. In fact, in gallium arsenide also the pinning depinning has been illustrated by using the sulfur passivation. So, when I discuss about the germanium we will discuss that in some more details of course, we can go through some one paper for Schottky barrier this book also we can see.

And we will this paper which has come at 2010 you can see. So, with that we will conclude our discussion on Schottky source drain contacts. We will take on germanium go to new materials with classical and non classical structures; we will discuss in next lecture onwards.