Nanoelectronics: Devices and Materials

Prof. K. N. Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture - 24

Rectifying and Ohmic contacts and challenges in MS unction source drain MOSFET Technology

We continue our discussion on Metal Semiconductor Contacts and Metal Source Drain Junction MOSFET.

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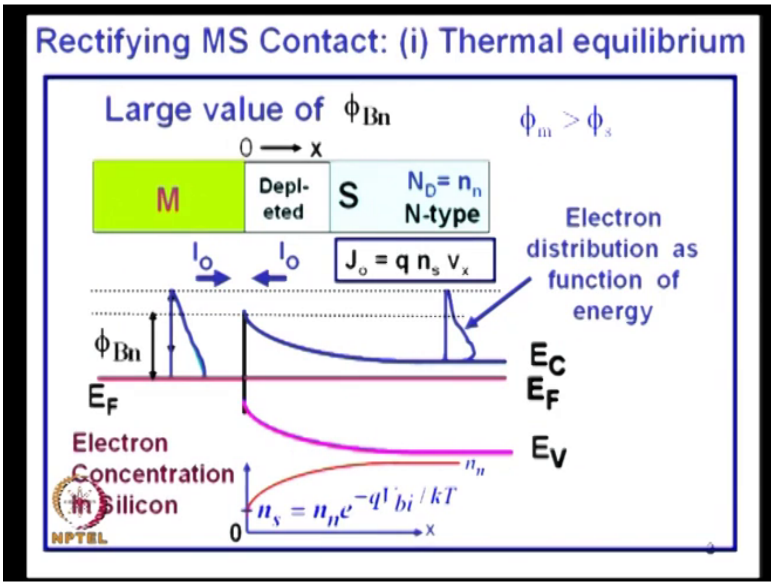

Rectifying MS Contact: (i) Thermal equilibrium

Large value of ϕ_{Bn}

$\phi_m > \phi_s$

$J_o = q\, n_s\, v_x$

Electron distribution as function of energy

Electron Concentration in Silicon

$n_s = n_n e^{-qV_{bi}/kT}$

Last time we discussed the principle of operation of a metal semiconductor contact. We took a case where the work function of metal is greater than the work function of semiconductor. So, this is the situation under the thermal equilibrium and there is a depletion layer in the semiconductor and a negative charge here plus charge in the depletion layer. So, this is because of because electrons are transferred from the semiconductor to the metal because the phi M for a function of the semiconductor is larger.

So, Fermi level there level there is usually below the Fermi level of semiconductor. So, electrons get transferred from semiconductor to the metal. So, we get this is the distribution of carriers this is the barrier phi B n the electrons which have energy above this barrier can cross there giving raise to current I 0 now thermal equilibrium there is no current.

So, the electrons on this side which are above the barrier here the barrier is v b i they are crossing with here. So, they go to cancel each other and we have shown that that current I 0 or current density J 0 is given by this term.

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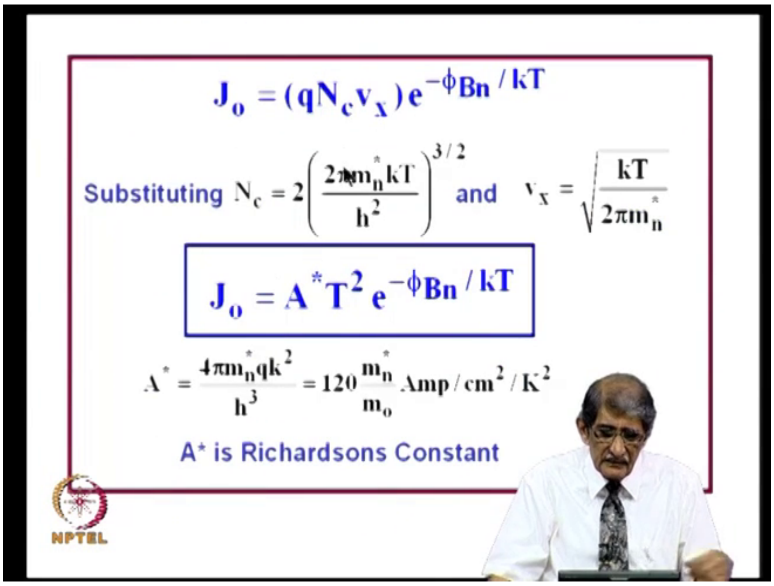

$$J_0 = (qN_c v_x) e^{-\phi Bn / kT}$$

Substituting $N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2}$ and $v_x = \sqrt{\frac{kT}{2\pi m_n^*}}$

$$\boxed{J_0 = A^* T^2 e^{-\phi Bn / kT}}$$

$$A^* = \frac{4\pi m_n^* q k^2}{h^3} = 120 \frac{m_n^*}{m_0} \text{Amp/cm}^2/\text{K}^2$$

A* is Richardsons Constant

Which finally, is a star a star equal to Richardson’s constant which depends upon the effective mass of electron with respect to the pre mass 120 m n that you 120 m n star by m m 0 T squared main component area dependence on temp on the of the current depends upon the barrier height. If barrier is more this is less term e to the power minus phi B n by k T if the barrier is low this is large current now thermal equilibrium you saw that they are equal number of carriers crossing each other and that is canceling as J 0.

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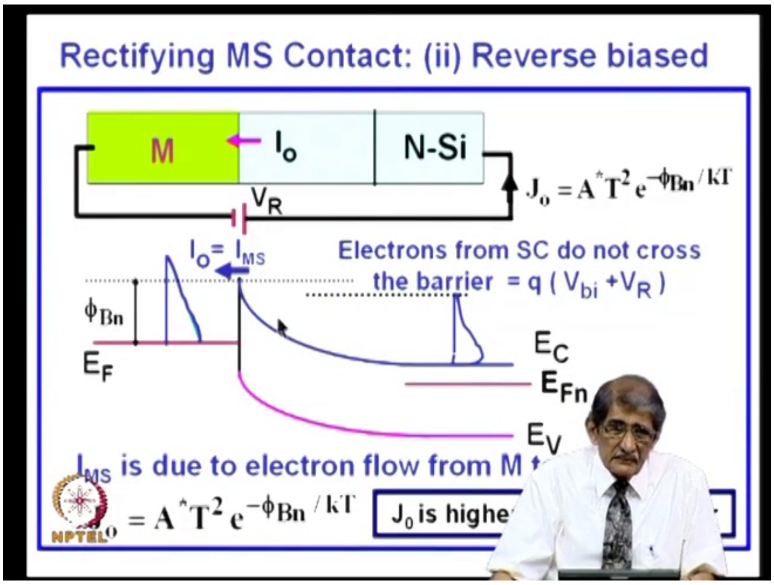

Rectifying MS Contact: (ii) Reverse biased

Electrons from SC do not cross the barrier $= q(V_{bi} + V_R)$

$J_o = A^* T^2 e^{-\phi_{Bn}/kT}$

I_{MS} is due to electron flow from M t

$J_o = A^* T^2 e^{-\phi_{Bn}/kT}$

J_0 is highe

We also saw the forward bias condition I am sorry reverse biased condition where you make this plus now notice the entire voltage appears across the depletion layer.

So, the barrier height which was v b i on this side as increased by v b i plus V R. So, the potential energy of this conduction band here brought down by an amounting equal to V R. So, the energy distribution because the electrons do not have kinetic energy here so you have reduce the potential energy, kinetic energy is up to that particular distance is fixed by the temperature. So, these electrons find a much bigger barrier much more than bottom of there in thermal equilibrium therefore, these electrons from semiconductor are not able to cross to the metal. Now on this is a very very important point you must note on the metals side the barrier height does not change this is the difference between the p n junction and the metal semiconductor contact in the p n junction the total barrier height changes potentially variation takes place both on the N side.

And the p side there is no drop in the metal in the case of there is no voltage drop in the metal in the Schottky barrier contact metal semiconductor contact since there is no voltage drop the potential layer is changed barrier height is same thing that is the important thing. So, whenever you apply voltage to a metal semiconductor contact if I make the semiconductor plus the barrier height on the semiconductor will increase preventing the injection of electrons from the semiconductor to the metal.

So, whatever you get a current, current direction is from plus to minus like that I 0 that is due to these electrons which are having energy above the barrier on the metal side. So, these electrons still can cross please do not get confused when arrow the arrows for the direction of electrons a direction of current electrons flow is from here to here by convention.

You know that negative charge if it moves in x direction current flow is in a minus x direction if plus charge moves from the minus to plus current directions also same thing. So, I M S the symbol is current is I due to transfer of electrons from metal to semiconductor that is a notation. So, this has not changed because this barrier height does not change distribution are not changed.

So, I 0 remain the same thin. So, you get a current whatever you got I 0 there previously whatever I 0 was coming due to this transfer of electrons from the metal to semiconductor was getting balanced by the current injection from the electron injection from the semiconductor to the metal, but since that is removed there is only current component due to the transfer of electrons from the metal to semiconductor that is I M is going in that direction and that we have estimated how much it is a star T square E to power minus phi B n by k T.

So, this you can say it is like a p n junction almost the magnitude of current will be different decided by the barrier height phi b n in this case. So, the in the p n junction reverse bias means n side positive with respect to p side, metal n type semiconductor same notation if metal semiconductor is might plus the current flow is from is less and that is the reverse saturation of current. Now let us see what happens if we followed by of that, but please remember whatever bias I applied to this metal semiconductor contact this barrier phi B n is not going to change. So, the electrons injected from the metal to semiconductor totally decided by how much is the barrier height barrier is. So, how much if the barrier is very low almost all of them will be available over current flow if the barrier is high very little be a current flow in this case now forward bias again remember this would not change.

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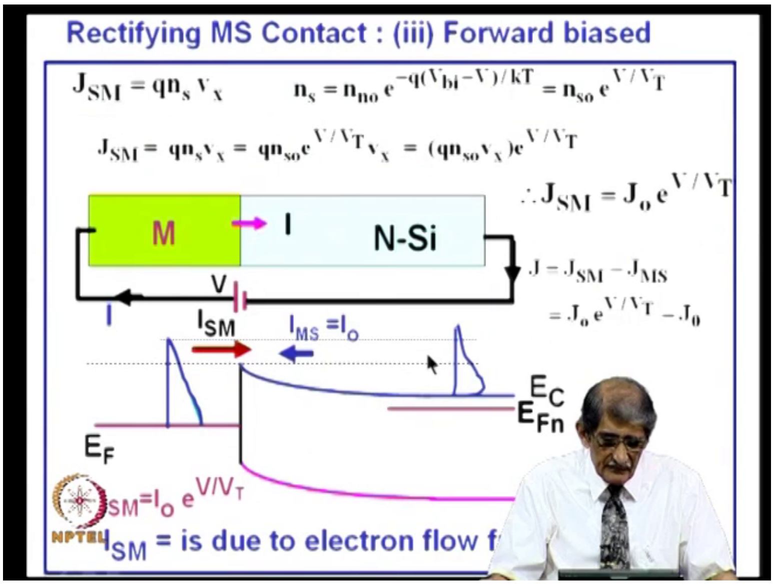

Rectifying MS Contact : (iii) Forward biased

$J_{SM} = qn_s v_x \qquad n_s = n_{no} e^{-q(V_{bi}-V)/kT} = n_{so} e^{V/V_T}$

$J_{SM} = qn_s v_x = qn_{so} e^{V/V_T} v_x = (qn_{so} v_x) e^{V/V_T}$

$\therefore J_{SM} = J_o e^{V/V_T}$

$J = J_{SM} - J_{MS}$

$= J_o e^{V/V_T} - J_0$

$I_{SM} = I_o e^{V/V_T}$

I_{SM} = is due to electron flow f

If a forward bias thermal equilibrium this Fermi level was in the same level see in the previous case the Fermi level has come down path Fermi level because entire energy levels have come down, but here from the thermal equilibrium we have made this plus on the metal side this is minus. So, the penitential barrier across this which was plus minus because of the plus minus on the object side that has reduced by V V applied, now what happens earlier this distribution are just coming up to this end. Now because of the forward bias the potential energy are the conduction band edge are gone up. So, this situation will be the same thin. So, some of the electrons which are above this particular line dotted line see dotted line above this barrier can go from left to right electrons.

Whatever electrons are there from the dotted line up to the peak they can cross from the right so that there are more electrons now crossing from semiconductor to the metal. Now how will this be current vary this current varies as J S M current due to the transfer of electrons from semiconductor to the metal.

Actual direction is from current flow direction is from metal to semiconductor electrons flow is from semiconductor to the metal that is why the S M is given like that. That is number of electrons on surface into velocity velocity thermal velocity root k T by some number that we have seen already. So, early N S number of electrons actually will be whatever carrier concentration here is there into E to the power of the potential difference n n 0 is the carrier concentration here where neutral region into e to the power of minus q barrier originally it is V b i now it is V b i minus V because of forward bias by k t.

So, what is n n 0 e to power of minus V b i that was electron concentration which was present and thermal equilibrium situation at this point? Now that is raised by the amount equal to e to the power V by 2 V by V T. So, what you have to remember is whatever thermal equilibrium carrier concentration are there here it has raised by e to the power of V by V T. So, current has gone up whatever thermal equilibrium J 0 was there has gone up by an amount to e to power V by V T. So, what you have got is this current due to transfer electrons from the semiconductor electrons transferring from the semiconductor to the metal that is I M S that remains the same thin.

But I M S that is current due to the transfer of electrons from the semiconductor to the metal transfer is like that current flow in that direction that has gone up exponentially how much is the gone up depends upon how much is the voltage. So, what you say may imply is this current is J 0 e to power of V by V T like in the case of forward bias p n junction diode whatever J 0 is there it may be e to power V by V T and this current is due to that that is present that is in opposite direction. So, total current is from the metal to the semiconductor. In fact, the plus side it comes like this battery is driving the current that is J S M current density is J S M minus J M S J S M J 0 e to power of V by V T and current due to transfer of electrons from the metal to semiconductor is J 0 itself you subtract that. So, the current is J 0 into e to power of V by V T minus 1.

This is what I have written here like exactly like a the case of diode there is no difference the only thing is the J 0 term in this case will be different from the J 0 term in the diode case we will see what it is. Once again remember this barrier height does not change because of forward bias because of forward bias the current flow has increased, because of increasing the electron injection from the semiconductor to the metal. In the case of p n junction the current increases, because of whole injection from p to n and electron injection from n to p, but in this case whatever electron (Refer Time: 11:28) injected remains the same thing that is this quantity remains the same thin J 0.

So, it is the this component which is actually gone up due to increasing the electron injection from semiconductor to the metal in the reverse bias direction only that J 0 is there Which is due to the injection of electrons from the metal to the semiconductor there is nothing difference in semiconductor injected. Please note if I have to have electron injection from the metal to semiconductor, whatever electrons are there above this barrier are cannot be inject if I want to increase that electron current injected this is important for MOSFET action in the MOSFET n channel you have n plus source which inject electrons.

Here you have metal if it has to inject electrons to the channel n channel this barrier must be small because only those electrons which are above the barrier can get injected whatever is here is going in the opposite direction let us see that. Now if it is a reverse bias if the potential you reduce here this cannot inject electrons back, this is the theme of a basic ground for the MOSFET, now just see the I V characteristics J 0 depends upon J 0 depends upon a star T square e to power minus phi B n by k T.

These are constant for a given temperature it depends upon phi B n.

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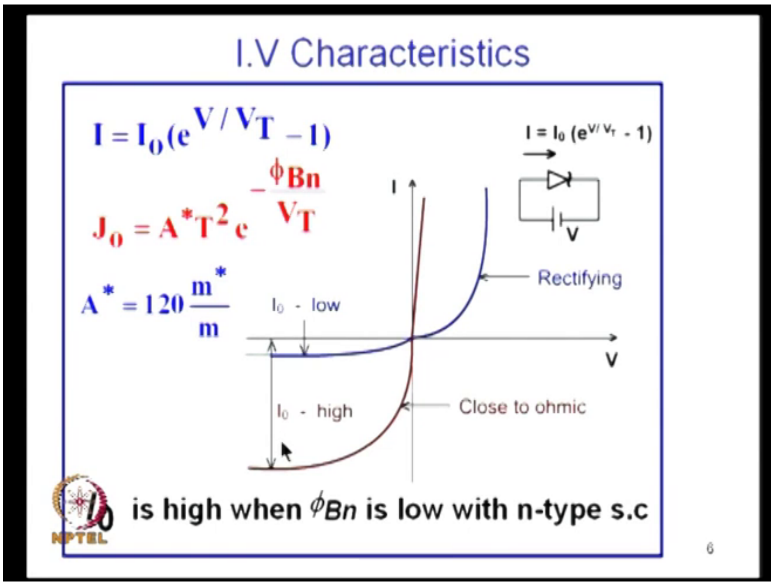

I.V Characteristics

$$I = I_0(e^{V/V_T} - 1)$$

$$J_0 = A^*T^2 e^{-\frac{\phi_{Bn}}{V_T}}$$

$$A^* = 120\frac{m^*}{m}$$

I_0 is high when ϕ_{Bn} is low with n-type s.c

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So, I V characteristics it is a rectifying diode J 0 is small if the barrier height is large number of electrons which are having energy above that barrier is small. So, high barrier height which you get when the phi M is larger than phi of S for n type semiconductor you get a rectifying you get I is equal I 0 e to power V by V by V T and I 0 will be low will be low because I B n is large that is the J 0. And the current is exponentially increasing now with the barrier height is low the reverse saturation current is large I 0 is large if I 0 is large I 0 into that quantity is large. So, this will be a characteristic of this diode with a smaller barrier height.

So, if a larger barrier rate is there you get good rectifying junction very large barrier height you can get the current reverse current close to 0 or Nano power to Pico high barrier height there will be large current in the forward direction exponentially increasing, reverse bias current will saturated PSI 0 a large value of PSI 0 I 0 is high when phi B n is low which with one that you may be looking for in a MOSFET action, because I 0 in the reverse bias condition is due to injection of electrons from the metal to the semi semiconductor.

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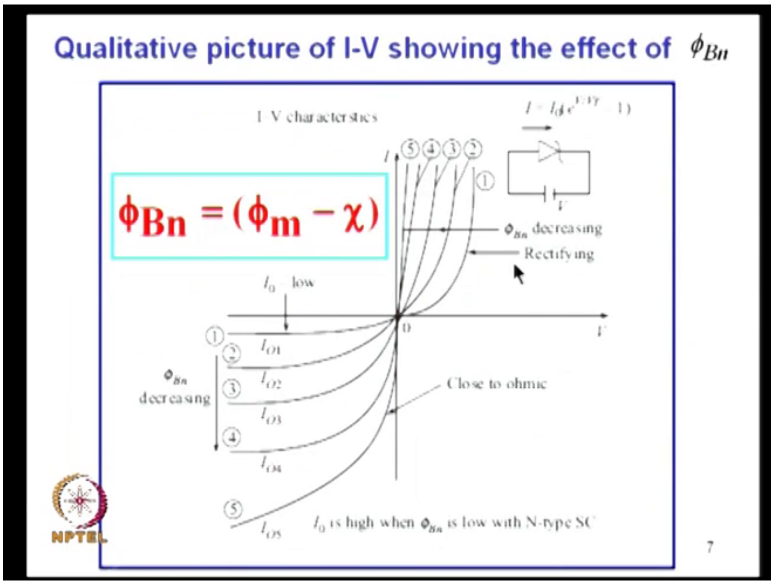

Qualitative picture of I-V showing the effect of ϕ_{Bn}

$\phi_{Bn} = (\phi_m - \chi)$

Now, let us have a more detailed graph there are number of graphs I have plotted here large phi B n I 0 is low as increase of phi B n reduce of phi B n reverse current keeps on increasing the reverse bias this keeps on increasing on the positive side.

Even the smaller way you applied voltage give large current smaller phi B n the current is like that. In fact, the same graph I shown number of them keep on you reducing phi B n you had more and more current and you see ultimately when phi B n is very low, if you look at the characteristic at this source end that is almost linear there, that is voltage drop is very little you can have large current flow that is flows to a ohmic contact. So, phi B n very small indicates that that you get a ohmic contact, phi B n large gives you rectifying contact. Now what you have said is phi B n is phi M minus chi so if phi M higher you must get lower barrier height more closer to rectifying ideal rectifying characteristic.

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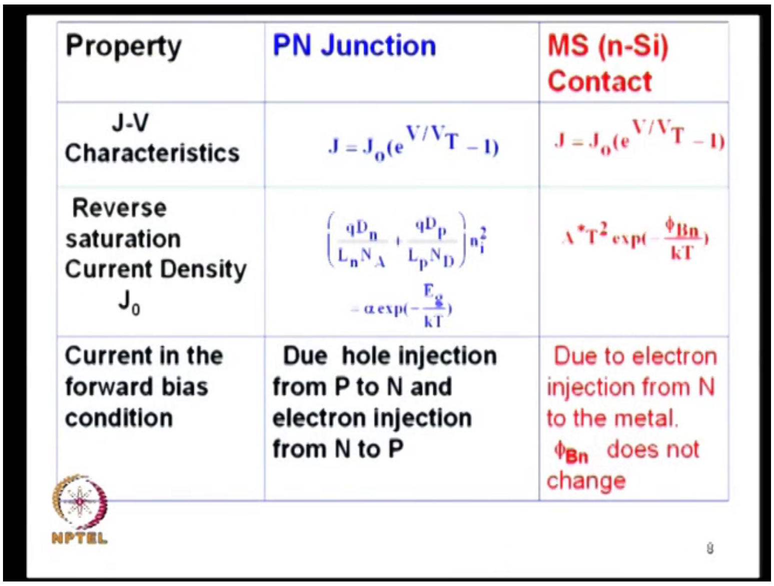

Property	PN Junction	MS (n-Si) Contact
J-V Characteristics	$J = J_0(e^{V/V_T} - 1)$	$J = J_0(e^{V/V_T} - 1)$
Reverse saturation Current Density J_0	$\left(\frac{qD_n}{L_nN_A} + \frac{qD_p}{L_pN_D}\right)n_i^2$ $= \alpha \exp(-\frac{E_g}{kT})$	$A^*T^2 \exp(-\frac{\phi_{Bn}}{kT})$
Current in the forward bias condition	Due hole injection from P to N and electron injection from N to P	Due to electron injection from N to the metal. ϕ_{Bn} does not change

Now, let us see the next slide comparison between the P n junction and the metal semiconductor contact, this is the very good comparison property I V characteristic if you take go through them you have the same type of same type of expression. J equal to J 0 e to power V by V T minus 1 J equal to J 0 e to power V by V T, but what is the difference in the characteristic J 0 in this case is a star Richardson's constant is 120 into M n start m 0 in silicon almost equal to 1 T 120 gallium arsenide about 8 T squared into exponential this quantity now in the case of semiconductor it is proportional to n I squared. So, I have got a constant which decided by the doping etcetera, but the exponential term n I squared is e to the power of minus E g by k T.

Now, let us see the mean contribute up to the reverse current is this exponential term saturation current. In the case of P n junction it is exponential e to the power of minus E g by k T and for silicon E g is 1.1 electron volts for gallium arsenide it is 1.43 electron volts. So, you can immediately say that the J 0 is between the silicon and gallium arsenide junction gallium arsenide junction will have much lower much lower J 0, because E g is larger there between metal semiconductor contact. And this P n junction if you take silicon E g is 1.1 and barrier height will be just go back and see thermal equilibrium if you see the barrier height phi B n is much smaller than the band gap phi B n is this much band gap is you can see from here to here.

So, even if this Fermi level comes down here it will come closer and closer to E g but always less than E g. So, if you go to this particular expression where we have comparison this is 1.1 electron volts this means something 0.6 0.7 electron volts. So, this will be this particular quantity will be larger compare to that e to the power of minus 1.1 by k T e to power of minus 0.7 by k T, this will be larger. So, always the reverse saturation current in the metal semiconductor contact will be higher than that in the case of P N junction.

Now current in forward bias condition in the case of P N junction current in a forward bias diode is due to injection of holes on the P type and N type injection of electron from the N type to P type the barrier height for both holes and electrons will be reduced in the case of P N junction in the case of metal semiconductor contact the current flow in the forward direction it is dominated by injection of electron from the N side region to the metal.

So, phi B n does not change. So, the electron injection from the metal to semiconductor does not change it corresponds to the J 0 term.

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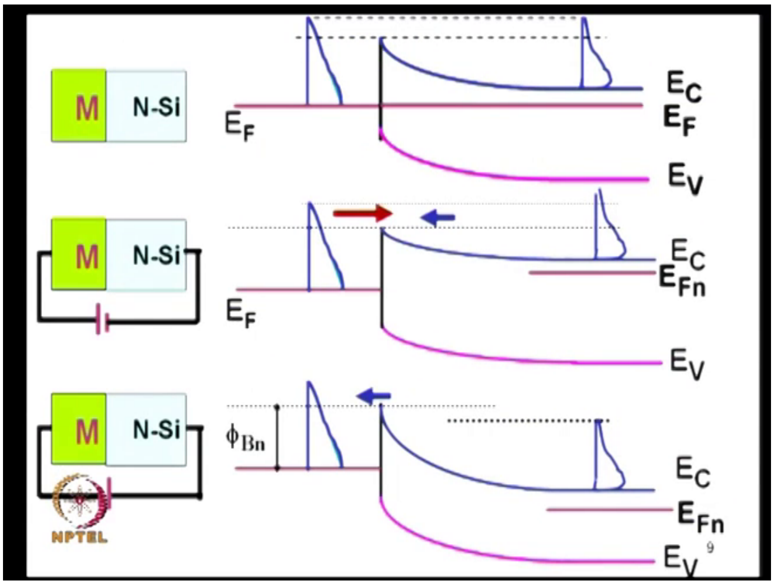

Now, if you want to see the different this is I think that I can you see it in one short metal N type semiconductor thermal equilibrium is like that forward bias more electrons are injected form semiconductor to the metal whereas, the electrons injected from the metal to semiconductor do not change that this arrow told that smaller arrow. And when you go to reverse direction bias you make n region plus nothing no electrons will getting injected from the semiconductor to metal, because they do not have the energy to go above the barrier all that you have current is due to injection of electrons from this metal to semiconductor that is J 0 itself so J 0 J 0 e to power V by V T no current.

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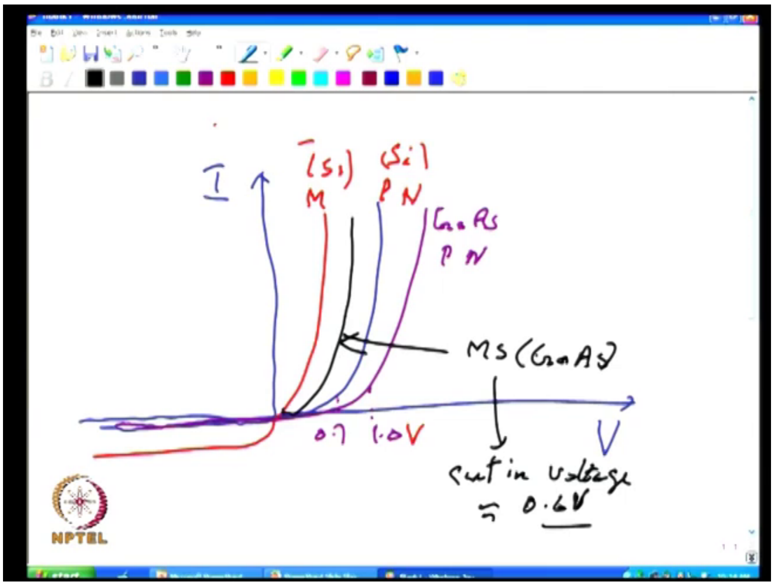

Now, before you go further into this I just want to show how the currents in various devices will be if I draw the voltage versus current if I compare P N junction silicon with p n junction will be the metal semiconductor junction rectifying P N junction with silicon will be going like this exponential reverse very little very little go into 0 and in the case of metal semiconductor contact what will happen barrier is low. So, current is more reverse current is more I am sorry reverse current will be more passing through that it will go like that and it will go like this 1 could not same scale forward and reverse this is the metal this is a P N junction. Suppose P N junction silicon this is silicon this is metal silicon suppose I take gallium arsenide the gallium arsenide P N junction.

That will be like this the E G is larger therefore, reverse saturation current will be even smaller that is the gallium arsenide P N junction. So, if I make a P N junction in gallium arsenide will have a more cutin voltage; cutin voltage of almost about you know silicon it may be about point 7 volts gallium arsenide it may be close to about 1 volt 1 electron volt 1 1 volt. So, you will have that is voltage. So, there is in gallium arsenide, now if I make a metal semiconductor contact in gallium arsenide that will be somewhere higher than this because you can get higher barrier height in that compare to the silicon.

So, that will be M S contact with gallium arsenide. So, in the gallium arsenide you can make metal semiconductor contacts much more effectively than in silicon, if you want to make the effect they use metal semiconductor contact in gallium arsenide.

Because we can get cut in voltage something like in this case V gamma cut in voltage or that case will be something like about 0.6 volts close to that of cutin voltage of silicon P N junction this one this is a gallium arsenide metal semiconductor contact that is because in V GS are you get a barrier height which are higher than what you get in the case of silicon. So, that is the idea that you can think of now let us get back to this.

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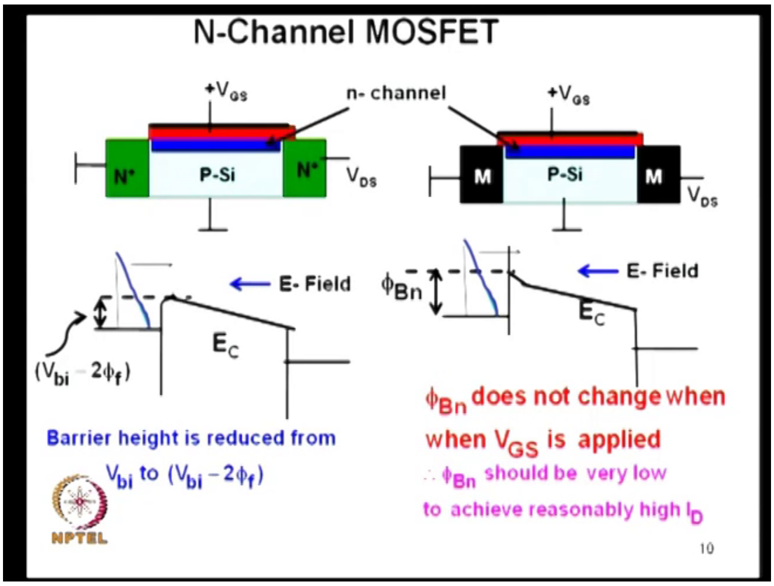

N-Channel MOSFET

Barrier height is reduced from V_{bi} to $(V_{bi} - 2\phi_f)$

ϕ_{Bn} does not change when when V_{GS} is applied

$\therefore$ ϕ_{Bn} should be very low to achieve reasonably high I_D

So, having said that if you want inject electrons into n-channel, you must have smaller barrier height that will go into that n channel MOSFET if you want to make. In that case of N N channel which schematic diagram, in the case of conventional MOSFET this is the channel, blue is the channel, red is the oxide above that I have the metal.

And P types of state I am talking of silicon junction, silicon MOSFET, N plus source, N plus drain, N channel when I apply plus voltage I can invert it. Now when I apply plus voltage to the gate there is a depletion layer below this and this potential is at plus 2 phi f, when it is inverted surface potential is plus phi f; that means, between that ground and this channel beginning there is plus 2 phi f this junction is forward biased; that means, the barrier whatever barrier was there originally I am just showing still as vertical, but it will go that barrier will be whatever built in potential is there minus 2 phi f. So, originally the barrier was built in potential when if there is no inversion if there is no voltage appear ranged between the source and the channel barrier height between the channel.

And the source built in potential now because there is a plus 2 phi f voltage here because of gate voltage at the channel the potential difference there is V b i minus 2 phi by f forward bias diode as, I was mentioning earlier when you invert the channel the source is getting source junction is getting forward bias by 2 phi f. So, barrier height is V b i minus 2 phi f; that means, the whole electrons can easily get injected across that I am just showing still that distribution per electrons from the Fermi level up to that like that in the n type region. So, you can see lot of electron get injected here if I increase the 2 phi f quite a bit of electrons can injected to channel, now from here to here when I apply a drain voltage V D G S V D S whether there is depletion layer at the drain layer or not there is a drop or there is from this source end to the gate end.

There is a voltage rise there is a gate end is that plus voltage with respect to source end; that means, if I draw the energy band diagram that will be going down like this plus is that lower end compare to minus, betweens this is plus this is minus I put it as lower electron lower energy in electrons because plus and minus here electrons can be easily go from in the minus to plus (Refer Time: 27:37) attracted to plus. So, that is another way of looking at that. So, whatever electrons are injected here go down into the along the channel the drift electric field from minus to plus and they collected, how much current flowing is there here depends upon, how much charge is present here because of the gate voltage also how much is the barrier height here, the barrier height is reduced by 2 phi f that is a quite a large reduction the barrier height.

So, entire current is controlled by the gate gate voltage more gate voltage more charge and whatever is collected here can be supplied from this source end because there is a reduced barrier height is there, now let us take a look at the metal semiconductor contact on the right hand side it is very interesting to compare this. This is what makes makes it difficult for the technologist to realize, metal source, metal source, drain metal source metals drain junctions, metal contact here. Here as you already have seen whatever I do on between the channel and the gate source, that barrier height whatever was there phi B n is not going to change that going to remains the same thing whatever I apply minus 2 phi f do here.

See in this case the minus phi f for reducing a entire barrier in this case if I do minus 2 phi f that is reduced here only this barrier reduced here on the n side. So, this is reduced plus minus here and that is across this depletion layer there that is a small depletion layer that is whatever 2 phi 2 phi f is appearing across that nothing here so; that means, number of electrons available here are fixed by the barrier height phi B n this distribution is fixed by temperature some of the barrier height is if it is a rectifying contact the barrier height is high.

So, these numbers of electrons available for transporting from the metal to semiconductor are only in this that small region. So, here whatever charges are here this portion same as this there is a voltage drop from here to here because of the current flow. So, the energy band diagram is like this. So, electrons reaching here will flow in the direction get collected by drain there is no issue on that thing because that is hill there it can be collected here. So, now, the point that you would see here is if this is not able to supply.

Whatever charges are inverted here it is getting collected, but the rate at which is the current can flow is ultimately limited by how much you say with this can supply, if the barrier height is let us say almost like they are very high, nothing can collect there is no injection or carriers because of barrier for electrons in the source region is limited by the barrier height I am sorry number of electrons that can cross this barrier depends upon the barrier height, more the barrier height more electrons are available.

So, the moral of the story is if I want more number of electrons available here to be injected I must have this barrier height reduced phi B n must be lower and phi B n is low as you keep on getting lower and lower ultimately what you saw was you get here, by keep on reducing the barrier height if you see this graph here I V characteristics I move along this line ultimately you get ohmic contact.

So, ideally what you would like to have here would be you would like to have this as a ohmic contact or phi B n as low as possible phi B that is a barrier height with respect to the channel not with respect to P region what we are concerned is the barrier height between the metal and the n region which is the inversal region. So, what we are looking for is metal semiconductor contact at the source end which will give phi B n as low as possible.

Now let us see whether you can get that by changing the work function, if you look at the this characteristics here, I just go back to the slides see here here you had taken phi m much larger than the phi of s that is the metal, which has got large work function means the Fermi level is at a much lower level compare to the Fermi level of the semiconductor, phi s small means the work function or the semi conductor is smaller pertain between the between in the vacuum level and the Fermi level in semiconductor the energy difference is less compare to the energy difference between the vacuum level and the Fermi level in the semiconductor.

So, now let us see what happens instead of I want to reduce the barrier height. So, that there is supply is there.

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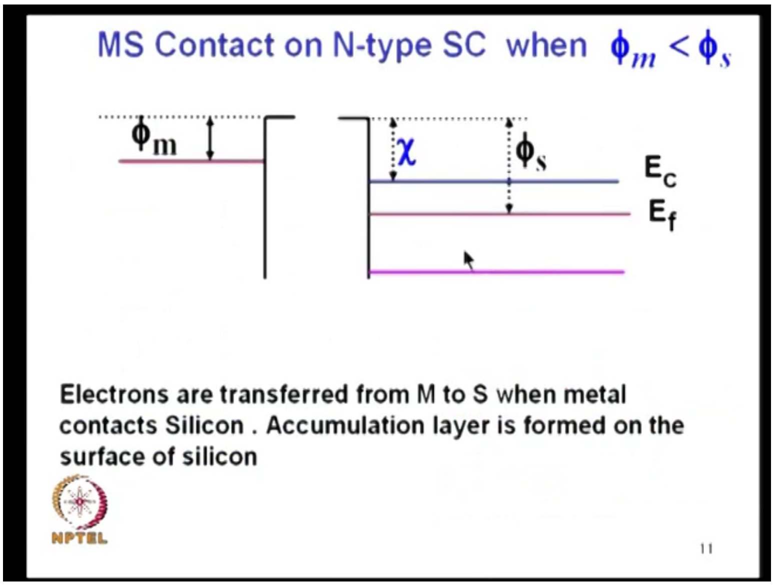

MS Contact on N-type SC when $\phi_m < \phi_s$

Electrons are transferred from M to S when metal contacts Silicon . Accumulation layer is formed on the surface of silicon

What will happen if I get phi m less than phi of s, see if this phi m where large that remain here that would have been here, then the electrons would have got transferred from the semiconductor to the metal depletion layer that give it rectifying. Here phi m is small compare to what is phi m from the vacuum level to the Fermi level that is smaller compare to this difference between the energy of the vacuum level and the Fermi level in semiconductor.

So, when you connect them together in the system what you will have will be electrons will be get transferred to from the metal to this semiconductor till the 2 Fermi levels are equalized.

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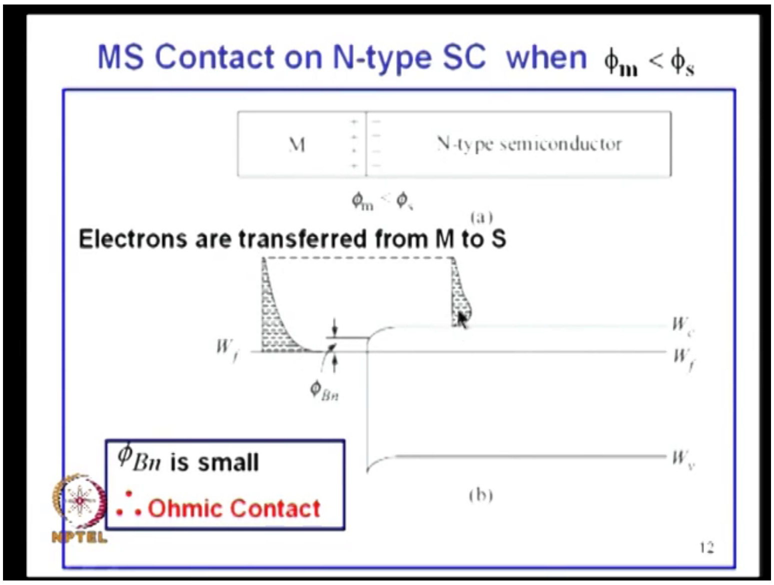

MS Contact on N-type SC when $\phi_m < \phi_s$

Electrons are transferred from M to S

ϕ_{Bn} is small

$\therefore$ Ohmic Contact

So, that is the situation electrons have got transfer from the semiconductor to the metal in metal there are already lot of large number of electrons. So, if you transfer electrons to the semiconductor to the metal there will be an accumulation layer see more number of electrons have got transferred from the metal to semiconductor; there will be a small charge sheet there is no depletion layer if it has to be depleted the electrons have been transferred from semiconductor to a metal, but now because of the higher Fermi level here electrons get transferred from the metal to the semiconductor.

So, this surface gets more negatively charged this surface get more positively charged that is the situation. So, you have got plus charges here and those plus charges you can put it as the electron density these are the plus charges, but electron distribution is like this in the metal electron distribution semiconductor is like this. So, that is in thermal equilibrium there is no barrier here because this is accumulation accumulation means very little band bending you know that accumulation we use to take phi S is equal to 0, but it is not 0 slightly negative here. So, very small barrier if the electron very small bending so barrier height only this much phi B n can be made very very small again determined by the differences between the phi m and chi of s phi of s phi m minus phi f s is negative barrier height is much small only.

So, the electrons here all so many electrons have energy above that here. So, many electrons are there if I apply voltage to this either way if I apply either way voltage where very small movement here. So, there can be large current flow, see in the it is difference between the 2 is pre scale this there was a big barrier here; here there is no barrier for either case very small barrier. So, if I have the plus here or minus here there will be large transfer of electrons from metal to semiconductor or semiconductor to metal. So, this is the way to go.

So, what we are telling is why do you choose metal with the high work function choose a metal with lower function for example, if I take aluminum work function is 4.0 5 and phi of s in semiconductor is 4.0 5 practically no barrier. So, you can be very happy if everything is fine you will say that you can have ohmic contact if I have aluminum on to the surface of the n type semiconductor or as a source of the n channel MOSFET.

So, now let us see if I have p type substrate because after all if you take N-types substrate you get when invert you get p type substrate if I take P-type substrate you get this type of n channel.

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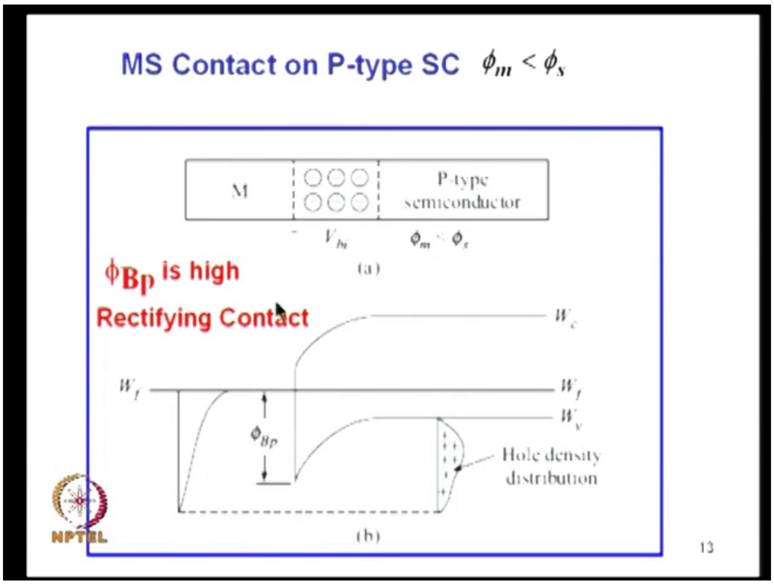

MS Contact on P-type SC $\phi_m < \phi_s$

ϕ_{Bp} is high

Rectifying Contact

Now, let us see what about the P-type substrate. In fact, whatever we have discussed I am not getting down to this suppose using the phi m is less than that of phi of s like in this case. In the P-type if we have P-type what would happen Fermi level will be even below phi m is less than phi of S electrons will get transferred from this semiconductor metal to the semiconductor. If it is a P type thing if electron get transferred from the metal to the semiconductor there will be depletion layer. So, if phi m is less than phi of s you will get a depletion layer here and you that will be rectifying.

So, thing to remember is if you if when you make the contact if there is a depletion layer in the semiconductor, you can change that depletion layer width and the potential barrier in semiconductor you can go you can change the barrier height in semiconductor that rectifying. If I have a phi if there is no depletion layer if has a accumulation layer then that is a ohmic contact. So, exactly by the same argument I am not getting down into that you can in the figure in this case electrons get transferred from this petal to semiconductor introducing depletion layer that will give us a depletion layer.

So, by applying a voltage you can change the barrier height. So, it will be rectifying contact if phi m is greater than the chi of s if phi m is greater than phi of s, in the case of P type material this is will lay down if the transferred transfer from there to there or you will get a you will get just like exactly reverse in a N type semiconductor where phi m is greater than phi of s.

We have got electrons transferred from this the semiconductor to from the metal to semiconductor depleting causing depleting.

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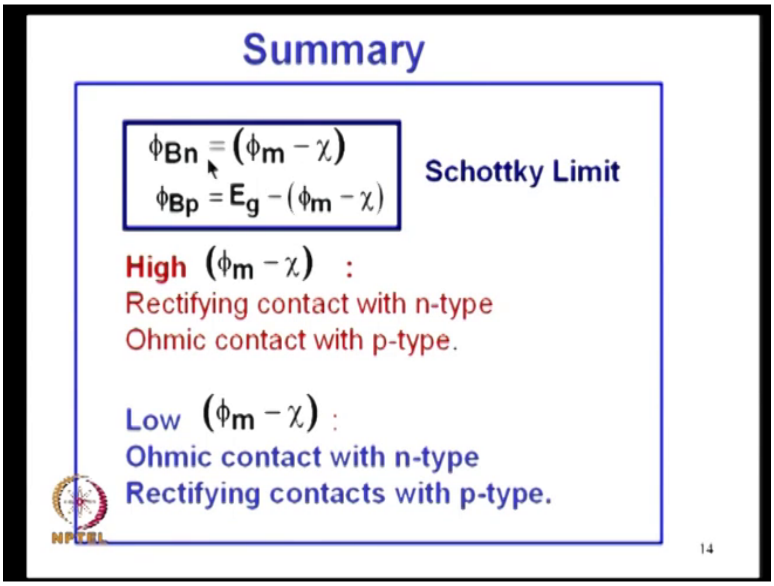

Summary

$\phi_{Bn} = (\phi_m - \chi)$

$\phi_{Bp} = E_g - (\phi_m - \chi)$

Schottky Limit

High $(\phi_m - \chi)$:

Rectifying contact with n-type

Ohmic contact with p-type.

Low $(\phi_m - \chi)$:

Ohmic contact with n-type

Rectifying contacts with p-type.

The object is true in the case of P type semiconductor if the phi m is larger than the phi of s you will have a accumulation layer in the case of P type semiconductor, with this sum up with summary of this discussion phi B n is phi m minus chi that is ideal and if phi m is high phi m minus chi is high. So, rectifying contact in N type semiconductor what is phi B p I do not know whether I pointed it be let me go back to that and show you this is phi B p if we take a look at this from if there is a hole here that is a electrons is absent there, to take the hole above this to the other side that has to cross this barrier height. So, the important thing to understand is if an electron is at this end to take it here you have to spend energy.

So, a hole at the near the Fermi level if you are talking about taking to the above this point up to this point is equivalent of taking electrons from this point to that time; that means, to take an electron from here to here you have you have to spend energy, that is higher energy for electrons. Same thing if I have to take hole from here that is Fermi level to this edge of the gap barrier height you have to spend energy. So, this is barrier for holes and here barrier for electron is that. So, when you go back to other diagrams here this is the barrier for the electrons and that is the E G band gap, band gap minus phi

B n band gap minus phi B n that is phi B n is that totally this band gap that minus phi B n is phi B p.

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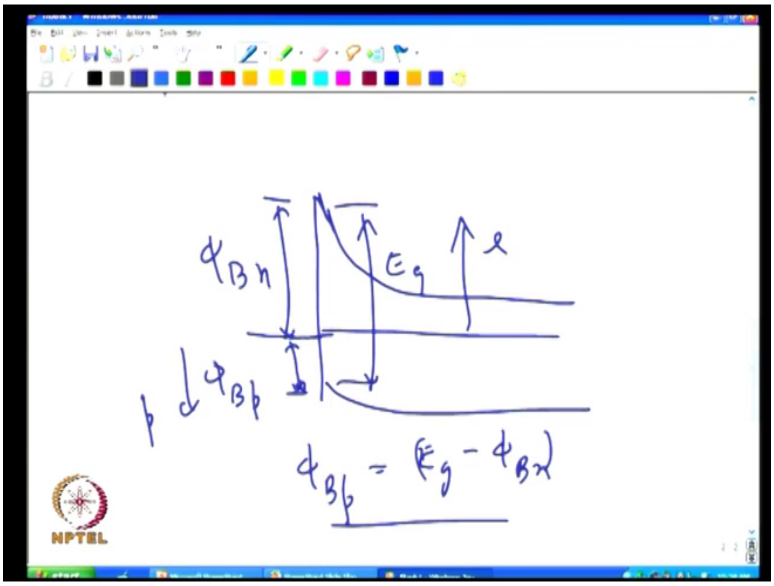

So, that is if you do not get it see if I have the energy band diagram like this like that is adjust the energy band diagram is like that let us say that is N type.

Now, that is a barrier height that is a barrier height for electrons and this is phi B p barrier height for holes, because it difficult it is difficult to take if you have to spend energy for plus charges that is the higher energy for electron that is higher energy this is higher energy for holes. So, this is the phi B p and phi B p you can see is the band gap, E g phi B p express in electron volts minus phi B n. So, you can see that if phi B n is high phi B p is always low, if some process gives you higher phi B phi B n that gives you lower phi B p this is something which you must remember. Now let me go further down. So, phi B n if phi m is larger than chi phi B n is high at the same time you can see phi m is larger than chi phi B p is low because phi B n is high phi B p is low.

So, you get phi m is larger than chi phi of s or chi, you get rectifying contact with the n type material our n channel, but then for the same for functional difference phi B p because if phi m n is large this is large E g minus that large quantity will be small phi B p will be small that will be ohmic contact in the p type substrate. So, if you get very easy to remember if you get rectifying contact with the p type material n type material or n channel device you will get ohmic contact in the p type material or p channel. So, low phi m phi m minus chi low value of phi m minus chi with low phi B n that gives ohmic contact on n type material rectifying contact on p type. So, now, what will say? So, if I want to make a this ideal theory tells us that I would chose a metal with a lower work function to make ohmic contact with the n channel because that can inject lot of carriers if I have a p channel I will make a high work function material here that is ideal.

Now, whole thing is under assumption that phi b n is phi m minus chi that was the most idea case.

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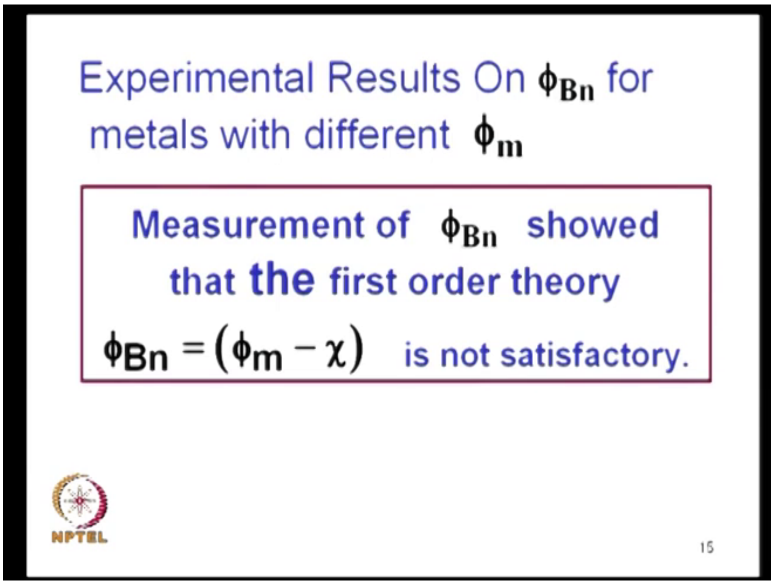

Experimental Results On ϕ_{Bn} for metals with different ϕ_m

Measurement of ϕ_{Bn} showed that **the** first order theory $\phi_{Bn} = (\phi_m - \chi)$ is not satisfactory.

Now, let us get down to our requirement experimental result from phi B n for metals with different phi m, you can see this slide you can see that measurements on phi B n there is a some ways of measuring by the I V characteristic etcetera or C V you I phi B n showed that, the first order theory whatever we have mentioned is not correct phi B n equal to phi m minus chi is not been satisfactory.

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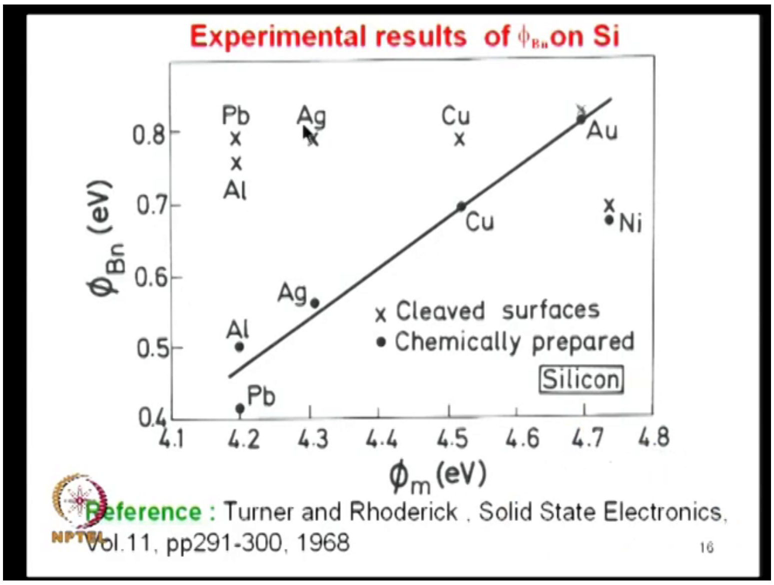

Experimental results of ϕ_{Bn} on Si

Reference : Turner and Rhoderick , Solid State Electronics, Vol.11, pp291-300, 1968

That is the phi B n all this dots are measurements they crosses are the measured phi B n by making the measurements on metal semiconductor contact either C V or i V it will give you that you can extract that.

So, what they did was they had silicon which was freshly cleaved you can just cleave silicon material you can just apply some pressure it will cleave along a particular plane and freshly cleaved means what if I have the thing, which is cleaved I have got this surface which is free I have the surface of the semiconductor, which has been just cleaved. That means, there are lot of dangling bonds there that will tell you that that surface has lot of surface states it is not ideal; ideal case there are no surface states when I discuss the ideal metal semiconductor ideal metal semiconductor contact theory assumption was that there are no dangling modes there are no surface states, when you have a oxide layer there it is a same surface state which you call at as call it as a interface state. Because it is the same surface state manifest that as the interface state many of the dangling modes are satisfied by the oxide there are still some of them which are not satisfied that is called interface states.

So, freshly cleaved absolutely see this is one the x axis your work function corresponding to aluminum silver copper and gold all this cross x. So, the phi V N is about 0.8 almost about 2 thirds of e g. So, let once you have fix the e g for silicon that was fixed that is freshly cleaved thing, but it gives a clue that there are large dangling mode feature responsible for that the surface states were responsible for this. So, if you are able to remove those when you are in business now what they did was let us see that let us cleave the surface give me chemical treatment for example, if you clean it with h n h c l h 2 o 2 solution and ammonia hydroxide and h 2 o 2 solution, then what you get will be a surface which has a layer of oxide a thin layer of oxide will be there even when you put it in a h n like that r c a one and r c a 2 because of that h 2 o 2 action that will be some amount of oxide.

Now when you very very thin layer may be less than a nano meter few angstroms when nano meter is 10 angstroms couple of angstroms that sufficient it fascinate some of those dangling modes. So, when you do that and put a metal you can see that barrier height has gone down is changed and as increase the work function, you expect a phi m minus chi chi is same for silicon phi m minus chi increases at increase and that increases linearly we are very happy that it is obeys the law phi m minus chi, but the change in the phi B n say from 4.2 you will change it to 4.7 or 4.7 5 around that for gold that let me take 4.2 to 4.7 that is that is about to 0.5, I should have got as per our theory the phi B n should have increased by the same extent that is 0.5 electron volts.

But you see here it is about 0.5 here it has gone up and become 0.8 instead of increasing by 0.5 electron volts it has gone up only 0.3 still not satisfactory the changes with phi m as we are happy that first order theory is, but it does not change as much as phi m. Let us see other materials is it characteristic of silicon alone same thing that we did gallium arsenide gallium arsenide result from cleaved 1 1 0 gallium arsenide cleaved.

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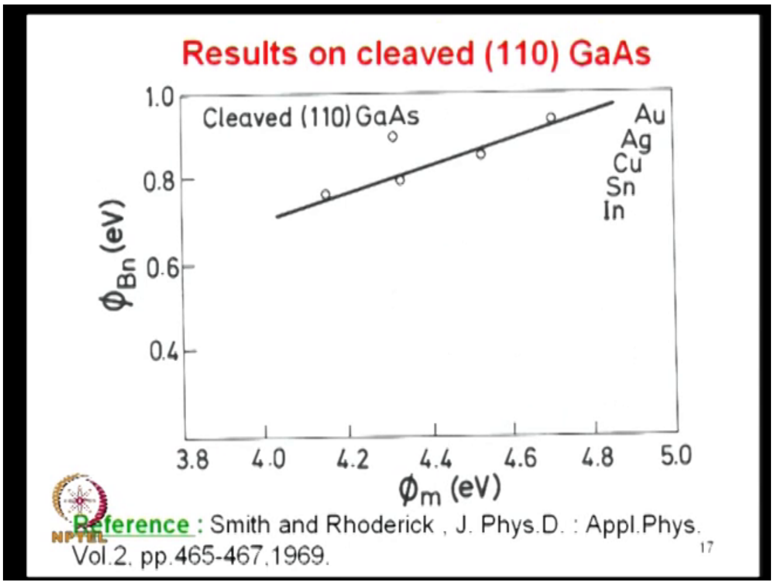

Results on cleaved (110) GaAs

Reference : Smith and Rhoderick , J. Phys.D. : Appl.Phys. Vol.2. pp.465-467.1969.

There are slight different phi m varied from about 4 right up to about 4.8 it changed hardly 0.2 electron volts. So, when it change it by a volt 1 electron volts close to 1 electron volts phi m your phi B n changes hardly about 0.2 electron volts.

But again the indication is there on the dependence of phi B n on phi m, but not as much as you expect.

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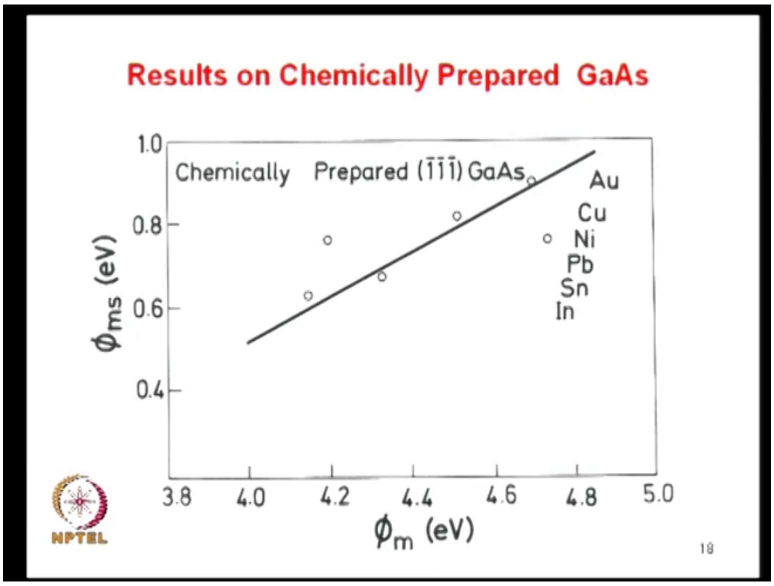

Results on Chemically Prepared GaAs

Chemically prepared thing see here this is just freshly cleaved in the case of silicon it was flat here it is slight different was there may be the surface state number is less in that

1 1 0 plane. Now another surface 1 1 1 1 1 or it is a family there they chemically prepared chemical treatment you give. Then 1 4 to 4.8 when you change it increases from instead of point at electron increasing phi B n it increases something about to 0.3 electron volts. So, still almost a linear variation is there with phi m, but not as much as you expect everything points out that if there are interface state is densities are high.

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The phi B n will become independent of phi m.

But if interface state densities are reduce to some extent by passivation it will become proportional to phi m, but not as much as there is a proportionality constant a factor which is not equal to 1, but less than 1.

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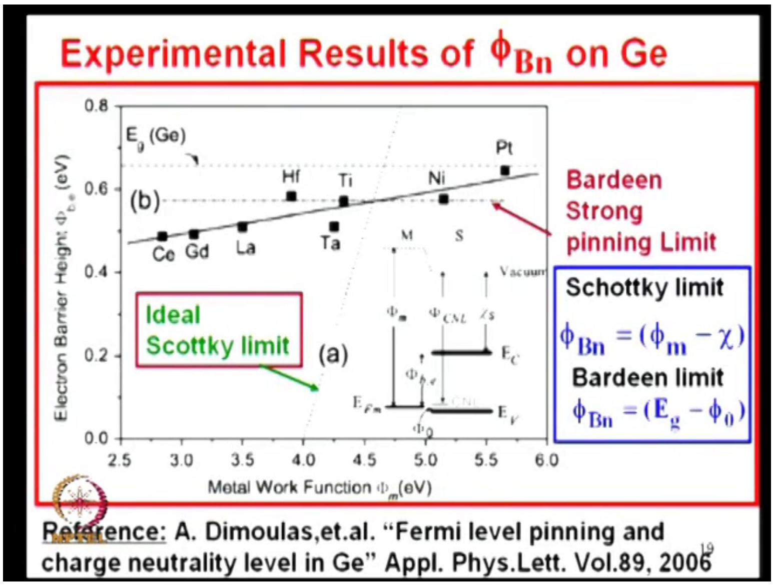

Experimental Results of ϕ_{Bn} on Ge

Ideal Scottky limit

Bardeen Strong pinning Limit

Schottky limit

$\phi_{Bn} = (\phi_m - \chi)$

Bardeen limit

$\phi_{Bn} = (E_g - \phi_0)$

Reference: A. Dimoulas,et.al. “Fermi level pinning and charge neutrality level in Ge” Appl. Phys.Lett. Vol.89, 2006

Now, let us see. So, we have seen silicon we have seen gallium arsenide let us see Germanium; Germanium if you see why we are taking look at germanium is this is a one material which they are trying to use for making the MOSFET with metal semiconductor contact. They are using germanium because of it is much higher electron mobility compare to silicon, much higher hole mobility compare to silicon. If you go to gallium arsenide electron mobility is much higher compare to that of silicon whole mobility is not it is almost that of whole mobility in silicon, but in germanium you will get both of them where factor of 2 3 higher.

So, let us people have made metal semiconductor contacts with germanium vary in the work function from right from about to 2.5 to about 5.5 or more platinum from c c m metal to platinum, you can see there are all over the place this squares are the measured fields if put the thing together it does not follow any rules, but I can draw or at least if it is phi m minus chi this should have been a dependence taken a chi of germanium that falls about 4.0 5 close to that of silicon and if I add phi m, you can see 4 and 4.5 means that should have been somewhere 0.5 electron volt this point 0.5 you are corresponding that 4.5 minus 4.0 5 that is 0.5 would have been in the barrier height you do not get that.

If I take 3 electron volt I must got it somewhere it down here, but you get almost like this. So, just some quick the thing will be get back to this later on to examine that I can draw a straight line like this they needs almost flat compare when I am using hafnium, titanium, nickel, etcetera. It almost flat close to about slightly less than 0.6 electron volts, remember the band gap of germanium is 0.6 6 electron volts. In the case of silicon we had 1.1 electron volts and you had the barrier height flat coming to about 0.8 electron volts that is about 2 thirds of that in the case of germanium band gap is 0.6 electron volts.

So, what you get is slightly less than 0.6 electron volts that is below 0.6 electron volts, but I can draw a flat line this or if I am more optimistic let us it is dependent on phi m I can draw this line leaving out hafnium and nickel and tantalum I can draw these line as straight line and say there is still some phi m dependence. So, this is the phi m here and this we will come back discuss this is the band gap E c minus E v and phi M is there for that case see very high this thing here.

So, this will discuss there is neutral level neutral level is very close to all this band that is a indication of that. So, these 2 this is actually the ideal theory the dotted line that theory was given by Bardeen and Schottky and barrier height was called Schottky barrier what whatever phi B n we are taking of is called as Schottky barrier because of name of Schottky who named it.

So, that is the Schottky limit you would have got phi m minus chi it means Schottky limit and Bardeen said it will be independent of phi m it will be having certain value decided by the neutral level in the Fermi level surface. So, that is the Bardeen Bardeen limit due to strong pinning limit surface pinning Fermi level pinning limit the all that what is there we will be able to discuss later.

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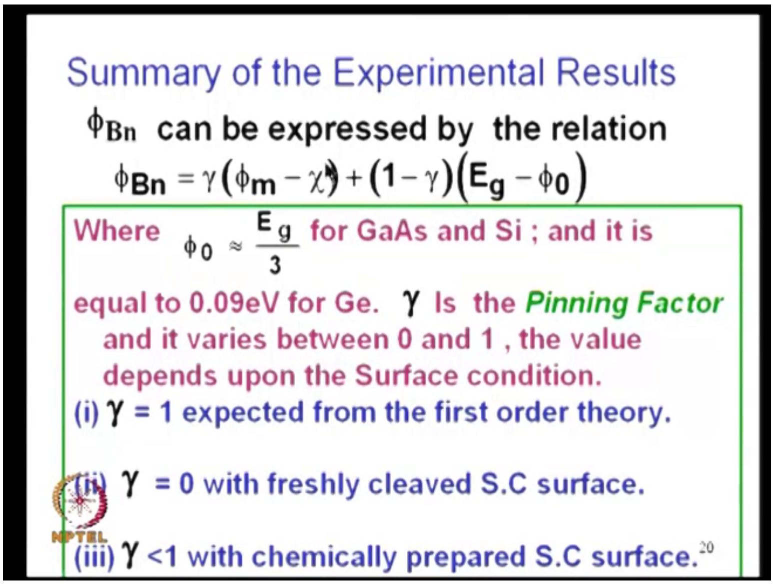

Summary of the Experimental Results

ϕ_{Bn} can be expressed by the relation

$$\phi_{Bn} = \gamma(\phi_m - \chi) + (1-\gamma)(E_g - \phi_0)$$

Where $\phi_0 \approx \frac{E_g}{3}$ for GaAs and Si ; and it is equal to 0.09eV for Ge. γ Is the *Pinning Factor* and it varies between 0 and 1 , the value depends upon the Surface condition.

(i) $\gamma = 1$ expected from the first order theory.

(ii) $\gamma = 0$ with freshly cleaved S.C surface.

(iii) $\gamma < 1$ with chemically prepared S.C surface.

So, from these things one can fit in a graph like this I will just discuss this how this comes up and what are the implications of that more details we will take up in my next presentation. So, what we have concluded from this experimental results is phi B n can be expressed by a relation ideal case it is phi m minus chi, in the practice I can express phi B n as gamma times phi m minus chi plus 1 minus 1 minus gamma times E g minus phi 0 because you saw that depends upon E g minus phi 0.

So, gamma equal to 0 or gamma equal to 1 second term is 0 gamma equal to 1 phi minus chi that is a ideal case first order theory when gamma equal to 0 first term ideal theory is gone and 1 minus gamma equal to 1 E g minus phi naught. So, you can say that in high freshly cleaved surface gamma also equal to 0. Therefore, first term enters and you got a term which is independent of phi m v g minus what is that phi 0 we will see in my next discussion and gamma in between the 2. So, what we said is ideal theory it is phi m minus chi non ideal theory worst case gamma equal to 0 and it is depends it is independent of phi m and you get E g minus phi 0 in between you get gamma is less than 1. So, something point phi times phi m minus gamma point phi times e g minus gamma like that.

So, in summary that is what you are telling you can express it in this fashion the details of all these things how it comes up due to the surface states or interface states. We will just discuss in our next presentation complete details of that how to overcome on that, how to overcome from these problems and how to use it we will see it in the next presentation.