Nanoelectronics: Devices and Materials
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Lecture – 23
Need for MS contact Source/Drain Junction in Nano scale MOSFETs

We start with the new module; module 3 of the Non classical MOSFET series. And this will be on the Metal-semiconductor Contacts and Metal Source Drain Junction MOSFETs; that is instead of p-n junction, we have metal semiconductor junctions as the source and drain.

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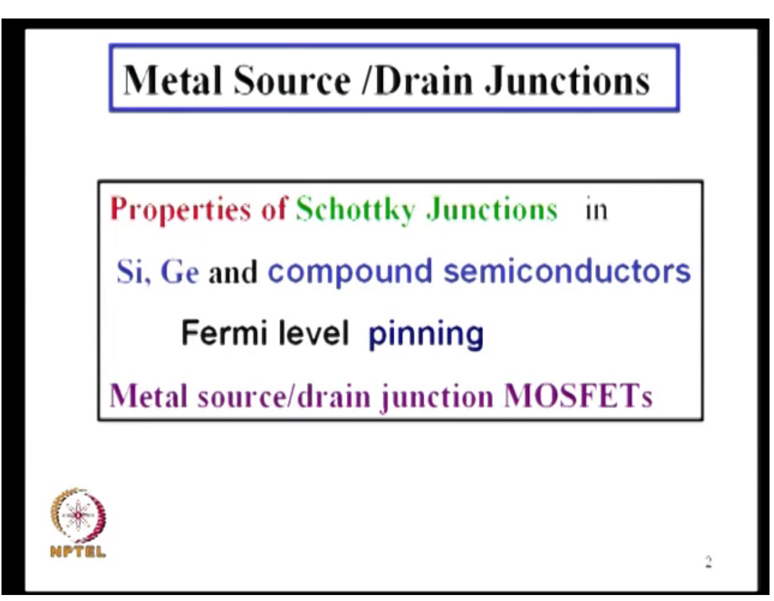

Now, here we will discuss the properties of Schottky Junctions and silicon, germanium as well as in compound semiconductors; how they are different? All of them are similar, but there are slight differences are there. Then Fermi level pinning effect on this Schottky barrier, on the working of this metal semiconductor contacts and then of course, MOSFETs using these; metal source drain junctions.

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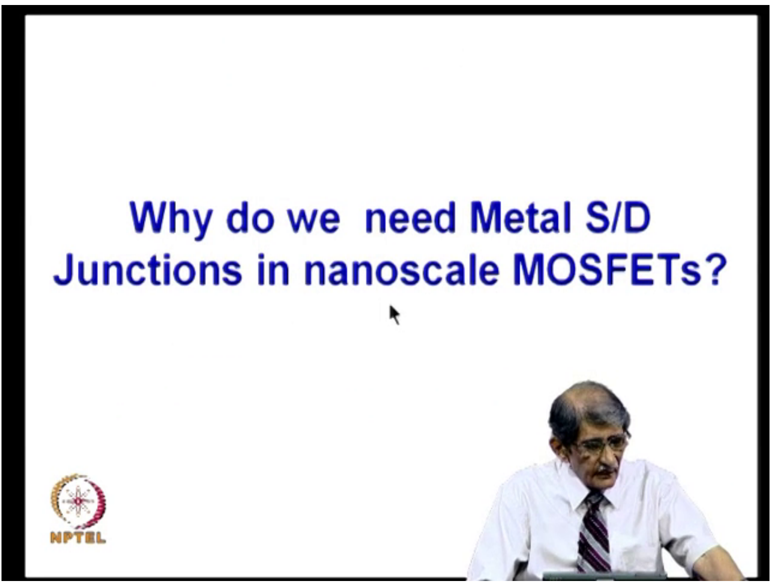

So, the first question what comes to anybody's mind is; why do we need this type of change from the conventional P N junction to metal source drain junctions. Particularly when you go for small scale or nano scale MOSFETs.

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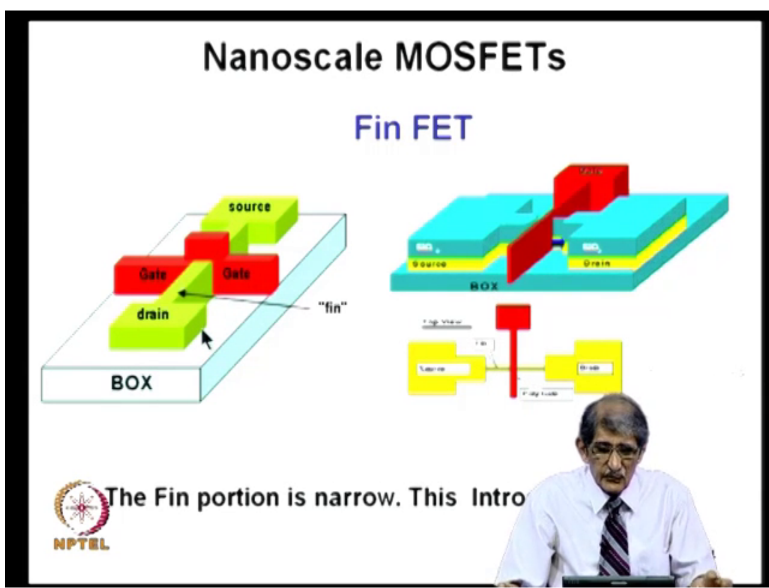

For this purpose, I have put here the Fin FET which we discussed last time. In fact, the idea is this is the diagram which I showed last time. Now, a simplified version or the three dimensional picture of the looking from the other side, you can see it is like this.

Now, you can see you have got the source, drain and this is the fin; which connects the source and drain.

In fact, the channel is found there and if I have the gate only in this portion; this is a oxide and the poly silicon or metal gate; that is this. I am not showing multiple fins only one fin, if I want to have multiple fins that will come parallel to these fins and the gate will be formed around that.

So, the inversal air is just formed just below this gate; that means; the channel length is from here to here; that is the channel length. Wherever gate is there below that there is channel, the width will be that portion; which is surrounding that channel like that. So, that is a width; it is not all round, some time they call it also all round gate; it is there from all the three sides. And here, as I already pointed out thickness; see this is the back gate, this is the front gate you can think of.

Usually, we have it like this top gate and back gate; now you have it like this, you have call this as back gate this as front gate. And initially you got on the top, but that very thin so; that means, you have got S O I layer; this whole thing is S O I layer, you have prepared the whole thing by etching the S O I layer here. See this is the buried oxide on it you had a S O I layer, you have etcher this portion and you are realize the transistor like this one device I have shown. So, the width is whatever is surrounding that channel is the width of that; that is h; twice height plus the width of the fin.

So, whatever analysis that you do for; double gate MOSFET holds good; front gate and back gate you can use it. And the thickness of the S O I layer in that formulae will be the width of this layer. So, that is the thing now what? Why I have brought this out is; this fin portion is very narrow. And between the channel actually starts from here, this is not inverted or anything and this will be N plus doped up to that point.

But because this is very thin, you will have lot of restrictions coming into there; probably by a, area of cross section to a current (Refer Time: 04:28) you have to make it thin because you want this as; that layer to be very thin when the gate comes in on that. So, you cannot make it wider. So, that is where the series resistance come to picture, that is where the problem is there when you go to smaller and smaller scale MOSFETs for which this Fin Fet is relevant.

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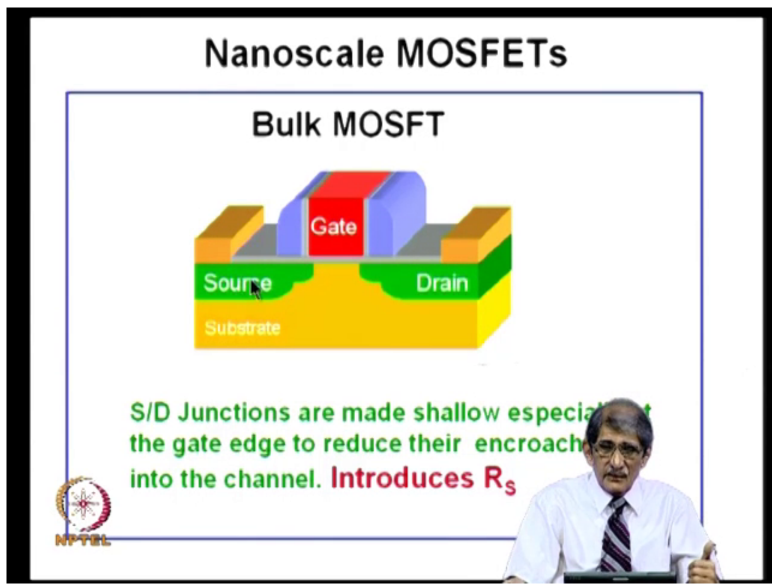

And if you take a look at the conventional MOSFET, there also you have the problem. There you have this implanted region at an angle you implant; to change the doping concentration there. And this thickness of this source region is less here; even here, you would like to use shallower and shallower junctions. Because if your scaling down in the lateral direction; vertical direction also you must scale down; rays there will be lateral junction formation will be there.

So, it will spread laterally also; if you diffuse deeper, it will be laterally also. It will implant afterwards you are inhaling that will be move down, little more also that little more that laterally. So, you are making it shallower and shallower junctions; so, make it shallower and shallower again use a current flow in this direction, I can just show that here.

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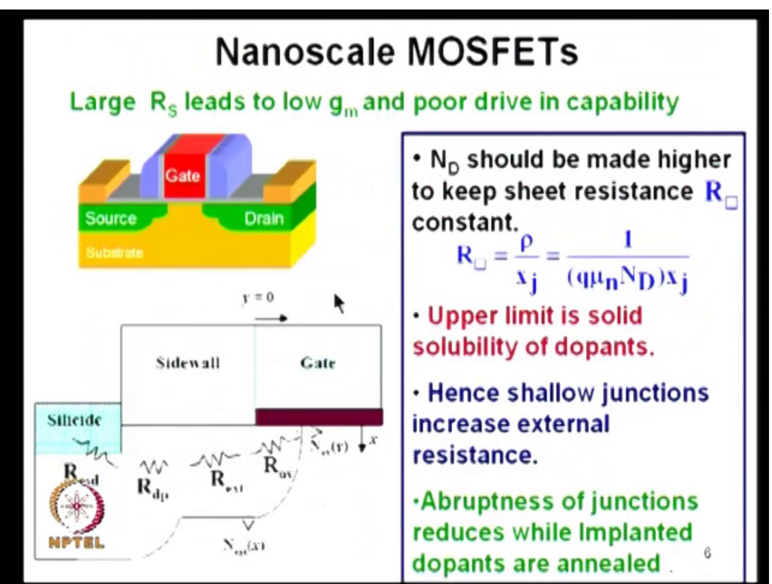

See this particular portion; again I have put here, that is a metal contact from the metal contact which is may be silicide; through this N plus region flows into this channel here; channel is here; this is a gate, you see this spatial layer that layer; I expanded it and shown, this small region I have put it like this to magnify the impact of this resistance; I have put it there.

So, this diagram is same as what we have taken here; junctions are made shallow especially at the gate edge; here to reduce their encroachment into the channel, that introduces lot of restrictions; this portion. Now, how can you reduce the series resistance? You can reduce the series resistance, by reducing the sheet resistance. Sheet resistance is defined as resistivity of the layer; divided by thickness of the layer. And what is resistivity row? 1 by sigma is resistivity and sigma is q mu N into N D and x j is the depth of which is going.

So, if I want to reduce that R; that is this resistance comes in here, I can reduce the row or I can increase x j, but increasing x j is not allowed. Because, while scaling down the devices; you want scale down in the vertically also. So, x j you cannot increase, you want to keep it low, the only parameter that you can manipulate is row. Row, it depends upon 1 by and N D; doping. So, you can increase the doping; already you are attempt for twenty doping concentration, the source drain regions.

So, you cannot go beyond that point because the upper limit on this doping concentration is decided by the solid solubility limit; means there is a limit up to which; the material for example, silicon can absorb the dopants without losing the crystallinity; that is a solid solubility limit.

For example, if you put phosphorus; you may get something like five times 10 to the power 20; per centimeter cube. If I am using boron, propitiate; you will get something like 10 to power 20; for its solubility; so, the upper limit on that. So, the only way you can reduce that distance is; go to at different material, change over from the semiconductor there, change over to metal; metal will have lot of carrier concentration, 10 to power 22 or even more; of that order.

So, you can increase the carrier concentration very much, you can reduce the resistivity, you can reduce the series crystal; that is the goal. So, shallow junctions increases the external resistance and also in the case of this type of junctions; because the profile goes something like that gradually, it is not abrupt. If it is abrupt, you know you have got entire layers same doping right through.

So, you have got a region where the doping is getting down to lower level. So, that is why if you put a metal; the whole thing can be thin; at the same time it will be just one sheet there, you can put thicker metal; if you like, so that is the idea.

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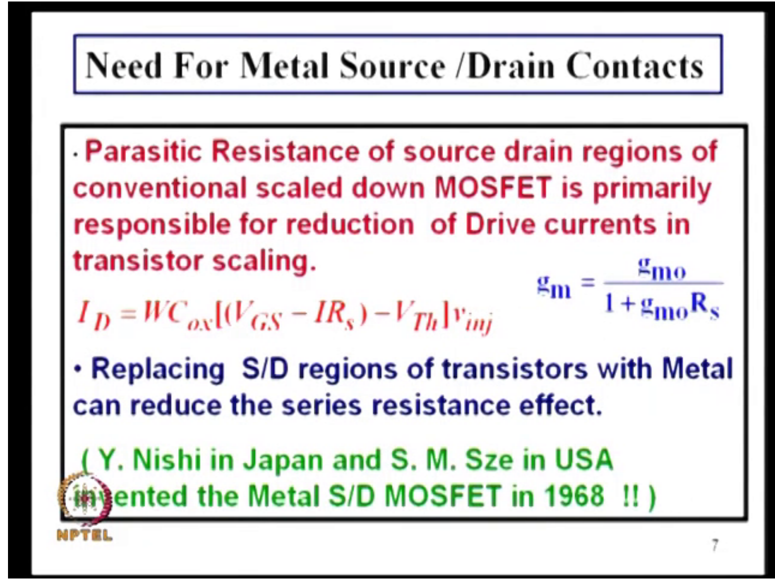

Now further; metal source drain contacts have further benefits; one is parasitic resistance of source regions of conventional scaled down MOSFET; whatever I told I have written here is primarily responsible for reduction in the drive current. How do this happen? This equation; whatever gate voltage you apply, part of it goes to the resistance resource; what is available for creating the channel is less, for a given voltage. So, drive current gets reduced; so, speed of the device gets hurt; if you cannot drive a capacitor fast, the speed to be slowed down. All these MOSFETs are required to drive the capacitor as charge them.

So, they must have higher transconductance g m; g m is delta I D by delta B; for a small change in the input signal, the current should change quite a bit; that is a indication of g m. Now, I do not know whether you remember this; if not I will just put that see how this you; g m, due to the presence of I R; R S; series resistance turns out to be g m 0; that is transconductance without the series resistance and R S; it is related like this; let us quickly; maybe I can just go through that; see for example, if I take the MOSFET.

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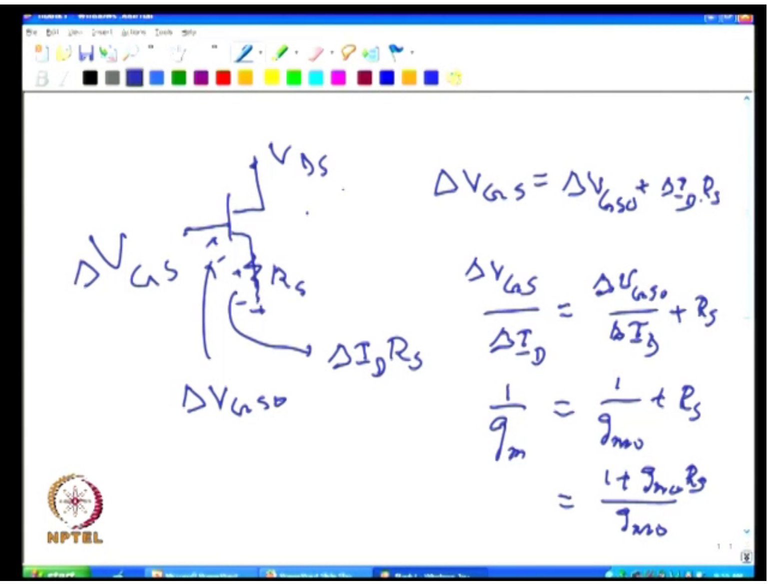

I have a resistance there R S; that is a source resistance. Now, I have the V G S applied; now or I say what we are trying to find out is; V D D is there V D S; what we are trying to find out is, if I have delta V G S here; how much is the delta V G S here? How much is the delta V G S here? So, this is actually delta V G S 0; if R S is 0; delta V G S equal to delta V G S; 0 and this drop is delta I D into R S.

So, you have got delta V G S equals delta V G S 0 plus delta I D times R S. Now, divide delta R by delta I D; see what I want is, delta I D by delta V G S. So, delta V G S by delta I D is equal to delta V G S; I am writing as divided by delta; that is really bad. So, that is; delta I D plus R S; so, this quantity first term is 1 by g m; that you get and this second quantity is 1 by g m 0; g m you would have got 52 were equal and plus R S.

Now you can now go back and see that the g m; so, this is actually equal to g m 0, 1 plus g m 0 times R S. So, now you can see g m is equal to g m 0 by 1; by 1 plus that. So, this is what we have said there; so, what happens is; now your g m becomes like that. So, it comes up by that; so, you can see if R S is large; g m is correspondingly reduced.

Now, R S becomes larger because of these shallow junctions and Fin Fet; all those things. So, there is a need for reducing that R S, to increase the I D and also to increase the trasnconductance, to increase a driving capability. So, replacing source drain region of the transistors with metal can reduce the series resistance effect, now if you see what it is going to be.

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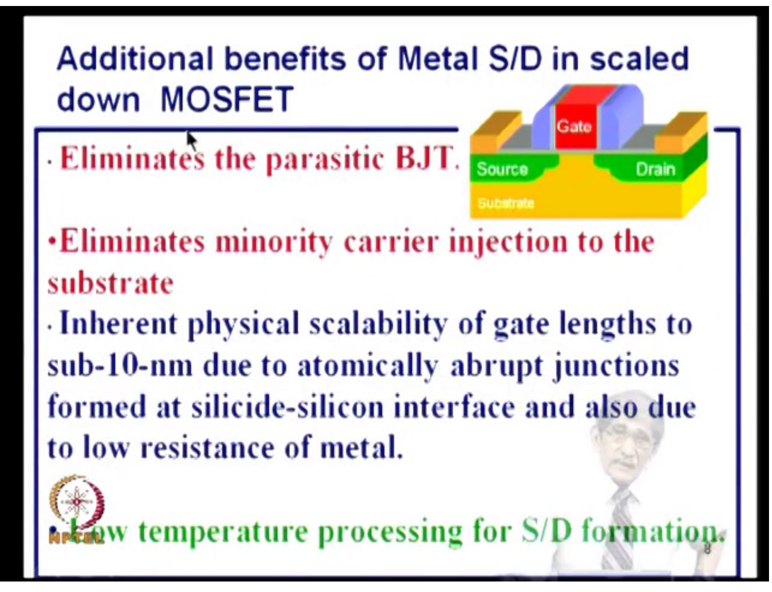

Now, there are other benefits; one is series resistance gets reduced, other one is; in a conventional transistor you have got; n, P N that is a bipolar transistor come into picture. Particularly, if the S O I device; if you do not have the count contact, that is a very much dominate. So, if I replace the junction the metal semiconductor contact; you do not have the transits reaction; bipolar transits reaction is not there. So, that we will understand

better after we discuss how that eliminates that; when we discuss the metal semiconductor contact.

And also because there is no P N junction, there is no minority carrier injection there, which to substrate. All those effects which you do not like are eliminated by putting a metal semiconductor contact. Still you have got to see how? Whether it works like a transistor by the MOSFET. So, you can use the abrupt; atomically abrupt junction by using a metal on the surface.

So, all those limitations of shallow junctions etcetera goes off with this. Further, if I am replacing this junction with a metal semiconductor contact, your processing temperature goes down; because you are just evaporating metal; at the most you may do some sort of annealing at about 400 degree centigrade. So, that way your thermal budget; on the wafer is reduced, that is one of the very important things people worry about, try to process at as low temperature as possible to keep for a bigger wafer; wafer work page etcetera is reduced to process at low temperatures. You have to work, worry more and more these, if you go to 8 inch, 12 inch.

All that effects you try to minimize. So, lower temper do not be carried by a low temperature; initially when you have to go to a physics person, specialist; low temperature he will limit a thin to have generic temperature, but we are talking about low temperature; if it is a 500, 600 centigrades is low for us, for processing.

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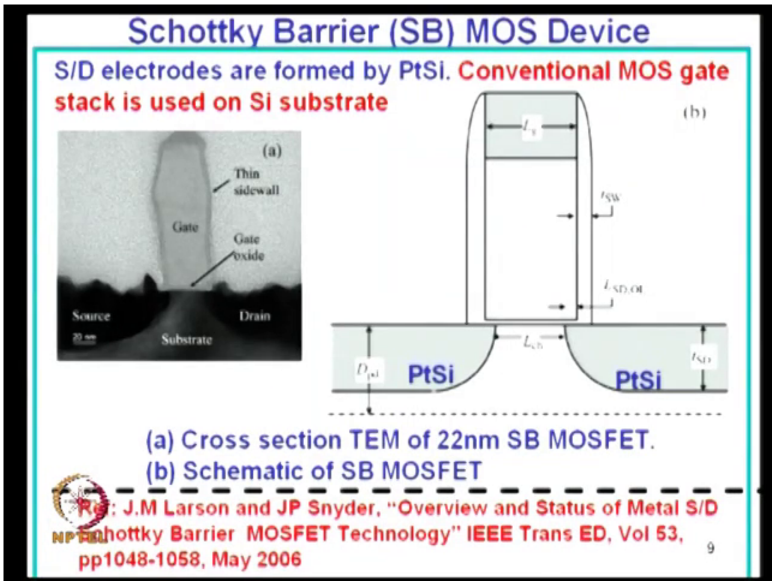

So, this is actually just to show that really that type of devices have been fabricated; you can take a look at one of the papers which has come to which gives a very good review even as 5 years back. Even now that is a classic paper which people; will refer; so I put it here; in I triple E transaction electron devices; it is a long paper, which gives there are some sort of review of the devices. This is the cross section; t m cross section of; at 22 nano meter Schottky barrier source drain metal contact, this is the gate and you can see this; I do not know, you can see the dark portion there.

This is shown here by this portion; this is a platinum which is silicide which acts as a metal semiconductor contact. There is no junction, so in the previous case you put some silicide etcetera you do; how do you do? You have that there; N plus is there, junction is different, but now you that has the use platinum, silicide as the metal semiconductor contact.

There you can get a junction like this, which goes underneath that, you can get self aligned structures. We will come back to this when we go to transduction; right now what you want to take a look at is; this is a schematic of the Schottky barrier, these are all the depletion layer width; let us not worry about it at this moment, we will have occasion to discuss details of this, when we come to transistor. So, main thing that focus is you can get the metal semiconductor of this shape. You can get abrupt junctions here and you can get this gate; which is poly silicon and you have got this spatial layer on both sides that I am sure; it has been illustrated in the previous lectures.

So, you have got the spatial layer. So, that there is no sorting effect when you put this platinum; you can just lift off that from there and you have to platinum on here till side it is spread laterally underneath into that. But this is not like spreading in to the junction, it will just small spreading.

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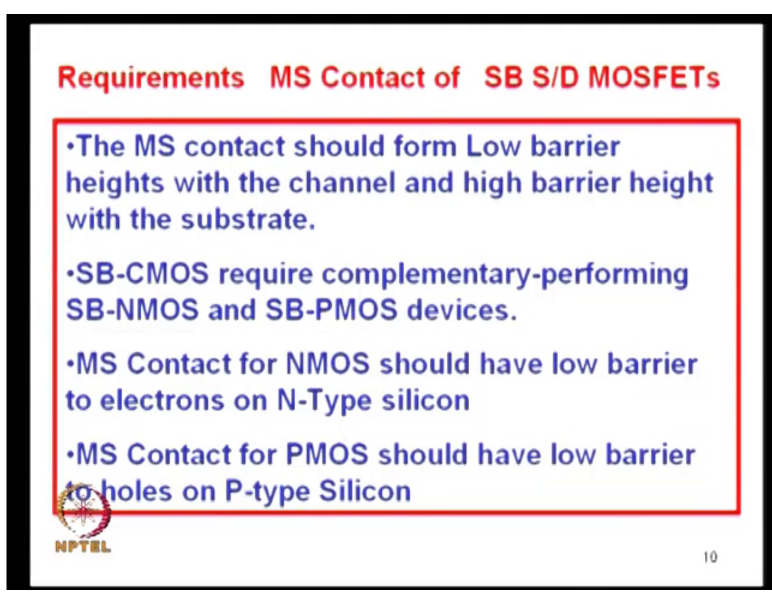

Now, what are the requirements here? This metal semiconductor contact should form a very low barrier here; if it is a N channel device; to be N-type region, it should form a very low barrier. Why should it form a very low barrier? It should be able to inject electrons to that barrier; through the barrier. And also if it is a P-type substrate, it will form a rectifying contact. So, there is requirements it will make a good ohmic contact on to N-type material; it would make a good rectifying contact on P-type material. So, when we have a inverted channel here, that will form a ohmic contact there.

So, these are the requirement which I have put here and they are summed up you know whatever I said is summed up here; CMOS; you have N channel, P channel both. When you put a metal; you will have N channel there. So, you must have a ohmic contact on to the N channel, if it is a P channel you will have N types of substrates P channel here; that should make ohmic contact to that. So, there are conflicting requirements here which can be met by how we will see.

The idea may not be very clear right now, but when you talk about the metal semiconductor contact, it will become clearer. In fact, few years back; people were not talking much about metal semiconductor contact; it has only a part of syllabus; where somewhere they put one 10 minutes discussion on that and proceed, but today it has become a matter of research, lot of discussion are going on all that.

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Now, let us get around the quickly on to; it is a very simple concept, you can go through that rather easily by discussing. First, when you say; you need to have a low barrier height means, it will be ohmic contact. So, on to channel you would prefer; a metal co making ohmic contact; on to substrate, you would have rectified contact; what are they? Ohmic contact; low barrier height, rectifying contact; form higher barrier height. In MOSFET, metal semiconductor contact at the source would form an ohmic contact to the channel; Schottky Barrier junction leads to fundamentally different mechanism that is what I am; other thing right away.

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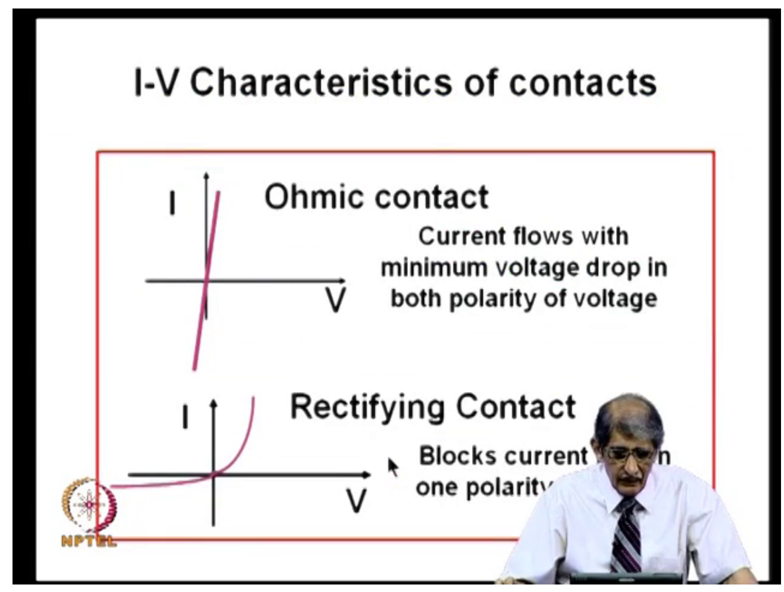

Now, ohmic contact I V characteristic like that; anyone knows, ideally it should be vertical; 0 voltage drop, but you can never get 0, there will be finite resistance, rectifying should have block current from this direction and its delve the current flow easily; ideally it should be vertical here, 0 there you never get that.

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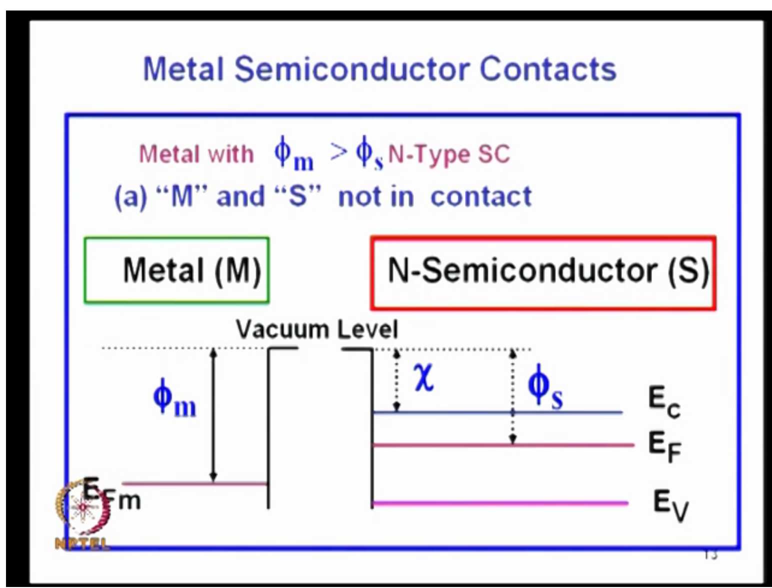

So, now let us get down to discussion on; all of you are familiar about the energy band diagram. So, it becomes very easy to analyze this metal semiconductor contact; the energy band diagram. This is a metal block; this a N-type semiconductor, they are two are separated; they are not connected, they are neither physical in contact nor electrically in contact.

So, metal has got the Fermi level there and that is a vacuum level. So, what should do is; you have the term called work function difference, which actually is the energy difference between the vacuum level and the Fermi level. Virtually, it gives an idea how much energy you want to supply to terms to take it away from the metal.

Say for example, if you take a metal, if you heat up red hot; it emits electron; that is you are giving energy much more than that 4.5 electron volt energy by heating with red hot. If you see the old vacuum tubes, you will see that there is a filament which is heated, which is a source of electrons. So, that is a by; for a function phi m, now semiconductor if you take; the vacuum level is same here, conduction band, balance band, N types of Fermi level is closer to conduction band and there is a term called the electron affinity

that is chi; that is the energy difference between the vacuum level and the conduction band edge.

And the work function of semiconductor phi S is; the gap between the vacuum level and the Fermi level. Now, next what we do is; so, we are taking a clay case where phi m is greater than phi S; like this. So, you can immediately say that; if you join these two metals, need not join; keep them close by, connect this by external wire, it becomes a complete system.

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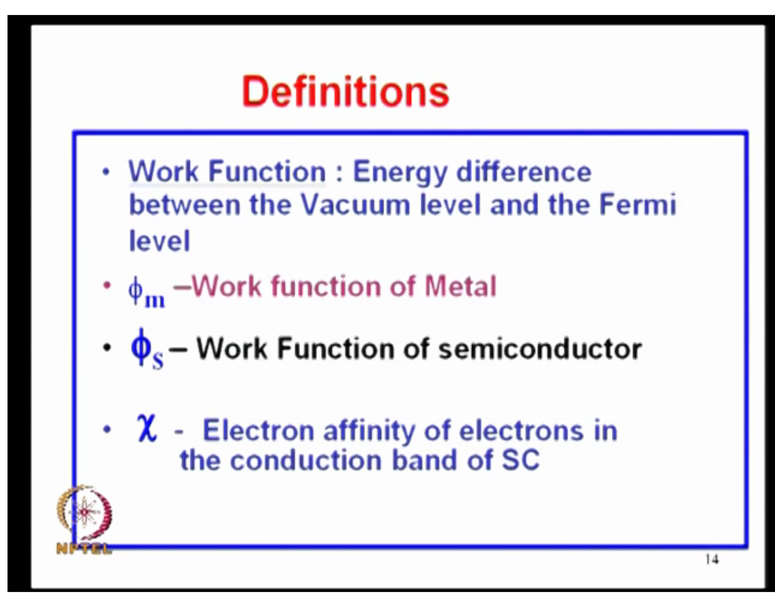

These are the definitions.

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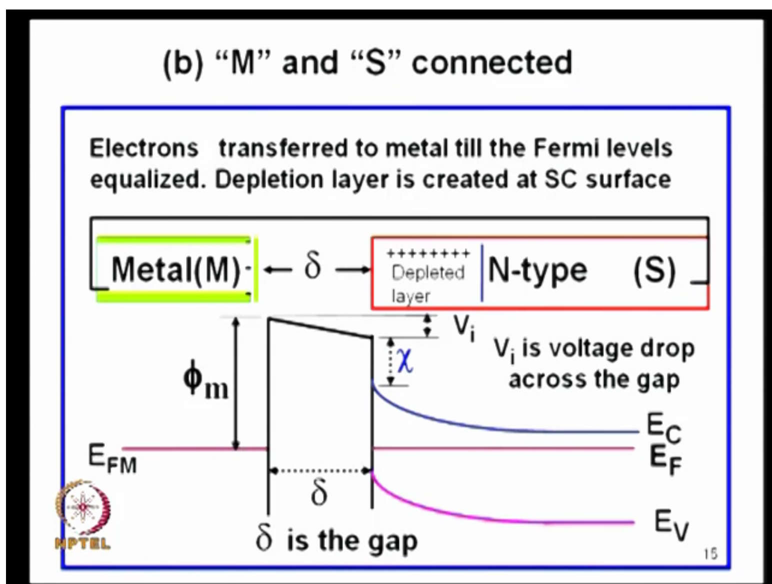

So, when I connect them together; there is a gap that may be a small gap, this is a complete system. So, what happens is because here; because the Fermi level is above this; and there are lot of electrons at a higher level here occupied because it is N-type, there are lot of states available here; the electron like in P-N junction, electrons will get transferred from the N-type region to this metal.

So, leaving back at depletion layer plus charges behind here like that; the plus charge is the depletion layer, a finite width here and their trans have gone; transferred on to this up to this negative charges here, 1 negative charge I put here indicating there are; if there are 10 charges here, there will be 10 charges here, so many electrons have transferred. Now, this is; what about energy band diagram? This layer is depleted, metal the number of electrons are very high, there is not be a layer, there will be charge sheet of large concentration electrons on the very surface itself; that is why it do not have a depletion layer or accumulation layer.

It is a charge sheet there, now if we take the energy band diagram; this is N-type, this is depleted and plus charges are there; through this gap the electric field will terminate on to minus charge because plus charges will look for negative charges, they are here because they have been transferred from here to here. So, you have got a analytic field from the semiconductor to the metal surface; here it is distributed charge, here on the metal it is charge sheet completely.

So, because there is electric field from this side to this side; the energy band diagram will be moving in this fashion; because this is negative, this is positive. So, if I have to take an electron from this side to this side; further it is more difficult because plus minus; that field is in from right to left; therefore, it become difficult to take electrons from the right to left. That means, the energy band diagram will be moving up, this is getting back again to the basics.

Similarly, the electric field; this will be maximum here, but it will be varying here, it will be linearly varying potential will be parabolic. Like all the discussion that we have been doing, so we have got the N-type material here. And as you move from here to here, more and more depletion; it becomes less and less N type. So, you can see the conduction band moves away from this Fermi level.

So, conduction band moves away from the Fermi level; telling that this is depleted and this energy band diagram is bent up to here telling that electric field in that direction. So, and delta is gap; now what I do is these are standard text book; everywhere you will see these type of diagram, including the book which we had written Achuthanand Bhat; that also all the diagrams are there. So, I reduce this gap, the charge transferred remain same thing because this has happened till the Fermi level has equalized, you do not draw the Fermi level here in this enthusiastic portion.

You do not; that is not have any meaning because it stop it there, they are equalized.

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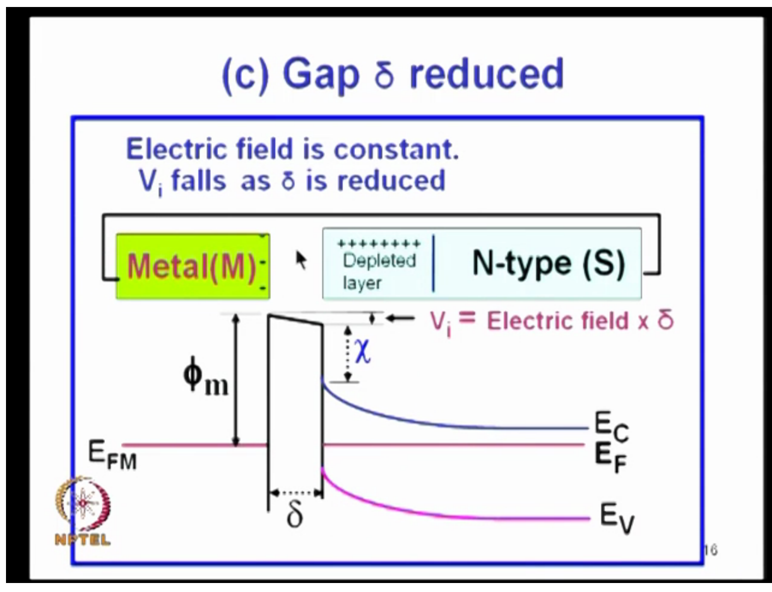

So if I reduce the gap, the charge here and charge here is not changed, but the gap is reduced; what will happen if voltage is reduced? Field lines are same; number of charges here, number of charges are same thing because has a hybrid transfer and bring the Fermi level equal. So, because the charges are same; the gap is reduced, the voltage drop is reduced. See the chi; see this is a vacuum level, whatever potential change is there in energy band diagram here, is reflected on the vacuum level also further reduced.

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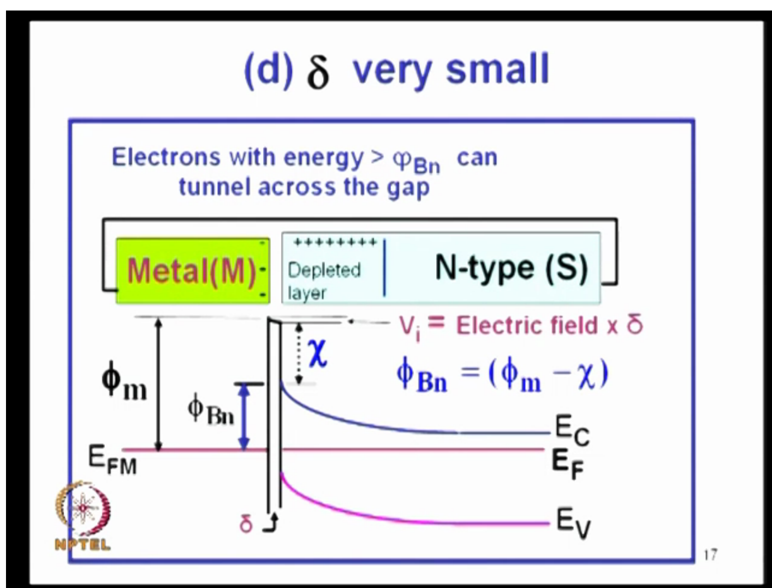

I reduced it further, the voltage drop is reduced further; there is a small voltage drop in that layer. If there is a; this layer could be as small mono layer of oxide even present there, which usually is present; so, that is a thing. So, you have got electric field here, electric field here there is a drop; V i across this layer.

Now, phi m is that per function difference here; to the vacuum and there are drop here or voltage raise here, this is a conduction band edge in semiconductor; chi is here. So, the vacuum level is slightly dipping here because there is voltage drop; all the energy band diagrams bend, only which does not bend is Fermi level; thermal equilibrium situation.

So, phi m and this particular height; energy difference, this as I pointed in written it as phi B n; which is in electron volts. I call this as a barrier height for electrons, I call this as barrier height because if the electrons have energy greater than phi B n; after all in the metal, at room temperature there will be electrons beyond this point, they will be above

the Fermi level, they will not only be here; at 0 degrees of course, there will be no electrons above that.

But at room temperature; there will be electrons from here up to certain height. Now, all those electrons which are having energies above this phi B n; find a very thin layer, they can cross this by tunneling; if it is 1 nano meter or of that order; two of electrons which have energy greater than can tunnel. So, phi B n is the electrons which are having energy less than this; that is phi B n; they cannot wrong; because there is a this region there are no states; these energy gap, there is a band gap here.

But here immediately it sees the available states in the conduction band all this things, now they can tunnel. Similarly, electrons present here can tunnel from here to here. So, we can discuss this; ideally when you talk of the Schottky barrier or metal semiconductor contact, you do not show this layer; because that is not really coming into picture.

Because, carriers can tunnel from here to here and here to here; so, phi B n is phi m minus chi; if that drop is negligible; it is phi m minus chi. So, normally you do not show this gap.

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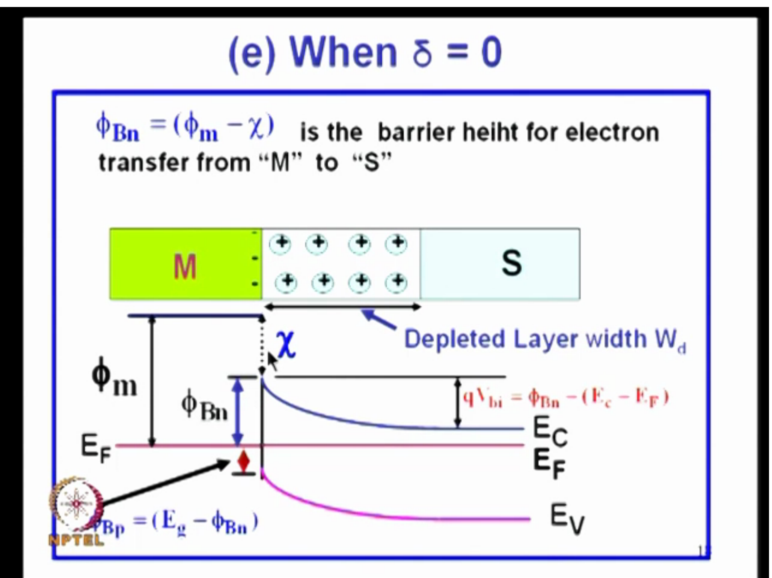

So, that is what we show; so, wherever you see the energy band diagram for metal semiconductor contact, you will see only for N-type like this. So, Fermi level of metal; a land with respect Fermi level of silicon and there is depletion layer here, depleted N-type

material has got plus charge and the minus charges are present here on surface; which will terminate on this.

So, entire voltage drop is across a depletion layer here; so, here to here there is voltage drop. So, phi B n is that barrier height; whichever; what we have discussed that is phi m minus chi, phi m minus chi; it is a phi B n; that is 0 level. Now, wherever there is a depletion layer here under thermal equilibrium conditions, you have got what is known as the built in potential.

Just like in the P N junction; in a P N junction, that is shared between the P-type region and N-type region. Here, it is entirely on the N side; there is no voltage drop in the metal; so, this is a built in voltage. So, built in voltage is actually the voltage raise from here to here like this; if I know phi m; birth functional metal. And if I know chi; electron affinity it is known for a given semiconductor.

For example, for silicon it is 4.05 electron volts; for gold it maybe close to about 5 electron volts; phi m. So, phi m minus chi is known because of materials there, you can even measure it; from the characteristics of the device. So, otherwise you can say; once you know phi m and chi; you know what is phi B n is. Now, once you know the doping in a semiconductor; you know what is the energy difference between the conduction band and the Fermi level? So, phi B n minus E C minus E F; gives you that q into V b i.

So, built in potential is related to the barrier height and the doping. If the doping is higher and higher, this will not change but the E C minus E F will decrease and therefore your built in potential become closer and closer to phi B n; this is ideal.

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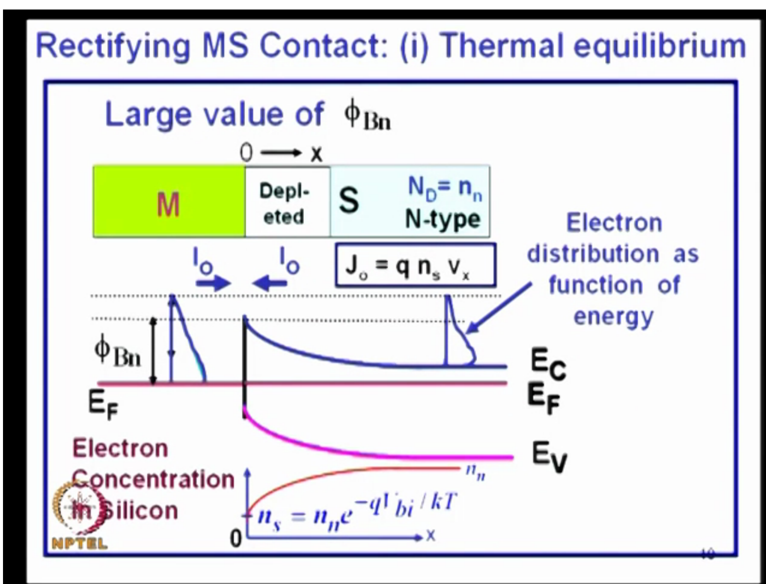

Now, let us just go further in two thin; this is we will see that, a structure like, this a metal semiconductor contact entire material with phi m, larger than chi will act as rectifying contact. Because there is large barrier for electrons from either side; how does it work out, let us see. Thermal equilibrium situation; I do not know, whether you understand this type of diagram.

I have redrawn, whatever I have drawn here; I have redrawn here, instead of putting this plus minus I just put depleted layer and there is negative charge here. On the left hand side; I have shown the distribution of electrons, because there will be; in the metal energy levels will be there continuously.

But the probability of occupation goes down from as you go from the Fermi level up; let me just see whether I can; I will put that diagram.

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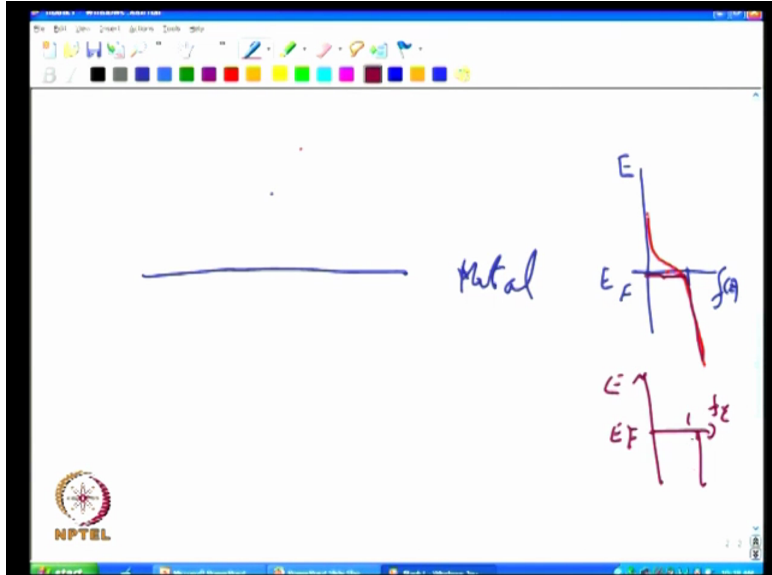

See what happening in the metal is; in a metal, you have got the Fermi dirac distribution; how is the Fermi dirac distribution? Energy verses formative occupation, if you take; that is one; the E F; now if I draw a Fermi dirac distribution like that; it is half there, at room temperature. As 0 degree how is it? At 0 degree is like this; I just redraw that, at 0 degree it is f E is 1 here, E F it is like this. Below Fermi level all the levels are occupied, above that they are not occupied; now let me just go back to this and see where I can remove that. So, just make it; my god everything gone; let me just clear out everything.

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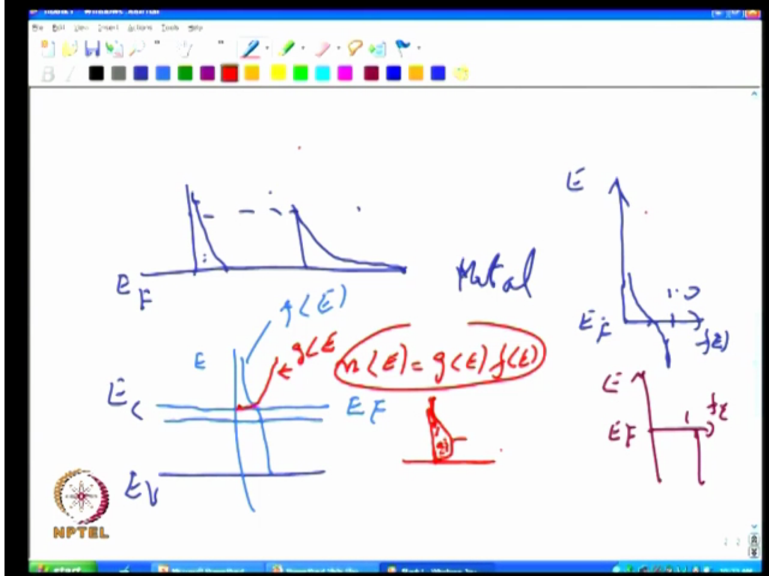

Let us redraw that once again f E and energy that is 0; E F. So, above room temperature; it is this is 1; how it going like that, formative occupation half there. That means if there are levels there, the implication is; the Fermi function you write it as 1 by 1 plus E to power E F minus E minus E F by k t; that is the plot there; that is the Fermi function; probability function.

So, when you write like this; meaning is, if there are levels present above that; that will be occupied. So, in a metal; what I have drawn is that is like that; in fact it will not be precisely like that, it will something like this; that is it will be going down something like this. Below that I am not showing; that means, these electrons curve, they have got energy above the Fermi level.

So, if there is a barrier like this; if I have barrier in this fashion; that is the barrier phi B n; these electrons over that can cross. There is nothing which going there to there and if there are electrons on this side, they can cross on that side. Now, how is it in the conduction band, semiconductor; you have the Fermi level here, I am sorry that is being; we are put it like this. We have the Fermi level here; here Fermi dirac distribution will be how will that be? I will put it like that E F is here, your Fermi dirac distribution may be something like this; I am sorry the problem of not drawing in beforehand. If this is 1 there; what happened? It is taking a bit time; I hope you do not mind this; why have this, just a one minute; try it once again. See, what I am trying to draw is the; Fermi dirac distribution on this graph, where that is the Fermi level.

And now you will have the line there; energy, this will be half here; like that, probability of occupation that is the f E. What about density of states? In the conduction band; it continuous, but the density of states is something like this; 0 there and goes like this. So, the N at any E is equal to; if I call this as g times E; density of states, g times E into f E.

So, if I draw; that is this is a probability, this is the density of; that is at conduction band edge probability of density of states is 0, it keeps on increasing, for probability keeps on increasing. So, your next distribution comes like this; something like that, see this is 0; probability is there, but; so, the if I go from here to here; if I draw the product, these two things together; that will be 0 here, it will increase; then go down like that. It is even though you find out effective density of state with respect to conduction band.

The actual distribution will be like this; there will be 0 here, number of electron as you go away from the conduction band, it will slightly increase then fall down to 0. See product of probability because if probability decreases, density also increases; product actually goes through the peak somewhere here. So, now let us go back to this diagram now I have drawn that here this is a density electron distribution here.

When integrate the whole thing; you get that N c; you find out effective density of electron when you find out; you integrate the whole thing there. So, here you can see now under thermal equilibrium conditions; you have got this distribution like this, which is above that here. So, all those electrons here can move that side; all those electrons from the metal here; under thermal equilibrium when the Fermi level has equalized, definitely number of electrons which are able cross somewhere it here; must be equal to number of electrons crossing from this side to this side.

I can write; I will write say that the current density due to the electrons moving; from the semiconductor to the metal because they have got energy above the barrier; these are the barrier, is I can write it as q, the charge the electrons, N density of electrons; here whatever electrons are available here will have thermal energy or thermal velocity v x in that direction; because we are taking one dimensional case. So, across that barrier how many electrons per second are crossing? That will give rise to current density. So, I can find out this current I naught; if I know how many electrons are present here; because all of them can move here.

If you plot the electron density from this end to that end; see we put it as a depleted layer, when you say it is a depleted layer, the implication is there are no electrons. But from here to here; if you go there is a potential variation, if there is a potential variation like this plus minus; that means, electron concentration is decreasing exponentially with respect to that.

So, if the drop from here to here is V b i; from that point and that point it is V b i, the electron concentration just at the edge of this metal semiconductor junction; will be whatever electron concentration there in the semiconductor, bulk multiplied by the bulky sent n electron concentration; N region multiplied by E to the power of minus V b i is a potential drop; built in potential; n n into E to the power of minus V b i by b t; b t is k T by q; this is the Burson's law, but there is no current law. I can say that carrier

concentration is that; now all those electrons are having thermal energy because of that they are above this barrier.

So, those electrons can cross from here; if we have a directed field they will be move in that direction otherwise it will moving up and down. So, we are considering that the electrons are moving here with velocity v of x. So, the current is q n into v; that I think; that is the basic equation, which used even when deriving the MOSFET equation; charge into charge density into velocity; that is the current density. I multiplied by area; I get the current.

So, from this semiconductor to the metal, there will be current I naught; what is the current flowing from here to here? It would have to calculate because you know the current net current is 0; so, from here all these electrons which have high energy; should give exactly opposite current. So, what we are saying is; when the energy band diagram is like this under thermal equilibrium conditions, there is exchange of electrons; free exchange from this side to that side.

And I think that current is 0; whatever is injected from metal to semiconductor is balanced by whatever injected is from semiconductor to metal. So, this is energy band diagram under thermal equilibrium conditions. Now, let us see what happens? When I have bias condition? How does it work out as a rectifying junction? So, I hope this diagrams all are clear; electron distribution are function of energy here and here.

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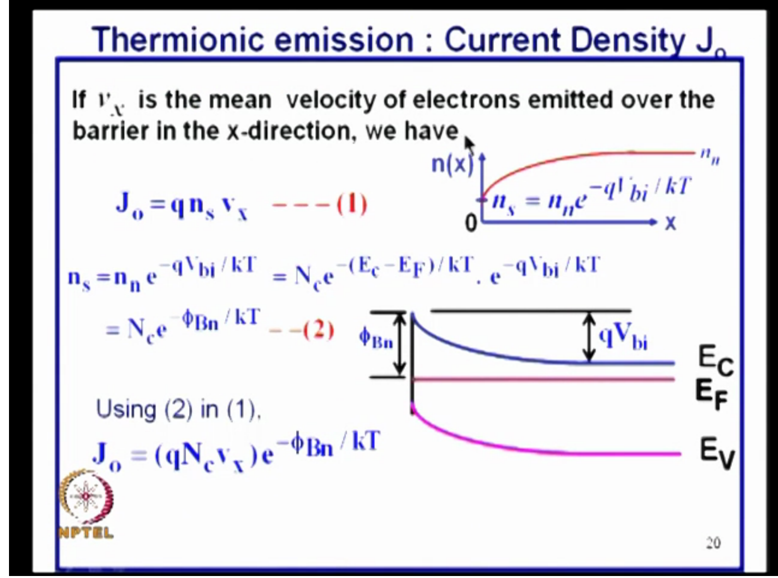

Now, what we have shown is; whatever I had discussed there, put it in terms of the equation. We are considering only this now; that is n of x is like this; J naught from metal semi conductor to the metal is this; q n into v of x and n s is equal to n n into e to power minus k T; we are trying to get compact. So, what is n n? In entire material, the electron concentration is equal to effective density of states into E c minus E F by k T minus; this is a standard formula.

So, that is the standard formula which I have substituted for n n; this term, into E 2 power minus k T; I will restated whatever I have written there; by substituting for n n. Now, what is this quantity? e to the power minus E c minus E F into E to power minus q V b i by b t; what is their quantity? E c minus E F is this, q; V b i is this and E c minus E F; plus q V b i; is this quantity and that quantity is nothing, but phi B n. So, what we are telling is this whole thing can be put as N c into e to the power of minus phi B n by k T; because some of this two with that; that is phi B n. So, that makes it simple; that means, electron concentration there here is equal to N c e to the power of minus phi B n by k T.

Now the J naught; what was J naught we said? q; n s into v of x; n s is this one; q is there, I substitute for n s from here; see 1 and 2; n s is given by this. So, that is q; N c into e to power minus phi B n by k T phi v x; same thing I read it out. So, this quantity inside here; is decided by the density of states and the thermal velocity of electrons in that direction.

And so, J naught now you can see initially what you refer to in diode J naught, you will see that; this also for this diode also; that is the reverse saturation current we will see how it is; that depends upon barrier rate phi B n. And phi B n depends upon phi m minus chi; so, J naught will be lower; if phi B n is larger; J naught will be higher, if phi B n is reduced, low barrier rate J naught to be have.

Now, you can see that if we have a diode which is J naught is very large, it will look like a very leaky diode, will look like a ohmic contact. So, you can straight away say; that if I make a device where the phi B n is low, it will look closer to a ohmic contact. If I make a phi a device with a phi B n large J naught will be low it will be it will be closer to a rectifying contact; we will see how it is.

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$$J_o = (qN_c v_x) e^{-\phi_{Bn}/kT}$$

Substituting $N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2}$ and $v_x = \sqrt{\frac{kT}{2\pi m_n^*}}$

$$\boxed{J_o = A^* T^2 e^{-\phi_{Bn}/kT}}$$

$$A^* = \frac{4\pi m_n^* q k^2}{h^3} = 120\frac{m_n^*}{m_o}\ \mathrm{Amp/cm^2/K^2}$$

A* is Richardsons Constant

So, now I just rewriting this again J naught is equal to that quantity, now we have to recall some of the formulae that are available already in the basic device; basic that you have studied earlier and see related to that effective math of electrons k T and Planks constant and this 2 pi by 2. So, N c is that quantity and just substitute enough for this and b of x for electron gas, the thermal energy root k T by 2 pi m n star; multiply these two together and simplify, you get some constant A star; all this, you know all this things will have been constant; here T to power 3 by 2 is there; here T to the power half, you get T square.

And other things are constant that I put it out as A star; when A star is this quantity. What is m n star? Effective mass; effective mass is mass of electrons in the semiconductor; which will be different from the mass of operates on free space; because of presence of built in electric fields, when electron moves from one location to another location. So, to make life easy for us; so, that we can use still use metal force; laws of force, you make use of force is equal to mass of index acceleration; talk of effective mass, so that is effective mass.

So, it is A star; which constant T square comes from here into that same thin whatever I written there is here; J naught will be A star; T square e to the power of minus phi; B n by k T and A star when you substitute for all this quantities q k phi etcetera, you will get 120; m n star by m naught ampere per centimeter square, per degree k square.

Why I put in this form is, the m n star by m naught depends upon the semiconductor. If you take silicon, it will be almost close to 1; slightly different. If I take gallium arsenide; it will be 0.067; that will be very very small. So, this A star in the case of silicon will be close to 120; slightly smaller, but in the case of gallium arsenide; it will be 120 into 0.067; it will be about 8 or so.

So that A star will be 8 ampere per centimeter square per k square gallium arsenide gallium arsenide. So, that is why I put this; because you do not have remember every time all the whole thin; 120 m n star by n naught; you will know the effective mass in terms of mass usually, we can get that constant. Calculation becomes ready for you; this squared into this phi B n; phi minus chi. So, that is what you get for; we have calculated this is the value that current that will transferred from here to here and here to here that is J naught; that current 0, thermal equilibrium.

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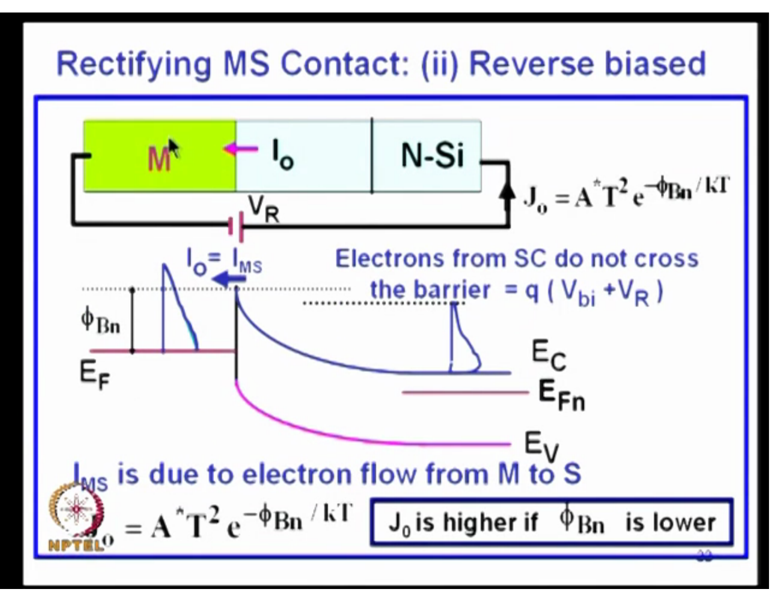

Now, reverse bias; I will at least be able to finish this, when the reverse bias what happens? If you see here, the Fermi level was here; when the reverse bias what happens to that? How do reverse bias? Like in the P N junction; P and N, if we have; here your metal and N, I make this N side plus; I apply voltage V R into that. The applied voltage will not appear across the metal, where the huge current will flow through that thing.

So, because it is like a metal and a interacting layer here depletion layer. So, the entire voltage adds on to the built in potential across this; depletion layer widens, the voltage of

across this layer increases becomes equal to V b i; V b i what are the polarity? Plus here minus here; plus, minus; you can see this; plus here minus here, band is like that its adds on to that depletion layer widens; that is a reverse barrier situation.

So, this portion; I am keeping it as it is with respect to that the voltage has increased here; that means, the band bending have taken much more. So, this earlier the Fermi level was coinciding with that, but now it has moved down by an amount equal to V R. So, entire energy band diagram; originally whatever was coming up here in this portion has come down by equal to V b i. So, if you go beyond the depletion layer, the charge distribution will remain to same thing.

Just I do not know; whether you can go quickly back see, whatever was here this portion has been pulled down. This in the neutral region this equilibrium diagram whatever I have drawn holds good, but beyond that point I do not draw the Fermi level; that has no meaning really, you call it as positive Fermi length. So, I just draw it here and here in this portion at a bend moved down because the voltage has increased that is moved down.

Now, what does happened to the charge distribution now? On the left hand side, the barrier does not changed; that is the key thing. The P N junction; barrier will change on the P side as well as N side, here the barrier does not change to whether no voltage drop on the metal, so barrier remain the same thing. So, all these electrons which are able to give raise to J naught or I naught from due to transfer of electrons from here to here, they will be there.

So, I have put a current here; in this direction implying electrons are flowing in that direction. See, this electrons are crossing from metal to semiconductor current from the semiconductor to the metal. So, there is that I naught component is still present to transfer metal to the semiconductor, but what has happened to the electron here? The electron distribution from the bulk is the same thing; number of electrons available in semiconductor in neutral region; that has not changed; that distribution remain the same thing.

Since, we have pulled the potential energy down; this actually is the energy distribution from here to here up to this point only. So, the maximum number of the electrons are available only up to certain height in the energy; beyond this there are no electrons. So, these electrons in apply sufficient reverse bias; they are not able to cross right to left. So,

whatever J naught was there from right left or whatever electrons were there from right to left is brought down to 0.

But whatever electrons transporting metal semiconductor are still there; that means there is a net transfer of electron from metal to semiconductor, there is no transfer of electrons from the semiconductor to metal. So, whatever was transferred from metal to semiconductor was I naught, but I have put I naught as at physical direction. Physical direction is opposite to the transfer of electrons, so you will have a current in the direction. So, this supply voltage into the metal giving raise to that same J naught whatever you have calculated.

So, with that I think we have just gone through the basic principles involved in the reverse bias operation or the thermal equilibrium metal semiconductor contact. More details, we will discuss in our forward bias; how it works, like rectifier; we will discuss in our next discussion.