Nanoelectronics: Devices and Materials
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Lecture – 22
Sub-threshold Slope & SCE suppression in FD SOI MOSFET, Volume Inversion and Ultra thin (UTFD) SOI MOSFET and quantization Effect, FINFET

So, we will continue our last session on the SOI MOSFETs and this is a lecture number 4, in that series of SOI MOSFETs, we will discuss sub threshold swing in a SOI MOSFETs and some short channel effects and the finfet.

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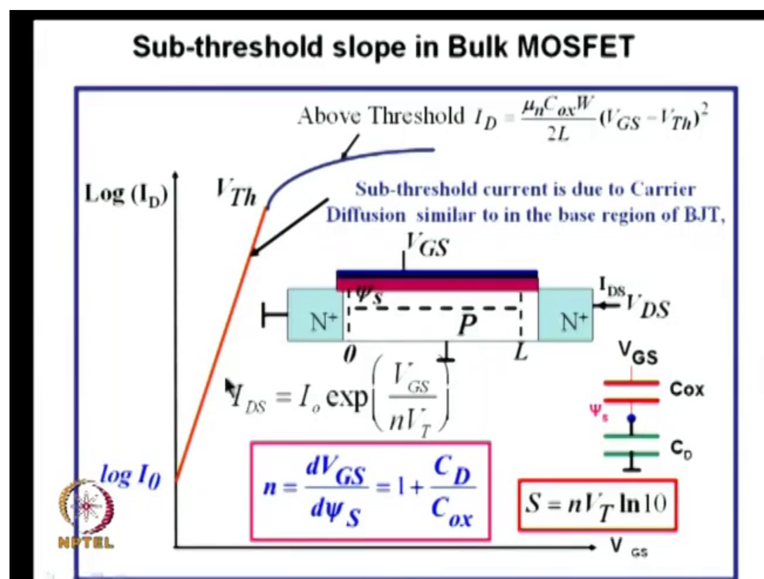

Just recall, what we did in the bulk MOSFET. This is sub threshold region, where you observe the current, below the threshold voltage. So, we saw that current is exponential there, given by expression like this. Now, n is the factor which decides so fast variable turn off, how quickly slope. So, n is equal to 1, we know that it is 60 millivolts per decade. So, you would like to turn it off with very fall change in voltage. So, and should be as slow to ideal as possible, 60 millivolts per decade.

So, we also saw that this n can be determined from this relationship, delta VGS by delta psi f s, it is a, it tells us the, how good is a coupling between the gate and the channel. If the delta psi s is delta VGS, coupling is excellent. Now, so, then n is equal to 1, but since there is a depletion layer is here, we saw that you can derive this delta VGS by delta psi f

s using this equivalent circuit. So, that we have shown that n is equal to delta VGS by delta psi f s using the equivalent circuit is 1 plus C D by C oxide, C D is the depletion layer. There is a depletion layer, there, their capacitance; this is a bulk MOSFET or partiality per unit SOI MOSFET, whatever, both same, C oxide per unit area, C depletion per unit area that is the thing.

Now, what we are trying to point out here is that n is the one which decides your sub threshold swing or sub threshold slope. You want to keep it as slow to one is to possible, now that n is decided by what is the capacitance between this point and a ground point in this case. It is C D. If there is another capacity of parallel to that C D like the d i t, we saw that will become larger effective capacitance becomes larger. So, this n become larger that is d i d increase, d i t increases the slope. Suppose, there is a capacitance in series of C D, then the entire C effective will come down. Let us see how it works out, as SOI MOSFET in the SOI MOSFET.

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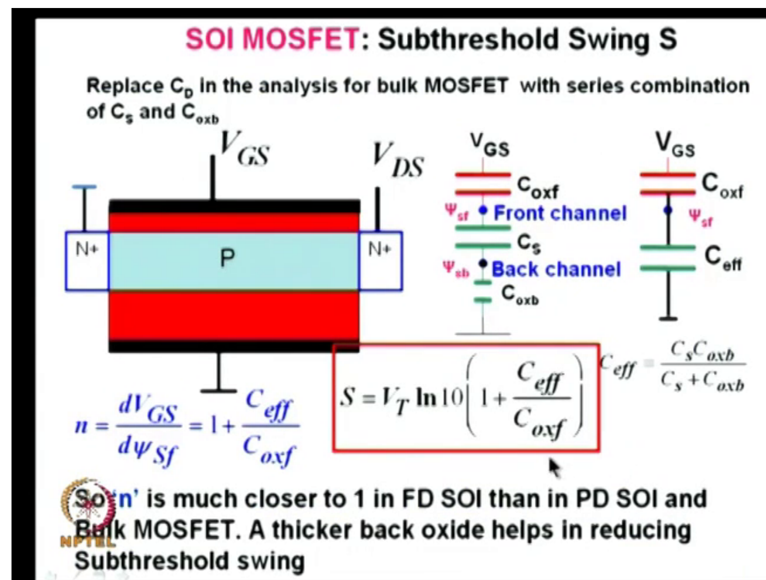

You can see that is the red colored, are on the oxide thicknesses as deliberately shown different thicknesses it does not matter. So, you have got back oxide, you have got a front oxide and I am showing a situation, where your applied voltage at front gate and the back gate is grounded, you can extent it to both gates.

So, biased. So, the keys gradually, front gate will be inverted. So, if I want to find out the sub threshold slope, see in this case n is grounded. It will be the front gate, it will be

conducting, that is the channel and if I chose a doping low and the thickness low small, it is the fully depilated case. So, then it is fully depilated, but is a gate and the ground, you can see there is a capacitance front oxide, then this capacitance between this point and this point silicon capacitance, which is actually absolvent silicon divide by t silicon and then in series, with that you have got this back oxide capacitance, thicker the back, oxide capacitance smaller will be capacitance. Now, what we pointed out in our previous slide is whichever channel, current here, observing from that point to ground point.

How much is the capacitance present, you can see that is a channel, where the surface potentially psi s psi s f. So, if I want to find out that n, I must have delta VGS by delta psi s f, that you can get from this equivalent circuit, front gate silicon, back gate all three capacitance series. So, from this point, from the front channel to ground, the total capacitance is a series combination of C s and C ox b particularly, if the C ox b is thicker, this capacitance get smaller and this capacitance C effective. What we are showing here, that is shown here as C effective. So, between the channel and this sub ground you have got one effective capacitance, which is actually C ox into C ox b by this series combination. So, if C ox b is small this is going to be small, smaller than what you get in the usual MOSFET.

So, the sub threshold slope n factor is 1 plus C effective as C ox f, sub threshold swing is k t by q log (Refer Time: 05:51) 10 that is 60 millivolts into 1 plus this quantity that is n factor. Now, you can have this C effective, very small compare to C ox f, particularly, when the C ox series front gate of very thin. So, you can get sub threshold swing very close to y V T lon 10 that is 60 millivolts. So, n is much closer to 1 in fully depleted, F D fully depleted SOI than partially depleted, that is partially depleted or even bulk MOSFET. So, you will get less than that and bulk MOSFET also less than bulk MOSFET thicker back oxide helps in reducing the sub threshold swing, but you may not have all the time thick oxide, but use it as double gate MOSFETs. You will see how it works out then the coupling between the gate and the source will be excellent and you will get 60 millivolts per decade.

And you go to double gate MOSFET operation and when this whole thing is depleted, will see how it comes up under, but otherwise what you have to understand is, and the whole thing is depleted whatever gate voltage you change beyond that point. it goes deviation junction we have discussed that. So, once this layer is depleted extra voltage

that apply here between the two of them that goes into the junction. So, delta VGS is equal to delta psi f s; that is the ideal factor will be equal to 1, this factor n will be equal to 1. So, you get 60 millivolts in double gate MOSFET ok.

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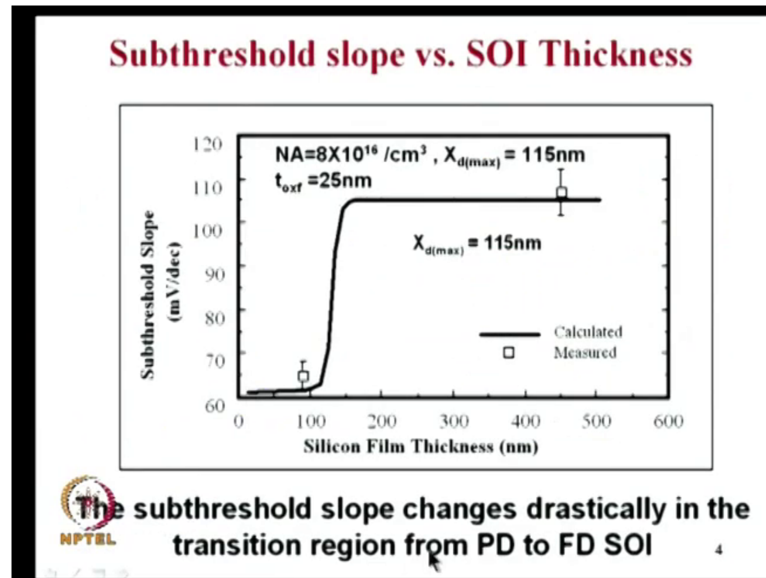

Now, this is just some of the result which I have even appeared in text book like college book. So, sub threshold slope or sub thresholds, swing both terms are used. Actually, it is inverse slope, because we are finding out that, we are finding out delta i d by delta VGS, but we use what we understand is for one decade, current change, how much is the voltage change ok.

So, you can see sub threshold swing or slope, when the SOI layer is thick. If the doping is 8 into 10 to the power of 16, then twice psi f e are there on the front gate. Depletion layer width is 115 microns. So, if your gate SOI thickness is thick, 200 microns or here, 400 microns, 450 microns. It is partially depleted. Depletion layer width is actually 115 micron, nano meter and SOI layer thickness is 450 nano meters. So, it is not fully depleted. So, in that case the C effective C D which corresponds to that thickness. Now, if you reduce the thickness to about 100 nano meters SOI layer, if this is 400 nano meters, it does not deplete by the time. It has gone to 115 nano meter. Depletion get, does not widen, but if this is 100 nano meter, it is fully depleted.

So, you will have the capacitance will be series combination of these three and you will get the sub threshold swing, very small, very close to 60 millivolts per decade. In fact,

this number is about 63 millivolts; you can never get 1, because you can never get this factor equal to 1 unless, you go to double gate operation. So, you have 63 millivolts per decade. So, what we are telling is, if you are for a given doping, if I keep on reducing the thickness, your sub threshold slope is fall, and we also saw that threshold voltage is also be smaller for a fully depleted case, as compare to that. Now, these two cases you would see, the i d verses gate voltage.

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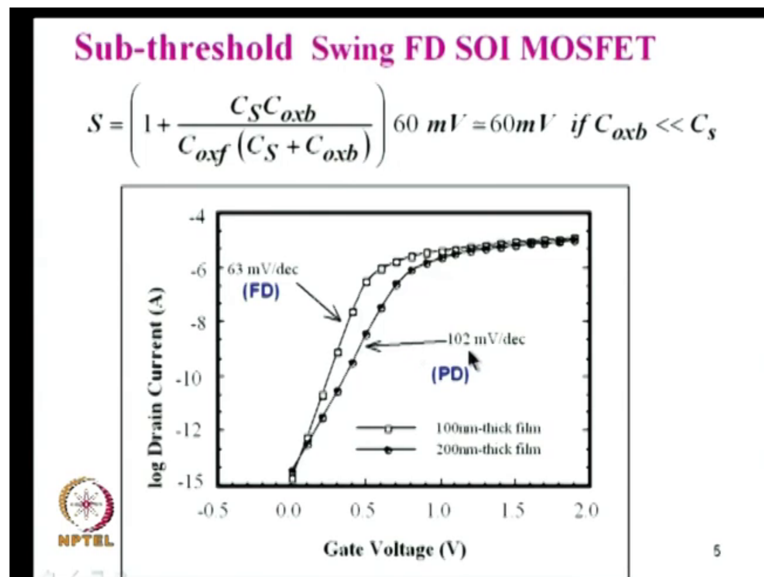

This is above threshold voltage, partiality depleted case that is 200 nano meter thick film, you have sub threshold swing of 102 millivolts, what we saw here in this region.

And you made it very thin 100 nano meters, this case fully depleted. You have got C; effective is C silicon in series, with the back oxide, which is very thick.

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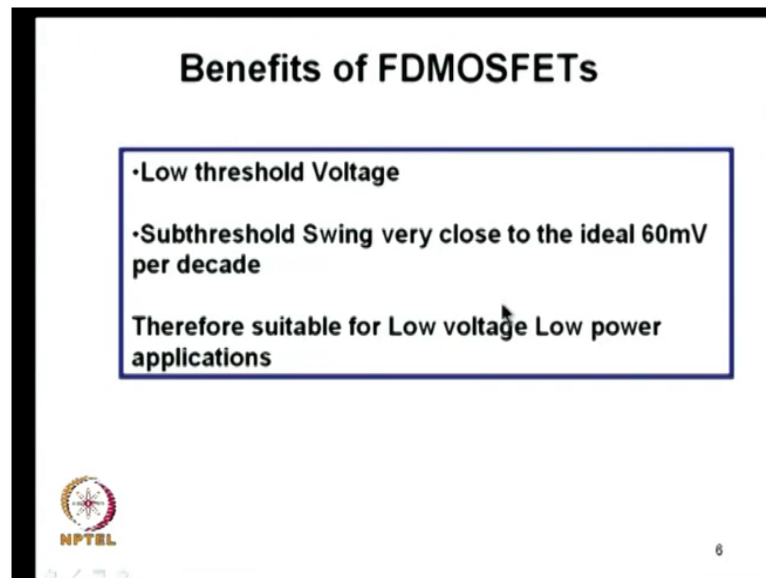

So, you get that now, very close 63 millivolts, per decade you get. So, benefits of fully depleted MOSFETs SOI MOSFET, low threshold voltage ,we have saw, we have seen already, last lecture sub threshold swing is very close to the ideal 50 millivolts per decade. What is the benefit of that? If you take here. Here, the threshold voltage is lower, if the threshold voltage lower, it enables you go to lower supply voltages, and if the threshold voltage is lower and sub threshold swing is ideal to 60 millivolts per decade, it can quickly bettered off.

So, that is why you can use the SOI MOSFET very effectively, for low voltages, low supply voltages, and that means, low voltage and low power applications. So, mostly you will see the application of this, is for low power, low voltage devices, and also, there is no large (Refer Time: 11:56) for that already.

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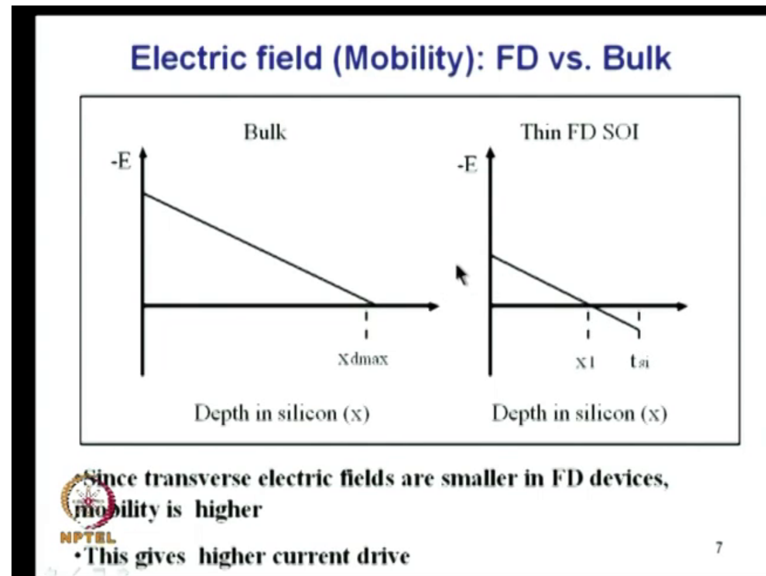

Now, this is just reminding you that, in the bulk MOSFET depletion layer, width is wide. This is a, in silicon peak. Electric field is larger, because of that wider deflationary width and that is why F D field is like that. This is belonging to back channel. This is a front channel.

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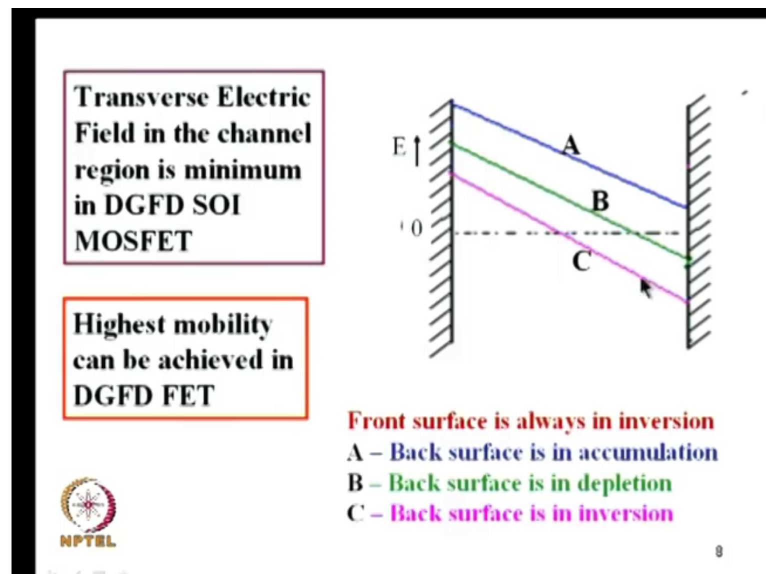

I will take field is smaller, all that you have seen already, to reemphasize that to, for that you recall the diagram accumulation, back gate depleted, both inverted lower and lower field.

So, when you have this particular situation, you can see that the field in this direction, transfers direction to this channel, go back to that, I will show you what we have telling, is the field in that direction from the gate towards the channel, that is what we are plotting here, that is small when a volt go to double gate operation, when both are inverted, if the field is small.

Now, you know that there is a transverse, field is small and the doping, I am sorry, the mobility will be high, if the field is higher, here, in this case, accumulation case, field is high and bulk MOSFET field is high, transverse field is high, because of high doping case and as a result the mobility of the carriers will be reduced, because of the transverse field. In this case you can use very lightly doped surface and therefore, the doping effect is reduced on mobility and double gate, when you use the transverse field is reduced. Therefore, effect of transverse field also, is reduced.

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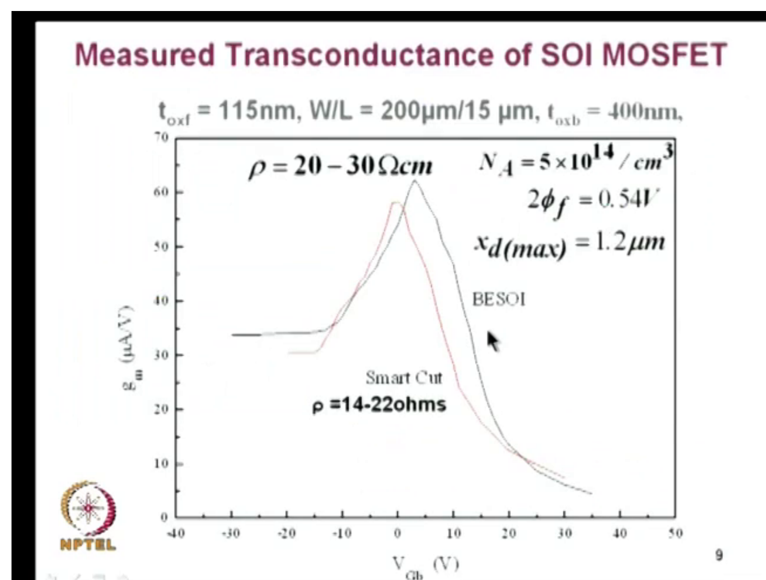

So, you can get x, best mobility is using, this type of device, this is one of those results which have been reported by some of our students when they made the MOSFET, where here, this was SOI MOSFET, the doping of 10 to power of 14 into 5 per centimeter cube transverse is 0.54 volts x d maximum is 1.2 micrometers, but your t silicon is, t silicon is much smaller than that. In fact, what you have got here is something like, let me see where it there, it is just about 4 400 nano meters or of the total. Let me see is there t ox b W by L is there t ox front gate is 1 1 5 nano meter, back gate is 400 nano meter and we

are chosen at is taken about 87 nano meters, much smaller compare to this 1.2 micro meters.

So, that is the thickness of that. So, it is a fully depleted layer. Now, what we are showing is that transconductance delta i d by delta V G, which would also correspond to the current as i increase that back gate, these are, there are two curves, the red one corresponding to one of them, corresponding to smart cut, SOI wafer made by smart cut, we wanted. See whether it makes any difference, if your smart cut or BESOI. So, the black one is the BESOI wafer practically, not much difference by the use, the same thickness. So, I bias the back channel in to accumulation by the back gate is minus accumulation. Front gate is actually inverted only one gate is conducting. In fact, threshold voltage will be high in those cases, and you will get the current due to one channel and as you increase the back gate to voltage 1 to negative to more and more positive side or being it to 0 back channel come to depletion.

Your current increases your fields decrease threshold voltage, decreases your current decreases. Now, when you go to a particular bias 0 voltage; here, we do not have to go to the details, what you are doing is back channel accumulation, back channel depleted, back channel inverted, in all the cases. Front channel is inverted in this portion, you are talking of front channel, inverted back channel taken from accumulation depletion and inverted. So, your current keep on increasing, that I showed you, some curve where the transverse characteristic shown. So, that is derived to go back to the previous lecture. You will see those graphs, what we are trying to point out is, the current is maximize both the channels are inverted. Now, from here onwards you have a situation, where you increase the back channel to plus. So, that back channel is inverted and front channel is going from inversion to depletion and accumulation.

So, best results you get best transconductance and best current you get when the both, the channels are inverted, that is what I am trying to show from here. So, this is showing that there is not much difference between BESOI and SOI, there is a transconductance that the maximum transconductance that we get in each device operation. Now, from the transconductance, you extract the mobility, you get this maximum current, maximum transconductance, because for the best mobility that you get.

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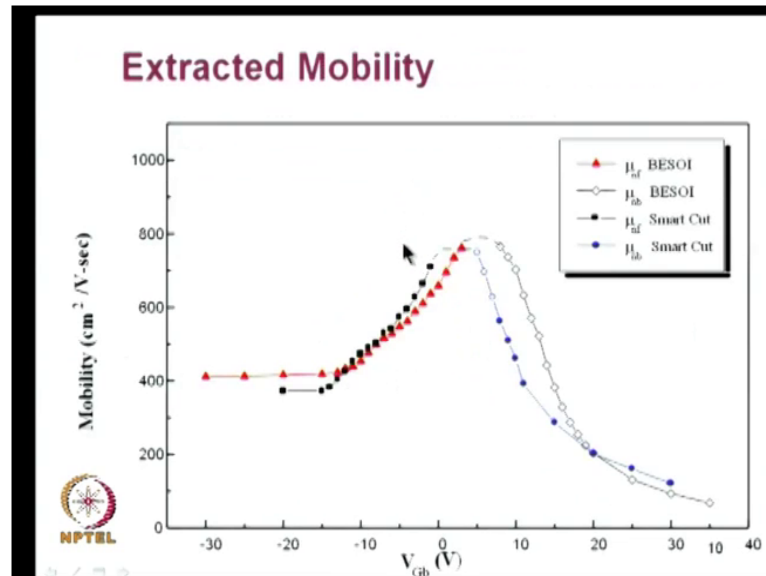

So, this is a situation where the both channels are inverted as I pointed out, when the both channels are inverted, the fields are small transverse field mobilities are best. So, you get best mobility when, the both channels are inverted these just as a information, I have just put it across you. So, at these are real and may be the location of best mobility point may have shifted. So, one device to other device.

Now, this is, the red is the mu n of the front channel, for the BESOI wafer and this is the mu n of the back channel. Here, this is mobility of both the channels combined effect, because in this portion we are seeing the front channel, inverted in this portion, we are seeing back channel inverted, because that channel voltage is very large. There is a good coupling is there, when you do that the front channel goes to accumulation depletion and accumulation.

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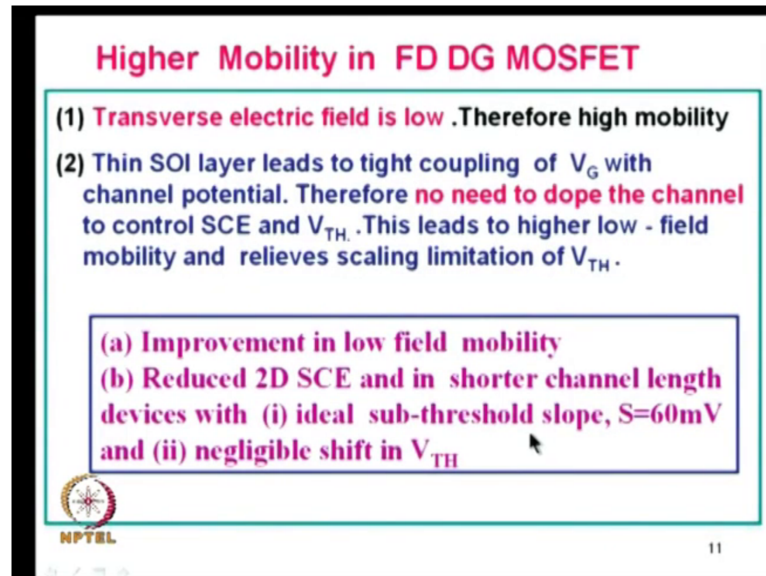

Now, through some of whatever, we have said, now fully depleted, double gate MOSFET transverse electric field is low to reiterate. Therefore, high mobility, high transconductance, the both channels are inverted, one more thing that you have, we will have to realize is that the. So, what we say from here is you can use double gate in the sense both gates, when connect together.

And have both channels inverted simultaneously, that should give the best mobility, because the fields are small in that case, we saw it already in our previous discussion. So, thin oxide, thin SOI layer leads to tight coupling.

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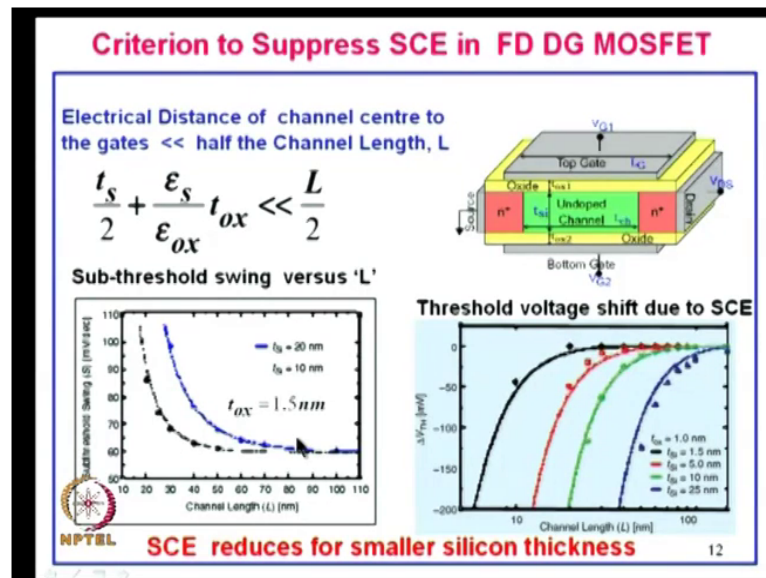

If you see, I am sorry, if I put a double gate MOSFET like this, I do not know whether you are able to see that, you see the SOI layer. This is the source channel drain front oxide yellow, back oxide yellow. These two slabs show you the gate, the three dimensional picture. So, I can, you connect both of them, such that both channels are inverted. Now, you can see, when we will get the short channel effects, we have to imagine or we know that this short channel effects coming to picture, when the drain begins to effect the potential nearer source end.

But if the gate distance between the gate, two gates, the electrical distance between the two gates is much smaller than this channel length. The drain has less control on the channel and nearer source region. So, some of the authors like Meindl, who are in transfer at the time, they gave this type of analytical guideline you will have. We will not have short channel effect, if the half, the channel length that is from drain to the middle, that is half the channel length, is greater than this electrical distance half. See when you have two gates, you can say that this half is of controlled by that, this half is control by the bottom one. So, what you see is look at the center from the center to the top electrode. What is a electrical distance? So, that electrical distance is t silicon by 2 t oxide be multiplied by epsilon s by epsilon oxide to get, because of the permittivity difference equivalent to the silicon. So, 3 times t oxide t silicon by 2, if these are silicon of that particular thickness, it is three times t oxide. So, that is the equivalent.

So, you can see, if the channel length is 20. If the t silicon is 20 nano meters, what we are telling is, 20 by 2 10 and if t oxide is 1.5 nano meters, what is epsilon s by epsilon oxide 3-3 times 1.5 that is 4.5, 4.5 plus 10 that is 14.5, L must be more than twice that, that is about 30 nano meters, if L is much larger than 13 nano meter, you will not afford channel effect, and when may have telling that, short channel effects are not there is sub threshold swing is 60 nano meters. So, you can see for 20 nano meter. This is the numerical solution using a software called Medici. They have done, they saw that sub threshold slope is up to about 40, it is somewhere below 70 and it is below 60 nanometer, 60 millivolts up to 60. What we are telling is, it will be more than about 30 nano meters.

I would say that you must put this as L by 4. So, if you have a a 40 nano meters channel length, for this condition you will have sub threshold swing of more than 60 about, may be about 70, but in bulk MOSFET, you will have about 100 millivolts per decade. It is much better than that, but if I reduce the thickness of the SOI layer 10 nano meters, that is reduced. You can see that you can go even right up to about 30 nano meters or 40 nano meters very comfortably, 60 millivolts per decade. You can easily go to 30 nano meter; still it will be about 65 millivolts per decade. So, if you want to go even to get down to shorter channel length, what should you do, reduce the thickness of the SOI layer, once further go to 5 nano meters, you can go even down.

So, the analysis source ultimately that you can go even down to about 16 nano meter channel length, without seeing this short channel effect, what is other short channel effect seen; one is the sub threshold swing increasing that you can go down right up to what I said is about 20 or 15. If you reduce the thickness below 10 nano meter thickness of SOI layer and oxide layer thickness one nano meter, if you are not able to go with one nano meter, change it with high (Refer Time:24:44) electric. Now, this is the delta with threshold voltage is about 0.5 millivolts 0.5 volts or 0.4 volts. How much is the shift and threshold voltage, if a, reduce a channel length, this is simulation. It closely matches this, but it is not very, we would have this much smaller than l.

So, you can see, if t oxide is 1 nano meter, then you will not see the shift length threshold voltage till it is about 20 nano maters close to about 20 nano meter. You go below channel length, if you go below 20 nano meters, you will get the thing. So, silicon thickness is 5 nano meter, t oxide is 1 nano meter, you can operate it very comfortably up to about 20 nano meter, without seeing a short channel effect, which is very hard on bulk

MOSFET, because then your sub threshold swing, everything will get effected, because doping a side. Here, you can go to very lightly rope material. So, this is a situation, advantages is very clear.

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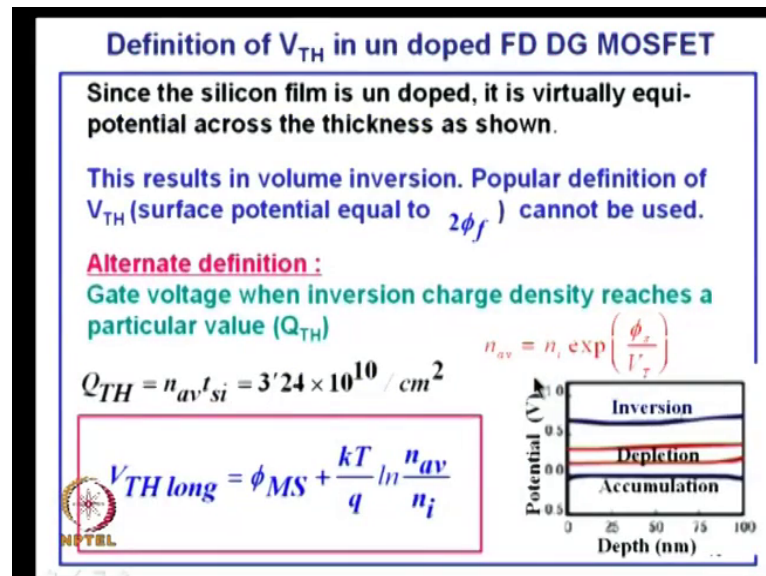

Now, one more thing, point that you want to see, is you can use very lighted out case fully depleted, undo practically, what will be threshold voltage. So, usually we define the threshold voltage as the gate voltage, at which 2 phi f is surface potential, but when you go to fully depleted case, it will not be 2 phi f and if it is undoped, there is no meaning in 2 phi f phi f is 0.

So, what they have said is you look at the charge in the channel. These are the potentials inversion that is the potential in which the undoped case, what the potential not vary across the channel, there is no filed there, I mean this slightly vary. So, this ignore that, this emerged on accumulation, it will be close to 0 depletion that will be plus, and, but what we are trying to point out, is you assume, certain charge for example, if I say the total charge per square centimeter, looking at the top from the gate is 3.2 into 10 to power of 10 per centimeter square. What does it mean? N average into t silicon, it is actually number, it is not charge, it is number average. In fact, there is a potentially constant, there charge will be constant over the entire width. So, this total charge effect is that, is what Meindl have shown. You can assume this and say, when this charge is

reached in the channel; that is the threshold voltage, but strictly speaking that will not be the case.

So, it will amount to an average, is equal to n i to the power of this. This is a relation between the potential and the average carrier concentration. So, for intrinsic case potentially, it is related to charge by this relationship background, doping multiplied by exponential, constant potentially phi s by V t. So, that phi s is given by this equation. See n average by n i into logarithm of that into k T by q gives you phi of s. So, what we are telling is, you find out the phi of s, that which the carrier concentration is reaching that value, it is approximate, but if you strictly want to see, what you have to do; would be you have to? I hope, I remember this thing.

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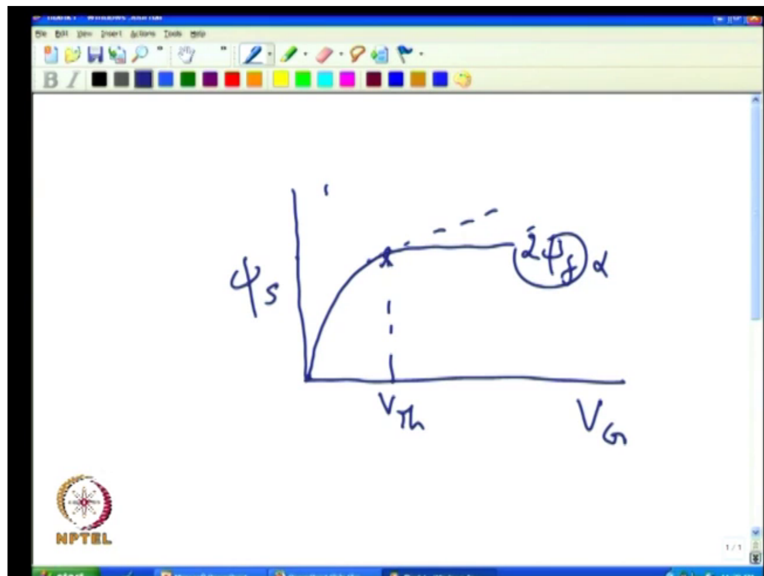

You have to go into a plot, where the V G verses phi, phi surface. In fact, phi surface should be almost same everywhere; that means, carrier concentration will be same everywhere, that you consult it as volume inversable, entire a volume of silicon is inverted.

So, if you start V G at 0 potential surface, potential is 0. It is shared between the oxide and this and the junction as keep on increasing, goes like that. So, you define this voltage V G as a threshold voltage. In fact, in the bulk MOSFET, this is the actually equal to 2 phi f to plot in a bulk MOSFET. Here, use twice phi f as the threshold voltage condition

by seeing that, when a keep on increasing that. In fact, 2 phi does not flatten out, it goes like this double MOSFET, slight increases.

Where it decades from this portion, you will take that thing, but in the case of a same MOSFET, it almost goes to that point, it will not, this will not, 2 phi f point. You take the phi s at which it is search rates, it will not be 2 phi f, it is different. So, as you do not know, what 2 phi f is, when the end out case, there is no 2 phi f, still you use this condition for that, because beyond that, what point, whatever voltage apply, go through the gate oxide and the entire thing is use for inverting the channel.

So, this is the point at which inversion take place that is the correct definition. In fact, we have nor for students, here at, worked on the thing to define the threshold voltage and a detailed paper has been written on that which as just, it is hot from the oven, just yesterday, we got the information that paper is accepted for a full paper in the general of applied phase, phase a.

So, that is that condition, there is lot of details involved in that, by the way it appears, you can just see that thing. So, you can see that there is a difference in defined threshold voltage. Now, there is one very interesting result with, people have observed some of the authors like Cristoloveanu, whose paper I will give at the end of the this lecture.

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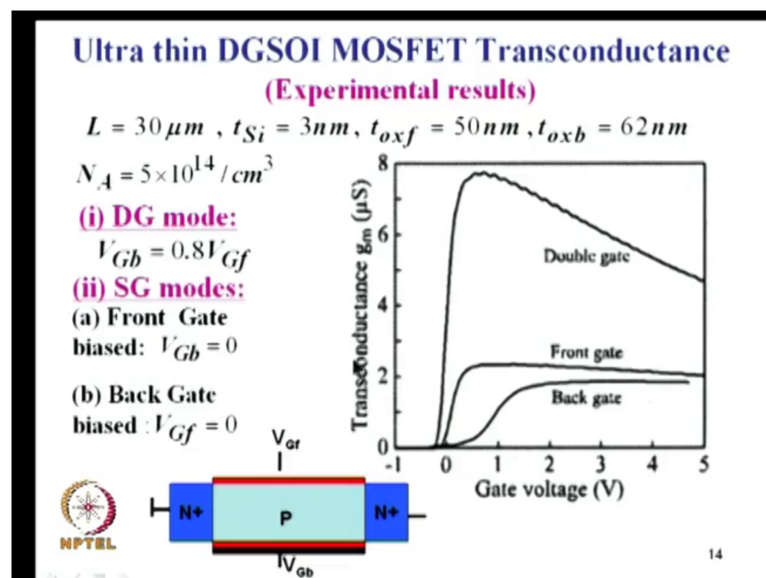

There is a reference which have given, you can see that source train. This is the channel, which you briefly depleted, and when you deplete fully, I can operate it as a single gate. How do I operate it as a single gate? Single gate mode V G p connected 0, apply voltage to the gate, till the surface front channel. Channel is inverted back; channel will be in depletion, because it is grounded. So, when you have that situation front gate inverted and back gate grounded, single gate mode, when you operate, they get some transconductance like this, keep on increasing voltage. You know V G minus threshold keeps on increases and there is a maximum transconductance, reaches. We have discussed in, when you discuss the MOSFET theory. So, transconductance reaches maximum, that is about 2, microsiemens, is the value for single gate operation, this is related to current delta d by delta V G.

So, that is a value now, instead of operating with the front gate, I operated at the back gate, these at as practical result, that they observed back gate. How do you do that single gate mode? Front gate is grounded, applied volt to a gate with respect back gate with respect source V G f 0, you get this sort of characteristic, you know the maximum task and it is almost matching, there is slight difference, because there is slight difference in the gate, oxide thicknesses 1 is 50 nano meter, other is 62 nano meter.

Now, when you operate, it is as double gate, both gates by; such that there is inversion at the front and back together. What do you expect? You get current two be the sum of these two and transconductance will sum of this two, but what you get is much more than, that it is not sum of these two, much higher than that you know, if this is 2 plus 2 4.

You would have expected 4, you get about 8. This is a very interesting result. They have observed. So; that means, when you use it as a double gate, is not nearly the channel current doubles. It is much more than that, because the entire volume is conducting, not only entire volume is conducting, the charges are confined to this center of this channel, that portion is there will see that.

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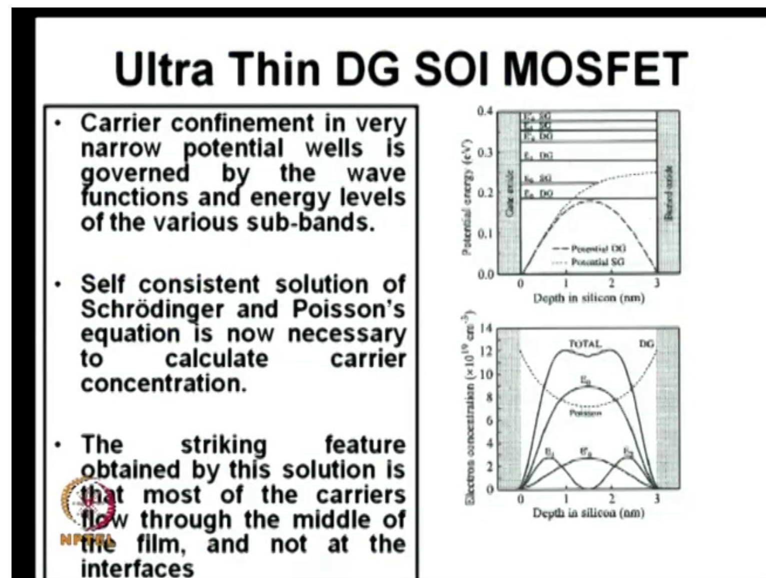

So, what is made out here is do not worry about all this number of lines, which are drawn. This is a front gate, this, the back gate oxide, this will explain this phenomena. Now, if the front gate is inverted, they potentially is plus. Here, going down to 0, usually you use to plot it from plus down like that, but now, we are putting this way. This energy bar diagram, this is equivalent energy bar diagram, ultra on energy plus. Here, minus here, potentially 0 there potentially plus. Here, there is we have; this is the double gate operation, single gate operation.

Now, you can see when we make it thinner, there will be condensation effects etcetera, there is, there will be fitting of an energy levels more than that. If you solve this Schrodinger equation and poisons equation together the, and estimate the carrier concentration, if I do not use a Schrodinger equation, if I do not take the quantum effect. This is the carrier distribution, because potential is maximum here, minimum here, maximum here, where it is potential, is maximum carrier concentration is maximum dotted line. Here, I hope you are able to see that maximum, minimum, maximum, that is the carrier distribution electron concentration, but your quantum theory tells you that, if there is a potential hill from here to there, where is a potential hill, you have the potentially corresponding to that.

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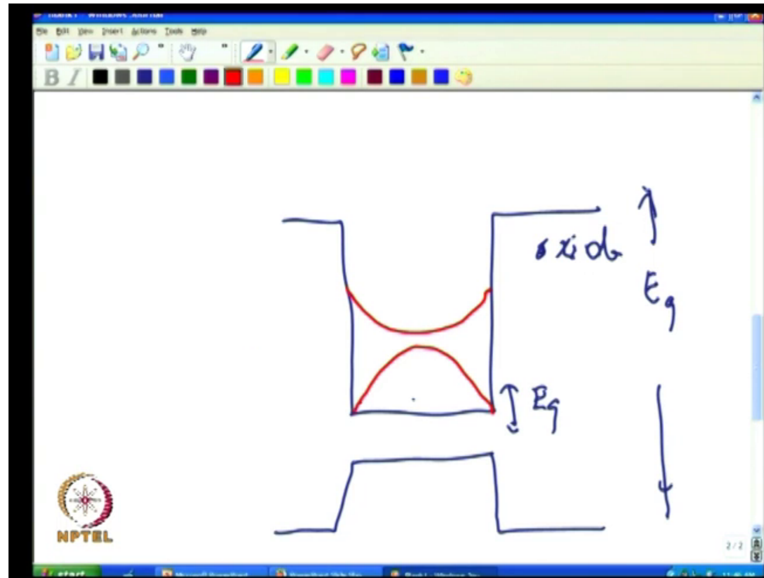

So, you have the, if I talk the channel, this is oxide. That is oxide band cap if you see, here, of course, here you have got the band cap like this. This is the conduction band of this is the E g of oxide, this is E g of silicon. So, you have got this is like a potential value. So, ultra oxide confine to this middle, because what is a probability of occupation at this point. If the potential hill is very high, I think I have just drawn that. There is a double end does not matter, if the potential hill is very high, the probability of occupation is 0, but this is a finitee potential, here to here. So, the probability of finding the electron, here, the probability of finding the electron, here, it low compare to probability (Refer Time:37:01) is low compare to probability of front gate here. So, ultras not be occupying it here. So, instead of ultra distribution being like, this instead of electron distribution, being like this. It will go, sorry like that, that is classical.

Now, what will be below here, it will go like that. So, electrons are confine to the middle of the channel. If the electrons are confined to the middle of the channel, what is the advantage; I shown is to a different scale, it may go beyond that these electron here, in the middle does not get scattered by the surface. This is a surface of silicon, they will not get scattered.

Therefore, the mobility at the center gets scattered, less mobility is better, because of that mobility is better, when it is like this, the current is much more than the current. When it is like this, see here, that is seen in the, that is what is shown here. So, the transfer here

now, the ultra other curves are all finding out for each wave function. This is electron distribution like that, it is a almost last here, here it is 0. So, electrons are confined here, I shown it in different scale, there in the previous diagram, what are drawn, this is electron distribution, this is a classical solution.

So, here electrons are getting more in that, nearer surface they get scattered, here most of the electrons are at the middle. They are not scattering, because of that you get the transconductance much better in the current double gate operation, much more than what, only one is conducting there.

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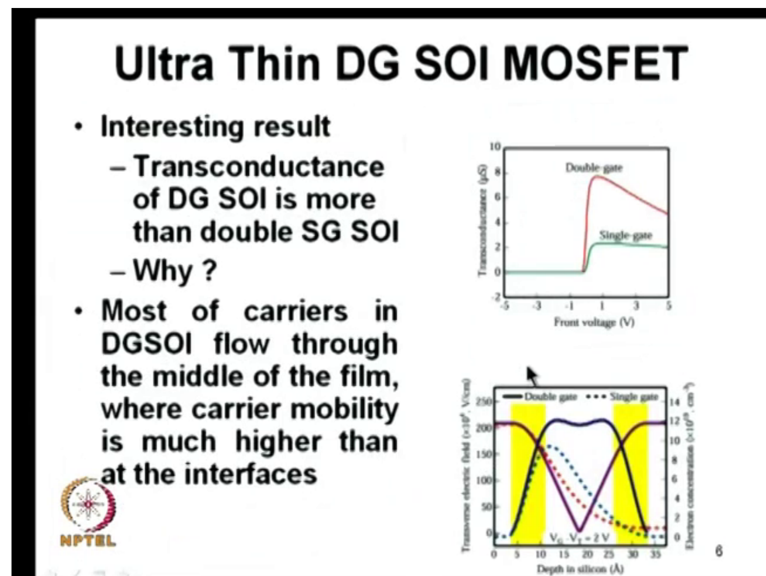

So, this is again reemphasizing the same thing, single gate, double gate and you have see the electric fields, here and this is the electron concentration here and electric field in the case of double gate, electric field in the case of single gate, there is reemphasizing that.

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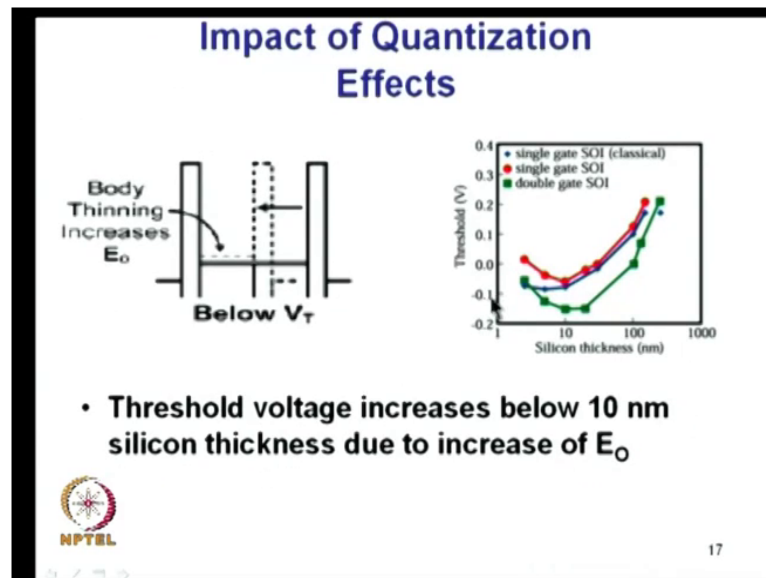

Now, let us see further, what we saw was if keep on reducing the channel thickness in the previous slide, we saw that the threshold voltage keeps on reducing. We saw in one of those slide that kept on reducing that, it came from doped, undoped and threshold voltage, come down low value. Now, when you go to smaller and smaller channel length like 10 nano meters and below threshold voltage begins to increase, it is not a good news,Because you want the threshold voltage to be low.

So, that you enable low voltage operation. Why that threshold voltage increasing? Threshold voltage increases, because I have shown this potentially layer, this is the oxide, this is the oxide and the silicon thickness is this much, you are the conduction bandage, will be like then or they energy level will be corresponding that all the energy level will get slipped it up. If a quantum well is actually like this and if you reduce it, all the energy levels even the ground level will shifted up, the energy level corresponding to smaller valve will be higher up. So, whatever energy level is there around e naught, the 0 level ground level, we will get shifted up, if the ground level is shifted up it requires more energy for electrons to be raise to the conduction band therefore, the threshold voltage goes up, because you have to have more energy; that means, more voltage must be upright to raise the electron to the higher level.

So, that is why, when you go to thicknesses like 10 nano meters or below threshold voltage, goes up. This is seen in single gate, single gate also SOI confinement, see here

there is a confinement. Here, whether it is oxide here. So, you get even in single gate you will get threshold voltage increases. We are concerned about this double gate MOSFET and as so SOI, where threshold voltage go down finally, increase because the quantum confinement effect. So, now, they are worked out some theory on that analyze it, using the contemn analysis, this delta e naught how much is the delta e naught is a measure of how much is the shift in threshold voltage.

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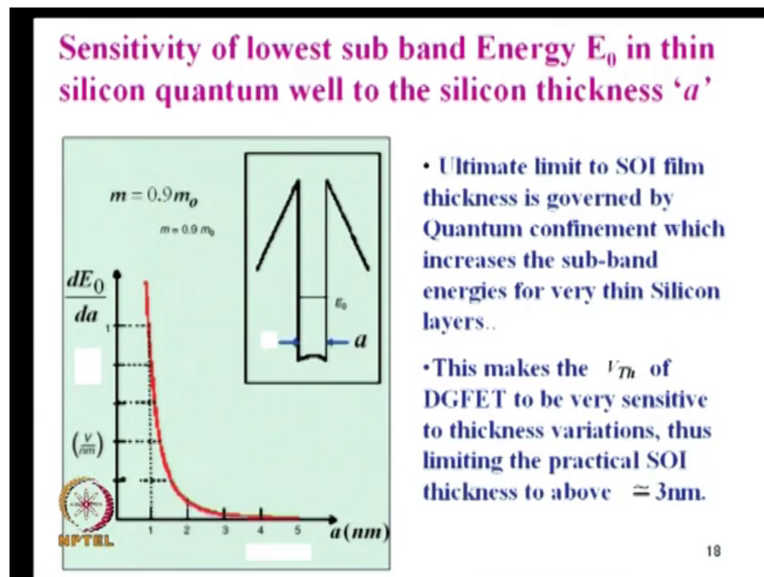

So, the delta E naught, what they have seen is up to 5 nano meters, not much change in delta E naught. It is there, but if I reduce this thickness, I have put it as a, it is t silicon, this is oxide pan gap, conduction band of oxide is here.

If I reduce this thickness keeping on, keep on reducing bring it below 4 3 2 etcetera below 3 nanometers, that energy level keeps on going up; that means, our threshold voltage keep on increasing by. So, many millivolts per nano meter, it will rise quite stiffly so. In fact, if you go to small value, it is may even go up several millivolts, I think this is millivolts actually. So, volts for nanometer reduction, here, if it is 3 nano meter, 2 nano meter will reduce, because of drastically, why should we worry about that, one thing is, we do not like that, to increase more than that can you make, see what you said is, keep on reducing the thickness threshold voltage keeps on falling that is good, but if you go to 3 nano meters etcetera, because of this effect threshold voltage will increase, you may not mind if it remains constant flat there.

But it increases, it is bad news from two points of view; one threshold voltage is high means your supply voltage must be high, second one you go to 3 nano meter thin SOI layer. You know how hard it is to get 3 nano meter uniformly over the entire wafer thickness 4, nano 4, micro 4 inch, width 100 millimeter or diameter SOI layer or if you want to talk of 8 inch across that entire wafer, it is very difficult to get uniformity of 3 nano meter. There may be 3 nano meter, 2.5 2.8, like that at least then you can see it goes up like that threshold voltage, goes up if there is 2 nano meter of you choose then it is, it effect 1 nano meter, you can see tremendous amount of changing threshold voltage. So, your entire your digital circuit will be all functioning there, analogue circuit, no hope. So, uniformity in the threshold voltage will be effected, if you go to thinner.

So, what we are telling is, we saw in the previous slide, here we saw, if you go to thinner and thinner silicon here, in this case this was giving 1.5 nano meter. The question is, we can go to very small channel length there, but the question is, whether can irrigate that sort of uniformity, one way of doing that fairly, uniformly is go to smart cur, smart cut. You implied the irons at exactly at the region, where you want clay width. So, you can get that thing, that value you can get, but it gone more different.

So, you can get go to shorter channel length, it will go to smaller thicknesses, but there is a limit up to which you can go to certain length, channel length. So, there is what I am trying to give the message, that do not think that you can go to 5 nano meter extra of this approach,.because then you are, thickness of silicon must be even going 1 nano meter, which is very difficult to get uniformity.

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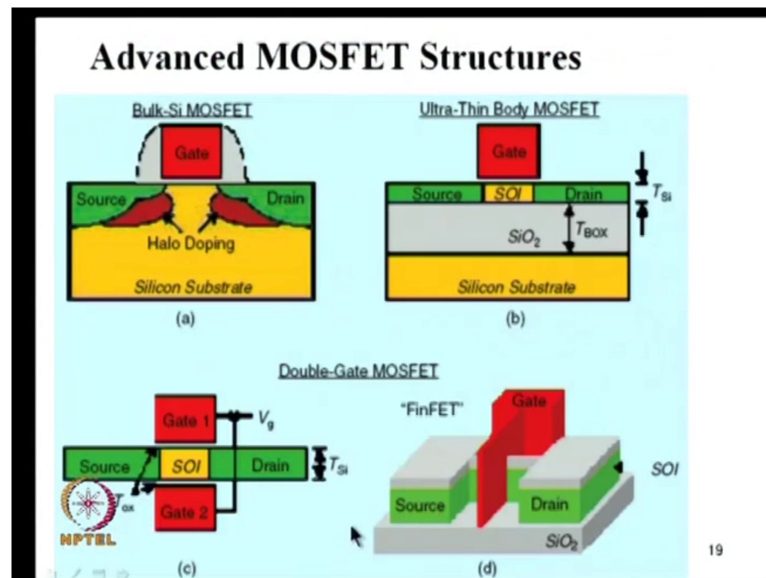

So, there are verities of SOI device. So, that you can get this is the bulk MOSFET, where you will chose, all this domain things are there say once, if you have to do you have to have trench isolation etcetera and this is the ultra thin body MOSFET, I can use single gate decrease from the top side itself, that is suitable for making, may be integrated circuit, but you can see the difficulty, there you have to go to this type of arrangement, here if I have like this, see the difficulty, you say, you can make ultra thin or double gate. Now, if I make a double gate like this, this is a SOI layer, I will have oxide everywhere, I must etch the gate from top.

And bottom like this, I will if not possible to realize integrated circuit, where this one wafer you got from one end to the other end, you got the wafer. Whole thing is connected to one, this is one gate here that entire thing will be one gate; that means, If etch on the front, you must etch from the back side. It is not a viable solution. So, the viable solution is go to this, that is a FinFET. In the FinFET, what you have is, I can show bigger diagram this is the one which you can integrate.

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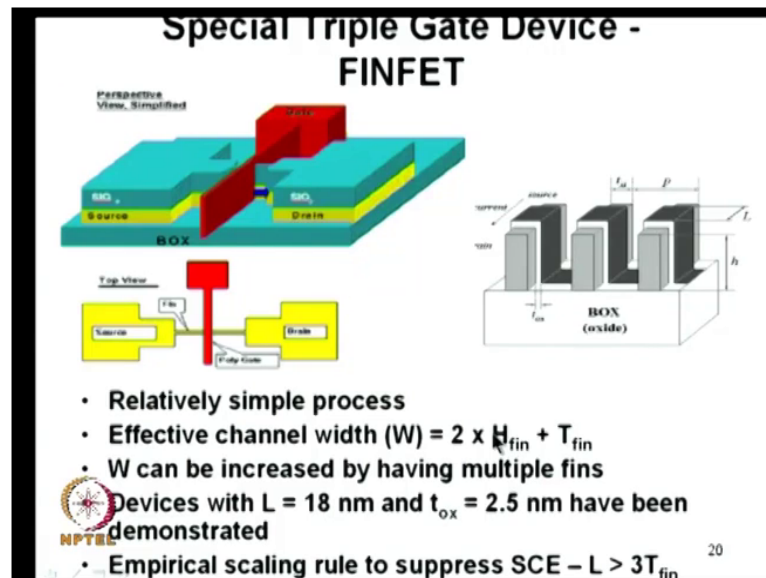

The FinFET you have the varied oxide below, that you have got the handle wafer, you have got this source region here below and you have got some oxide layer on the top of that, but the yellow is the source region n plus and you have that saved here and by lithography, you define this region the SOI is etched from reach, this region that is known by this. Here now, this is the region between the two, you make this pad big here.

So, that you can contact, get contact to this source and drain by lithography etching the oxide from this force and this layer is actually the fin, which again show it like this. So, if I take the go, from this is the, this portion is between this blue and this blue, a thin fin, there may be, can show it to you like this. If I have a fin like this like that there, I have the source here, I will have a source and this is the fin, I can make it very thin, see I can make it very thin, how can I make it, very thin by lithography. I can have 1 nano meter lithography right. On being lithography, I can do, I can make it very thin to your problem of thickness reduction is sorted out, here, by making that fin.

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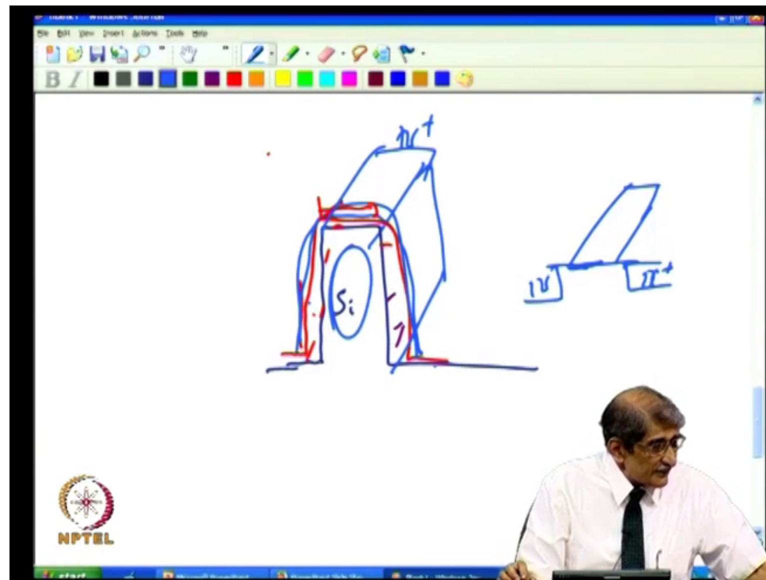

Here, it will be like that perpendicular, if I can, may be I do not know whether I can draw it separately here, see here what I have is fin, fin like this, that is a cross section, when I take, there you get it, like you see the silicon layer, SOI layer across that I have this oxide.

Now, this thickness, this show the SOI layer thickness of the SOI layer. I actually the, SOI layer and this is equivalent of that thickness of that SOI layer, which we are talking of front gate, back gate, there is a gate also, here all round, There is a gate, I think, I have to go all round, I got the gate here. So, we have got the metal oxide, semiconductor metal oxide semiconductor. If I take a cross section of the gate, let us just see that, but it is going perpendicular to this particular plane like that. So, my source is here. So, if we go to the diagram, you will see it clearly.

So, what are shown is this, the gate is going around that. So, you can see here from the source, should drain there is a thin, a thin layer here, perpendicular to that like that. So, it is like that. Now, surrounding that, you have get this gate, what is the w for this case, channel width, the channel width is, channel width will be this whole thing like the width channel length, is like that. This is going like this source is on here, n plus is here, n plus is on this side. So, your gate is going like this, usually you have the channel width like that. Going force is here and that is here and your oxide here, that is the, that is a w. Now, if this is, are like this source is here, drain is here and that is a w here. So, thickness

twice, the thickness of the SOI layer plus 30 width and this width it is equivalent of 2 gates on both sides comprising is.

So, electrons are confined to this force on completely. So, you get total volume inversion in this case. So, I hope that is clear. So, this is a gate red, is the gate metal which is surrounding this portion like this; now, I have shown here 1 fin going like this. There are more than 1 2 3 fins parallely between this source and this drain. See this figure shows only 1 fin, I have more than 1 fin, 1 2 3, if I have there, then you can have a, if I take the cross section here, if I had only 1 thin, I would have seen this, this is a fin, 1 fin, I would have, this is a gate going like that. The diagram which I have shown before, if I 1 2 3, you have got w is increased by that.

Because I think it is not clear, looks like just have time enough to go through that, what we are talking of is, we have got between the source and the drain point, here are small fin there.

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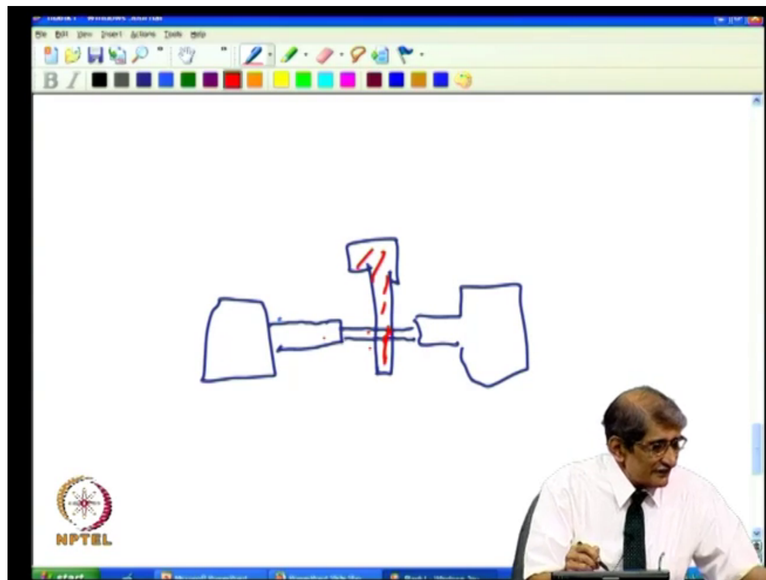

If I have sorry, I have, I will just remove that also I will go into that that is a point. Now, I have got this that is a one I got here, like this I have got, one fin like this, another fin like this, number of them. If I take a gate is like this. So, now, you can see that this gate, which I put as red, there crossing, this crossing that I take a cross section here, then I will see one here, one like that, this is what I am trying to show here. So, I take one number of them and you get more than one fin there.

So, if I only, 1 fin, w is corresponding to that, now is 1 2 3 fins are there, you can increase the current by putting more number, we call it a more number of channels in parallel.

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Summary

- FD SOI MOS devices have several inherent advantages over conventional bulk MOS devices like low V_{Th}, Ideal 'S', Improved low field Mobility and drive current mobility
- SOI wafers are also being increasingly used for other applications such as MEMS, radiation hard devices and high temperature electronics.
- Integration of FD SOI MOSFETs has been made possible with the invention of Fin FET

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So, that is the idea about that. In summary, what we have got is fully depleted MOS, devices have several inherent advantages over the conventional bulk MOSFET. Now, like low threshold voltage, ideal sub threshold swing improved low field mobility etcetera and SOI wafers are also being increasingly use for other applications, for example, MEMS, how can you use it; for MEMS micro electron mechanical system, I can realize a membrane, that can be done like this, I can use it for MEMS by, to realize a membrane.

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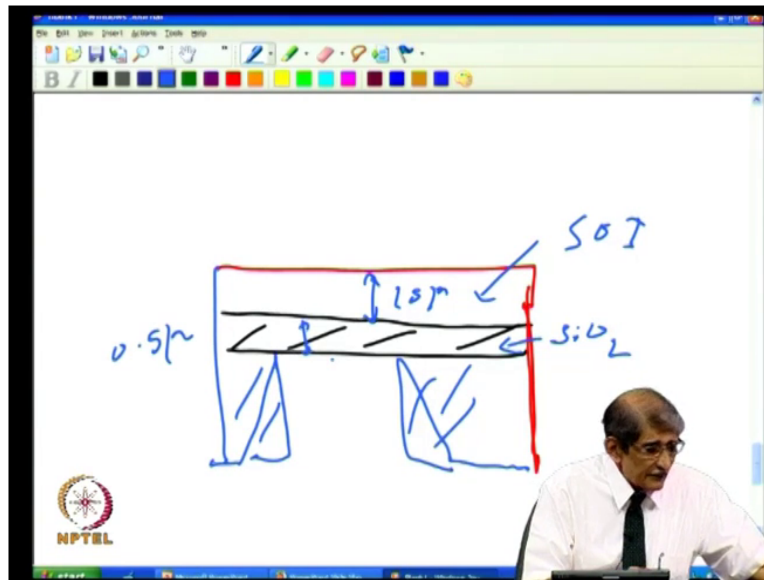

For example I can use an SOI layer, there is a SOI layer, there is a silicon and if I have a oxide here, that is SOI. I can etch silicon from back side.

By using, I think you can put this, I can etch it like this, either like this or vertically, vertical etch. If I use it, will go like that vertical, I can etch this is a S i O 2, I can etch, it means I, what will happen after etching; you will have this gone, my god. So, what you will have will be the; this will be like this. You will get it like that; I can etch the whole thing like this. So, the advantage is by time SOI layer is reached, etching stops k o etching, if you are using it, will not attacks silicon oxide. If I using d r i, you will get shape like this vertically tip react to etching, then you will have silicon here, it will stop etching. Here, what is the advantage; whatever silicon thickness is here, serves as a membrane, this will be very thin the 0.5 micron meters and this can be ten micron meters.

I think membrane created as a 10 micron, I can use it for Cintiq purposes, that is why I said, you can use it for MEMS, very lot more and more in our people are using this device for, using it for MEMS and for radiation hardened device also. They use it, because when you have a layer like that, whatever radiation impinges, it will cross it's layer and whatever electron (Refer Time: 58:33) generated will go to substrate, it will not generate carriers here. So, that is why relation hardened device is also used using that is why. Now, we also saw that, you can use integration, you can have number of derivative

devices isolated together, to make integration circuits C MOS, I can apply channel length, channel etcetera. You see this FinFET configuration.

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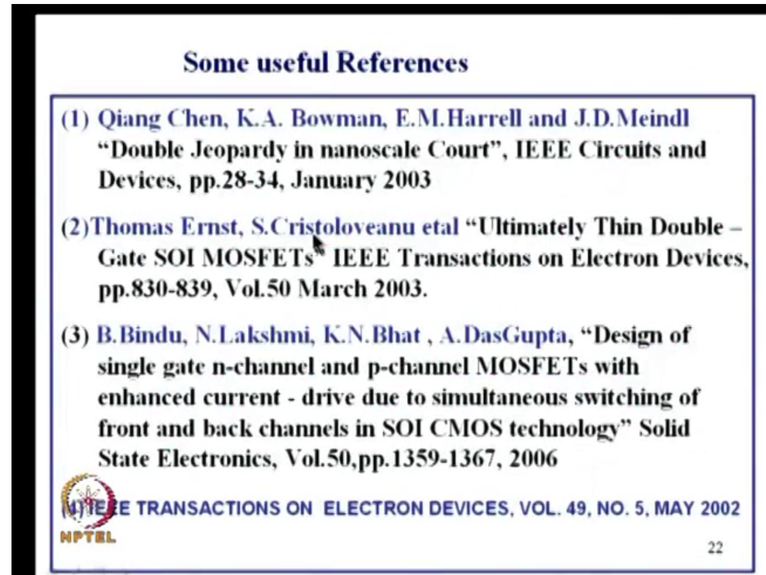

Now, there are number of wafers, which I have sited here, like which I have appeared over several years.

And I have just put here 2006, are the one that you know that, some of those figures which I had given, done by some of our students and myself and you can add to this one. Now, today onwards there is another general of applied physics, where the threshold definition is there. So, that I think, I will stop this SOI discussion. We will be going to the metal, metal source stage type of junctions, instead of this we will discuss that, in our next lecture. Ok then.