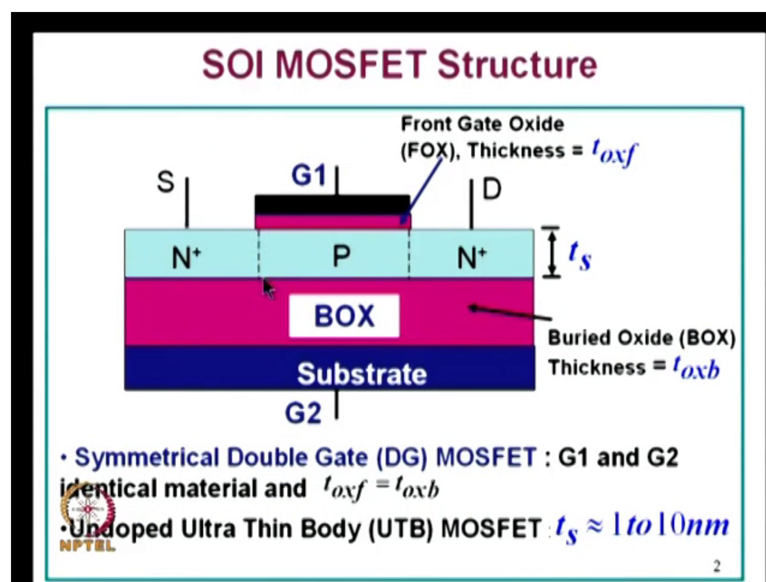
Nanoelectronics: Devices and Materials.
Prof. K. N. Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture – 20
SOI MOSFET structures, Partially Depleted (PD) and Fully Depleted (FD) SOIMOSFETs

So, we continue our discussion on SOI MOSFET that is silicon on insulator MOSFET, we have already discussed how to realize the SOI wafers, we have also discussed what are the merits of silicon SOI MOSFETs in as a discrete device or as a CMOS circuit. So, all that advantages you discussed last time, now we will see how this device functions differently or how if it different from the classical MOSFET.

(Refer Slide Time: 00:55).



So, this is the cross section of the SOI MOSFET, the top portion is actually the conventional structure.

Except that he has the gate only in this portion, junction only here. So, source channel drain and the gate oxide then the gate metal or doped silicon. In the case of SOI MOSFET you have got the buried oxide or back oxide. We can call it as the back oxide and the substrate on it is, we have this oxide is grown the device is fabricated; I have shown this thin here this have straight it in usually thick the whole the device there.

So, you can see that I just to see the terminologies you can use it as a dual gate, double gate front gate with the front gate oxide, thickness p oxide f it should t axial or t ox f back, back gate on the back oxide with the substrate act acting of a gate region and back oxide is or t ox b. Here I have shown it differently we will do the analysis for different thickness of oxide, but ultimately you want to have double gate MOSFET where, but symmetrical that sort of we will final the case of will be having on that it possible to in this lecture or subsequently.

Now, symmetrical double gate it is a d G double gated d G MOSFETs G 1, G 2 are identical materials and d ox f is equal to d ox b. Now, there are another class or devices you call these are double gate MOSFET, it can be symmetrical or a non symmetrical if they have put it is not symmetrical, now undoped. So, this layer channel layer region can be doped or even you will see that you can even have it undoped. So, undoped ultra thin body MOSFETs that is u t b MOSFETs will have t silicon that is the thickness of the silicon layer, t silicon which is 1 to 10 nanometer that is the ultimate ok.

(Refer Slide Time: 03:35).

Now, what we will see will be how to go about looking it analyzing this, how to understand the performance of this, you can have basically 2 types of SOI MOSFETs one is partially depleted SOI MOSFET other one is fully depleted SOI MOSFET. Lot of material on SOI MOSFET is available in a single book author by colinge, silicon on insulator technology materials to V L S I Kluwer publication, 1991 first addition 1997

second addition lot of basic materials are there what I discuss will cover some portions from there some portions on the papers with there with the appeared ok.

So, now let us see.

(Refer Slide Time: 04:32)

What is the partiality depleted fully depleted, do not be overwhelmed by this particular diagram, it is this portion see this is the same double gate what I have shown top gate front gate ox voltaging V G f we can apply back gate is substrate V G b you can apply. You know front gate oxide then between the front gate oxide and back gate oxide you have got this silicon, the whole thing is silicon you can ee the n plus layer is there source going from between the front gate oxide and back gate oxide similarly it ranges there.

Now, what we are talking consider now is the partially depleted MOSFET, means if we take the bulk MOSFET you have the only the front gate front gate oxide and the entire substrate, the substrate is depleted, how much is the depletion layer width depends upon a doping level. So, our threshold the depletion layer width is maximum, now we are considering a when we when we when we it will be partially depleted hopefully depleted, in the case of bulk MOSFET its always partially depleted only one channel. For example, if I cover this portion below this, this line that is actually the conventional MOSFET where when I apply sufficient voltage this channel will invert there we there we inversion.

Below the inversion layer there is a depletion layer and the depletion layer width depends upon the surface potential, when the front channel let us forget about back channel, when the front channel if you inverted the surface potential is twice phi f and that depends upon the dopy concentration. So, phi of in k T into logarithmic of N a by n i. So, higher the doping more will be phi f, to give an example when the doping is 10 to the power 16 phi f is 0.35 volts and that will give maximum depletion layer corresponding to that it is given by this relationship we have already discussed in details.

That I have calculated input it is about 0.3 microns I have broad this number if supposing the thickness of this SOI layer is on micron, when I apply gate voltage through the front gate when the front channel is inverted depletion layer width will be 0.3 microns per 10 to the power 16 doping. So, if this is one micro thickness the entire layer below that will not be depleted; that means, channel this whole thing is channel, d silicon it shifted down here t silicon is that thickness t silicon is only partially depleted on its inverted.

So, below this layer there not depletion layer, but now I use this back gate also to deplete from the back side and invert the back channel. So, what you have shown is this portion is x d maximum depleted to the front gate this portion is x d maximum depleted by the of back gate that is at x d maximum you had a, you have you will have a inversion layer here and inversion layer on the top, but now you can see there is no difference between the bulk MOSFET and this we have got one MOSFET on the top you have got another MOSFET on the back it is input in 2 MOSFETs in parallel.

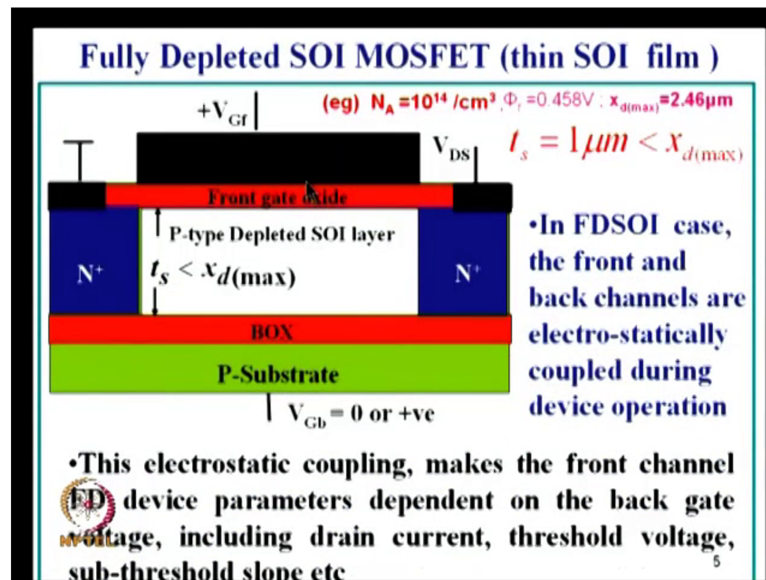
There is a no coupling between this region and this region, they are isolated that is partially depleted. So, in this example if the t silicon is total from this layer is one micron the top depletion layer will be 0.3 bottom depletion layer will be 0.3 and you will have 0.4 micron thickness un depleted. So, this is the partially depleted at the case. So, basic device equations for a partially deflation depleted there is p d SOI MOSFETs are same as that of bulk devices there is no difference. So, we do not have discussing the more.

So, this is not used very often except that you can still use it for radiation hard and devices it may not be you can have it few channels and the device is isolated from sub (Refer Time: 09:13) that sort of we can use, but these are a very popular device today for ics 2 inverted channels can exist in parallel, but this remember this numbers 10 to the

power 16 phi f is 0.35 depletion layer width maximum 0.3 microns. So, t silicon is one micron which is greater than twice the x d maximum.

So, it is the double gate operation. So, in that case when the double gate operation is there 50 silicon is more than twice the depletion layer width it is partially depleted, if it is a single gate that is there no back gate then t silicon should be greater than x d maximum then that is partially depleted the idea is clear.

(Refer Slide Time: 10:06)



Fully depleted device, it is has to removed then all these no material there is material is there, but there is a depleted layer to show there I have put this diagram like this here. So, you can see here front gate and back gate.

So, I have if I take, let if I take same one micron thickness of the SOI layer and if I use instead of 10 to power 16, 10 to power of 14 doping percent made a doped, p type doping then phi of corresponding to that is, phi of corresponding to that is 0.458, I am sorry that is twice phi f see that is remember phi f is equal to 0.35 and do doping is lower phi f will be smaller. So, what I have here is twice phi by f, here you have correct it, it is not phi f phi twice phi f phi f is divided by 2. So, twice phi f is 0.458 oh sorry.

So, corresponding twice phi f the depletion width is 2.46 (Refer Time: 11:30) because go back to that 1 twice phi f is lower, but n a is lower by 100 times twice phi f in the (Refer Time: 11:45) 3 cases 0.7 volts 10 to the 14 cases 0.45 volts not much different, but this

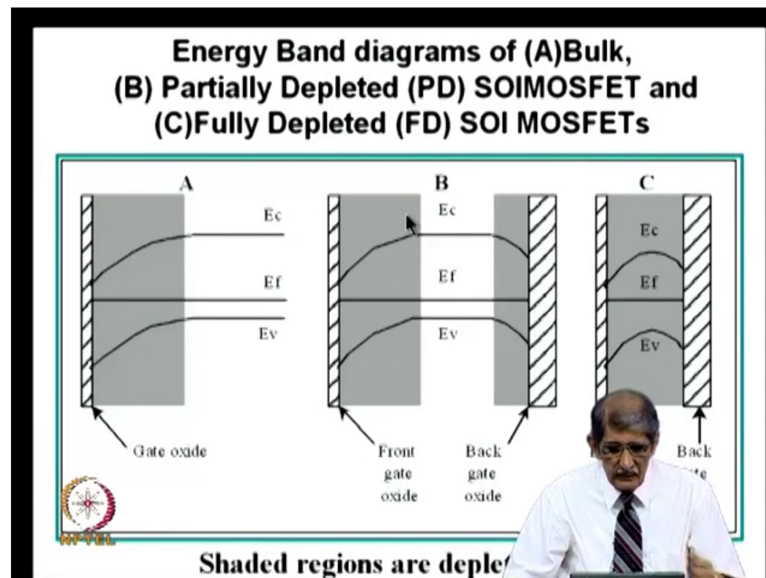
doping is reduced by factor of 100. So, depletion layer width will be more by factor about 10. So, you can see that x d maximum here is 2.46 micrometer if there is a thick as silicon layer bulk silicon depletion layer will be 2.46 as compare to, as compare to 0.3 micron is 10 to power x d case. So, now, what we say is if the thickness of the channel is 1 micron, the entire layer will be depleted it will go beyond that.

Even if this thickness have channel is 2.46 micrometer when the it is inverted the whole thing will be depleted. So, if the thickness is less than 2.46 micron it is definitely inverted both front and back channel can be inverted what happens in between we will see the so; that means, the case is different from that of bulk MOSFET. You have got the entire layer depleted you have got the front channel inverted back channel inverted. In fact, you will see that if you change the front channel potential it will change both front channel in potential and back channel potential in other words you will see that there is coupling with the front gate and back gate because there is no charge here.

Oxide depleted here oxide. So, whole thing is coupled if I change the voltage between the 2 the field between the 2 will change. So, that is a meaning of coupling will understand more about that later on, now let us go back to the 10 to the power 16 case. Can I make a fully depleted SOI MOSFET in 10 to the power of 16 doping x d maximum is 0.3 micron suppose here make this thickness of the SOI layer 0.1 micron is a fully depleted case. So, if I go to thinner and thinner layer I can use straightly higher doping.

Now, this is the idea of fully depleted and partial depleted and this operation of this is different from the bulk MOSFET whereas, partially depleted is same as the bulk MOSFET. So, we did not go into discussion of that will get down to discussion on the fully depleted SOI MOSFET let us take look at that.

(Refer Slide Time: 14:14)



This is a diagram which tells you the energy band diagram all of your familiar about energy band diagram, this is the bulk MOSFET, bulk MOSFET of side that that way gate oxide sub state.

So, all that is put like that. So, gate is there oxide shade it reaches in the oxide this is the depleted region, you can see the depleted region the band gap the energy band diagram when supports because the field is in that direction. So, you have got below the depletion layer there is no band bending, there is no band bending there is a voltage drop the entire voltage drop with the across this the depletion layer. So, this is the band diagram of the bulk MOSFET and if I draw the intrinsic level that will come from here like that intrinsic level will be below the Fermi level that will be inverted.

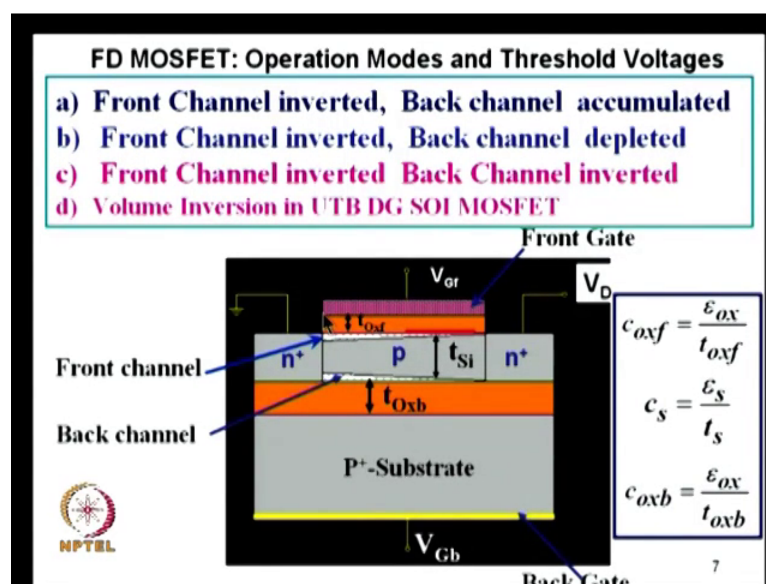
Now, let us take the partially depleted SOI MOSFET. So, this is the MOSFET now, it should like that I have put it like that front gate, front gate oxide silicon back gate oxide, back gate. So, you have got partially depleted this is the oxide this, this is the depletion layer. So, please remember wherever depletion layer width is there, wherever depletion layer is present the band bending take place plus to minus. Now, this is the region which is not depleted, go back they are coming from here to here depleted, no depletion, depleted from back side, depleted no depletion, depleted because now applied we will take plus here.

So, our field is in that direction here, here the field is in this direction the band diagram is like this, now let us say supposing this re portion is removed; that means, I have made the thickness equal to sum of this and this, this is removed. So, you put them together no depletion and the no undepleted portion fully depleted. So, this goes up like this, this goes up like this and the electric field here will be 0, see if you go here algebraic diagram is flat that typically 0 from 0 to 0 merge them together.

Up to this point the electric field is in that direction, belong through the front gate and from this side onwards from this back right side to the left hand side electric field is towards the left side. So, energy band diagram bends up, where they meet where they 2 depletion were meet here field is that direction, here the field is in that direction they are the 0 field is there and whereas, the 0 field is there the there is a potential minimum, comes from minimum increases of that way more about this we will 3 as you go further on this discussion.

So, this is energy band diagram of for fully depleted SOI MOSFET this will be inverted if this potential is twice phi f, this will be inverted back channel if that potential is twice phi f. Now, these also we are applying that voltage with refer to this source region, here after the analysis becomes different slightly, slightly different marginally, but you will have to be a careful and looking at the entire situation.

(Refer Slide Time: 18:16)



So, this is again the diagram of the soi MOSFET now these are shown this back oxide t oxide b thicker compare to the t ox f, not symmetrical, symmetrical case there will be equal and this is the t silicon t s we call it and the notation and this is the t oxide f (Refer Time: 18:45).

We are now talking of fully depleted MOSFET no more partially depleted. So, you can have in this case several type of operations, one you what have MOSFET operation there must be at least 1 channel inverted. So, that l trans in a n channel device l transfer created and you can transport it here like this. So, one case is front channel inverted and backchannel can be accumulated you can have the entire layer depleted, but still you can have you can how do we in accumulated the back channel apply negative voltage to the gate, if we take a mass cap p type substrate apply plus voltage to the gate you will deplete.

It keep on increase the plus voltage inverting suppose he apply negative voltage to the gate with respect substrate or the force plus charges will accumulate its accumulation. So, I can have accumulation layer here on the back channel by applying a large minus voltage to the gate back gate, but at the same time I can invert this front gate by applying plus voltage in the front gate you can see the flexibility that you get, that is one operation this is only more for academic understanding purpose in some cases the use it in some the special applications, otherwise its very rarely used, but you may come across such situation situations when the make use of it for integrating circuit sometimes.

Second case if front channel is inverted they apply a plus voltage large enough. So, that you can invert, how much is the voltage that that you must applied to the front, front gate to invert depends upon what is the condition on the back channel that also we will see. See the bulk MOSFET your threshold voltage it decide a must doping is fixed and oxide thickness is fixed, now here another parameter you can control the threshold voltage by it is a back gate you can do that also the bulk MOSFET I get (Refer Time: 20:53) change, but that will only increase the threshold voltage reverse by the input. If you can not apply plus voltage we want to the back gate because then there will be followed by if across the junction.

So, you can only increase the threshold voltage you can control the threshold voltage some extent marginally here there is a oxide, we can apply plus minus without hurting

this junction. So, if you apply minus here inversion, if I apply plus here depletion, front channel can be inverted with back channel depleted second case, third case is I apply a sufficient plus voltage to the front gate sufficient plus voltage to the back gate. So, that both channels are inverted. So, front channel inverted back channel inverted.

Now, you can see when you have both channel inverted you can draw a line at the center you can say half of the top portion of the silicon is and the depletion layer there belongs to front gate, it is now shared between a 2 both are inverted and half of the layer below this middle line here that is belonging to the back gate. So, whatever depletion layer charge if there belonging to front gate there or if t silicon the t s the t silicon total charge per centimeter square it is q n a into t s. So, q n a t s by 2 will belong to the top gate other charge will belong to per centimeter square with bound to back gate.

There is another class of devices which the which is a mores of litigated or another version of this third version that is volume inversion, ultra thin body u t b ultra thin body double gate SOI MOSFET. If I today we will talk of ultimately ultra thin body and in this analysis unlike in the bulk make MOSFET you will talk of t ox c oxide, t ox is capacitance percentage of square front gate oxide. Here he will have talk of front gate oxide c ox f which is epsilon oxide into epsilon 0 of course, divided by t ox f that is per centimeter square and you can also talk of c t silicon what is t silicon if the entire silicon layer is depleted the capacitance corresponding to that layer silicon layer, that is c silicon is epsilon silicon into epsilon 0 divided by d silicon, instead of oxide you have got that silicon permittivity silicon thickness you can talk of that.

That is when its fully depleted when it is fully depleted you are looking into try to the capacitor, when you go to sub threshold slope you will see that that capacitance come to into picture, that is why just brought in here back oxide capacitance c ox d. Now, when you go into the analysis of this a structure what we will do will be we will assume that this p plus p layer will p plus that is it (Refer Time: 24:18) dope. So, the whatever voltage we apply is available here to simplify it will modify it only marginally with a small top on the substrate if the doping is present there. So, when you go to double gates. In fact, the situation will be that will be heavily doped heavily doped.

So, we considered that case, to avoid more complication in other words you can say this is a metal here this is a metal there, there no drop here in the silicon. Now, let us take

look at how to what we are interested in this what are the operation modes and what are threshold voltages, once you know the threshold voltage you can use some MOSFET equation same equation you can use to describe the MOSFET current trans conductance. So, entire analysis is hovering around the threshold voltage, you can this is same equation we will see oxide w well (Refer Time: 25:24) with threshold whole square or w q into v v that is the ultimate equation, velocity into charge into w and q depends upon what is the threshold voltage is what is the gate voltage is.

(Refer Slide Time: 25:43)

Bulk Silicon MOS CAP Threshold voltage

At threshold voltage $V_G = V_{Tn}$. $V_G = V_{ox} + V_{Si}$

$V_{Si} = 2\phi_f$ $V_{ox} = \frac{Q_d}{C_{ox}} = \frac{qN_A x_{d(max)}}{C_{ox}}$ $x_d = x_{d(max)}$

$x_{d(max)} = \sqrt{\frac{2\varepsilon_s\varepsilon_o(2\phi_f)}{qN_A}}$ $\phi_f = \frac{kT}{q}\ln\frac{N_A}{n_i}$

Electric Field at the Si surface $E_S = \frac{qN_A x_{d(max)}}{\varepsilon_S}$

Continuity of electric flux: $\varepsilon_s E_S = \varepsilon_{ox} E_{ox}$

$\therefore V_{ox} = E_{ox} t_{ox} = \frac{\varepsilon_s E_S}{\varepsilon_{ox}} t_{ox} = \frac{\varepsilon_s E_S}{C_{ox}}$

$V_{Tn} = V_{ox} + V_{Si} = \frac{\varepsilon_s E_S}{C_{ox}} + 2\phi_f$

In general, we can determine the V_{ox} if we know the surface electric field E_S

So, now just before we go into that see you can see that this is bit more complicated structure then the other one, now t is when you apply a gate voltage in the bulk MOSFET what happens and how it will be. The bulk MOSFET I am going slow here because slightly different from the concepts there gate black oxide, depletion layer width when the plus plus voltage and of course, inversion is there. Now, here how did you recall, how did we find out the threshold voltage is at threshold voltage V G equal to V T n and V G gets shared between the oxide and the silicon and in silicon it shared between the it is part of the depletion layer.

So, at threshold voltage v silicon is twice phi f the drop. So, depletion layer corresponding to that is q depletion by I am sorry the oxide drop to make it very clear gate voltage is shared between the oxide and silicon and at threshold voltage what is the silicon drop phi by f that is very clear. Now, when twice phi of is the drop in silicon you

know how much is the depletion layer width from this formula, surface what it is twice phi f. So, depletion layer is this much, once you know what is depletion layer width you can find out what is the, what is the voltage drop across the oxide is that is this one.

Charge in the depletion layer width is q and a into x d maximum divided by that I divide this oxide if the voltage. So, what we did was p silicon is twice phi f corresponding to that x G maximum is see 1 there is formula corresponding that you know q d is that much per centimeter square; q d by c oxide is the voltage drop of the oxide. Taking a plaster charge on the other side of a capacity is q d minus q d q d basic oxide is voltage of x oxide; this is how we did the calculations. So, how did you arrive at that I am doing that because you may have multiple layers beyond this point.

If you have multiple layers beyond that point you may not be able to easily compute this here you know once is trap across the silicon is twice phi f you know depletion layer width you know charge the charge basic oxide is the voltage of across the oxide. Now, look at the other way what is the charge related to, how with the charge related to the field on the surface. If we apply gauss law through this surface top of the silicon surface you have apply gauss law it is part of the infinite surface. So, you apply Gaussian law to that portion per centimeter is part of that per centimeter square charge is q N A x d maximum.

Charge divided by epsilon s is field gauss law the field lines terminating on the surface is charge beyond the surface divided by epsilon s, epsilon r epsilon 0 that I have put to the epsilon s. So, you took that 1 centimeter square of the fear then you say the electric field that much. So, what we are telling is the q d by epsilon s is electric filed in silicon, now from the continuity of flux if you take I do not know whether you I have studied electro magnet field pretty much of studied or basic electro static.

If have interface here look at this I have oxide here, I have silicon here, electric field here and here will be different what is continuously the flux, del dot d into d of s is constant or the flux is epsilon s into epsilon. So, here epsilon is epsilon s is the field in silicon is c s and the epsilon s is the permittivity. So, epsilon s into e of s should be equal to epsilon oxide into e oxide that is the continuity of flux this is the d d is epsilon into e d in silicon is d in oxide oh I am sorry, d is silicon is d in oxide. So, now, you can see I am drawn the

electric field diagram here e oxide is higher than in e silicon, if I know e oxide I know voltage of across oxide, correct.

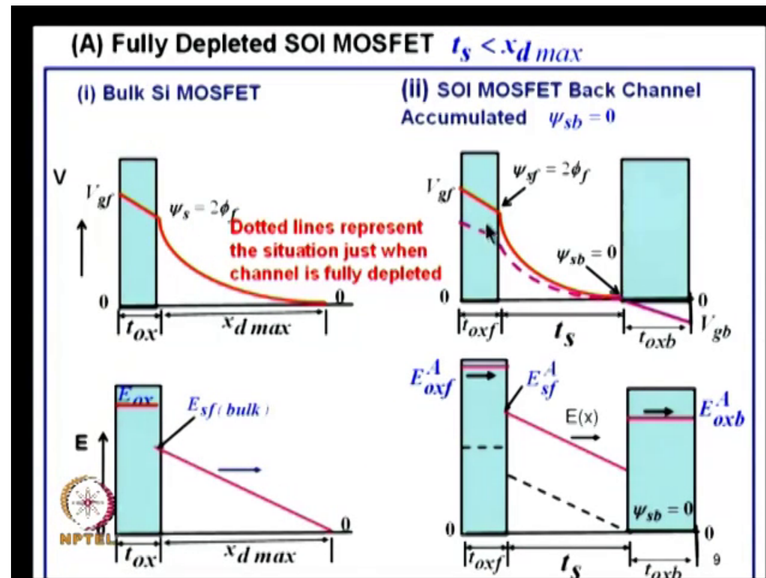
So, I am just trying to get this relationship slightly differently because you may not has that depletion layer width precisely, but you can find out if you can find out the 3 peak field on the surface you can find out the voltage of across the oxide because if you know the peak field e of s in silicon I know the oxide drop, oxide field from this relationship continuity of flux. Now, if I know the oxide draw field I know what is the voltage oxide is, it is exactly what I have derived that actually I am just recalling them. So, e oxide into t oxide will be the oxide drop, e oxide is from this relationship epsilon s e of s divided by e oxide is epsilon oxide is that. This is not flux in silicon divided by permeability in the oxide q is (Refer Time: 31:34) in the oxide electric flux, electric field. Flux product of the two if I divide by this I get the electric field in the oxide that into t oxide will the voltage drop. So, what is this quantity e of s into epsilon s here e of s is q d by epsilon s charge beyond that surface whatever charge is there divided by epsilon s the peak field. So, e of s into epsilon s was the charge here that is the charge.

So, same relationship you got differently, why I derived that is if you want to find the volt threshold voltage all that you have to do is what is the voltage across oxide when the surface potential is twice phi f. So, potential near the surface is twice phi f you can find the voltage drop across the oxide by knowing the field near the surface of silicon that is because epsilon s into e of s actually the charge beyond that point whatever is number of layers divided by c oxide will give the oxide. I think it is you when you go through this once more you will actually see. So, by doing this I have shown that what you write here is the same as this, if you are writing q d I wrote it as I showed that it is equal to q d is equal to whatever charge beyond that point let that be depletion error, epsilon s that is permittivity of the material layer silicon into the silicon field at the surface, that is what we get now here threshold volt is twice phi f plus this.

So, if you go to the same MOSFET all that you have to do is if you want to find voltage of this type of structure, all that I have to do is at threshold voltage of front gate I know that the potential here is twice phi f surface potential is twice phi f that is a condition for (Refer Time: 33:54) pi is twice phi f and if you can find out the field on the surface multiplied by permittivity divided by c oxide I get the oxide drop. That is all what we are doing it is as simple as that, we are trying to find out we are assuming twice phi f is the

potential there. So, gate voltage is twice phi with respect to ground. So, potential here with respect to ground is twice phi f, you want that only the gate oxide drop is there that is just epsilon s E of s divide by c oxide f I forget to say f assume that it is that oxide.

(Refer Slide Time: 34:36)



Now, let us take a look at its little bit more involved bits of this slope on this. So, this is the case of bulk MOSFET on the left hand side take a look at those figures now, this diagram I have drawn already in the previous page this is oxide that is the gate this is silicon, please note I am supporting all like this I put it like that, now gate oxide silicon bulk. So, in silicon because it is an informal dope matric field will always be linear, we have seen a number of times. So, this is the extreme maximum at inversion, we are considering threshold voltage.

So, we are considering a situation where there is inversion; that means, we are considering a situation where the surface potential that is potential at the surface silicone is twice phi f. I think the previous series of lectures you would have called it twice phi b if it is called sometimes it is called twice phi b I call it twice phi f both are same. So, you have the potential as surface electric field is linear and integral of that will give parabolic (Refer Time: 36:05). So, voltage of in silicon we take it like this parabolically and we are going back to basics and the potential is continues, in the silicon in the oxide there is voltage drop electric field is constant there are no charges if electric field is constant the potential integral of that linear.

So, you can see that voltage rises in the parabolic manner in silicon bulk MOSFET then it is linear, electric field rises linearly and it is constant there is no charge in between there is no charge here it is linear because as you go from here to here the charge keeps on increasing because depletion vary the charge from here to here is if you start 0 from here. I am sorry, it start 0 from here this end as you go the charge is going on increasing and voltage going down to you. So, let me without going to that linear becomes parabolic and constant becomes linear there and you see here e oxide is higher than the e silicon here because of the difference in the permittivity, over permittivity the factor of 3. So, this e oxide is 3 times this quantity E s f.

Now, let me now go to a bit more involved situation SOI MOSFET to the back channel accumulated, front gate oxide back gate oxide this colored portions are oxide this is the t silicon, what you are telling is you are talking of fully depleted case; that means, by the time it has inverted entire silicone area is depleted, but if I start with the back gate bias V g b negative see this diagram this full line here. So, the potential, when I apply voltage across this V g b back gate just go back to this I will show you, see here when you apply V g b we want to know with respect to what we are applying that we are applying with respect to this one point or some point somewhere in the silicon somewhere outside ok.

From potential neutral point with respect to that you are applying in the case of MOSFET also we are applying a voltage that is to gate to the source, source is connected to the substrate here also the similar thing situation you can have. So, when I apply voltage here negative with respect to that this will be accumulated, back gate is made negative with respect to ground; that means, this channel would be having plus charges, p becomes more p plus it is accumulated. Now, the potential here corresponding to that will be how much, in an accumulation layer see in a depleted layer because of depletion layer and band bending you get charges sufficiently you get region over its charges spread and the potential can be 0.1 volt 0.2 volt 0.3 volts or even 0.5 volts depletion layer drop ok.

For example when you take 10 to the power 16 doping you have got twice phi f is 0.7 volts; that means, voltage drop is 0.7 volts. Now, when we Inver when you have accumulation layer there you can accumulate charges with very small voltage surface potential. So, to volt potential of this region with respect to the substate will be very

small plus minus here plus there in other words you will have a charge sheet with very little dropping silicon.

So, the assumption here again would be that the it is a charge sheet with no drop across that charge sheet like what you do in the case of inversion you take the inversion layer you do not consider drop across that because charge is large. So, here you can say that plus charges are there which is actually decided how much voltage you applied and how much is the back gate thickness. So, you should take the back gate here you will have a field in that direction plus here minus here, but the voltage here will be 0 because we have a large plus charge is there that can come with very small voltage ac, voltage across voltage with the silicon because after all this charge is exponential related to whatever background charge is there whole concentration is 10 to the power 16, 10 to the power 16 into e to the power of phi by b t. So, let us say phi is even if it is 2 milivolts it were of phi by b t will raise this particular carry a concentration from 10 to the power 16 to double that value very easily. 25 milivolts if you take e to the power of 25 milivolts by 25 milivolts 2.27. So, if doping is 10 to the power 16, 10 to the power 16 into e to the power of 1, 2.27 times 10 to the power 16.

So, carry a concentration very large there. So, at the voltage that surface potential there is just few milivolts 25 milivolts. So, what we are telling is by applying an anti voltage the entire voltage will drop across this particular region and the potential of the surface will be raised with respect to the source by very small quantity 25 milivolts, 30 milivolts of that order. So, we are neglecting that and saying that that one (Refer Time: 42:15) 0 you can take into account and see that you will the analysis will still hold good. So, I am neglecting that voltage surface potential take in terms 0 that is what I put here psi s b is 0. So, when you do the entire analysis you will see that if you want to consider right angle accumulated you can put psi s b equal to 0, front channel inverted you will put psi s f is equal to twice phi f this is understanding that with which we are doing the analysis sim or simplification, but holds good quite a bit.

So, if I draw the electric field here I fix the voltages V g b there will be electric field like this then with charger plus charger, minus charger this plus charge can be very long because doping (Refer Time: 43:02) there and this will be negative charge. Now, when you started with that by a 6th we are not varying that voltage we are not varying the field, when I apply voltage to the front gate what happens initially, I am applying it with

respect to sub state that is with respect to source. So, apply voltage exactly in this case oh I am sorry exactly like this it will start appearing, you know it is not depleted fully and the volt is very low some voltage appear across the oxide some voltage across the silicon.

So, we will have initially there will be depletion layer starting from 0 here entire layer is not depleted initially there is 0 potential here depletion will start widening and at one point the depletion layer will come and merge here that is the dotted line. This dotted line is the situation when the depletion layer from front side has, from the front side has widened and ultimately merged with this point wherever the negative charge come growat the time from the depleted portion.

When I apply a plus voltage to the gate there is no charge here negative charge come from this substrate as the depletion layer widens because more and more plus charges are at the from gate more and more negatives from the substrate more and more widening from the depletion layer. At a particular point you can call it as the punch through voltage where the depletion area has completely merged with this point that is the electric field distribution there similar to this, but this field will be much smaller than that because this field was large on micron.

Let us say and that does not depleted this is if it is 10 to the power 16 this let us say point 2 microns it has depleted fully, but if it is point if it is 10 to the power 16 doping and this is 0.1 micron surface potential is not pi 5. When this has depleted here just go back to that graph and show you here itself you can see if it is 10 to the power 16 surface potential become phi square if the depletion has become 0.3 microns. Now, if you cut it from here and keep it only 1 micron it whole thing will be lowered than this.

So, there is you have got edge of the depletion layer here potentially is much lower than that, all that you do is you pull this side down. So, that field is lower, so when the depletion layer is not point 3 micron the voltage drop across silicon is not twice phi it is less than that. So, that is the situation here it is not twice phi square f and oxide drop is actually corresponding to this peak field you have got the off square drop which is lower than that, you have to follow very carefully this bit its slightly different from what we usually discuss. Now, at this point what are plus charges available was coming from negative charge here depletion layer, beyond that if I increase the voltage plus charge I

put here the minus charge will come from, where can it come from it can come from the other end. So, what happens is the field science from here rise parallely I wish I had another diagram here see at this point electric field is something maximum here, here it is 0.

Now, if I increase electric field at this point that is a hundred lines increase from here to here that side all the 100 lines do have any negative charge here it will have to go to the other end of the gate where there is negative supply is there. So, the extra 100 lines all of them cross this or centrifugation the electric field has increased from here to here by some delta I the delta I is 100 lines. All the 100 lines delta G will cross this; that means, 100 lines which are extra crossing here will cross this also; that means, electric field will increase from here to here by delta i. So, what we are telling is this distribution is not going to change, because there are no charges to terminate.

See electric field distribution if I see electric field will go up here if there are charges here, but there are no charges here. So, whatever extra charge is coming here it cross here. So, the entire field line will go up here by this parallel that is a meaning of drawing this line is there are no charges in between all the charges will come from here. So, what will be the voltage distribution, voltage here is not changing why your held to stay constant by the back gate that is remaining same thing, but this is field remaining same thing as before, it is not changing, but what has happened is the plus charges here have reduced because the negative charges that has over 1000 lines here originally out of which now here its only 1000 charges if there are field lines are constant.

Now, when this extra 100 field lines come here these are not changed that is because they field lines which are coming underline is coming here, remove those plus charges because they are coming from here now, you got that extra hundred lines coming from here there is no need of the plus hun plus 1000 charges there will be only 900 charges and this is the numerical number because 1000 charges here 900 charges here 100 charges coming extra from there as you tell (Refer Time: 50:13).

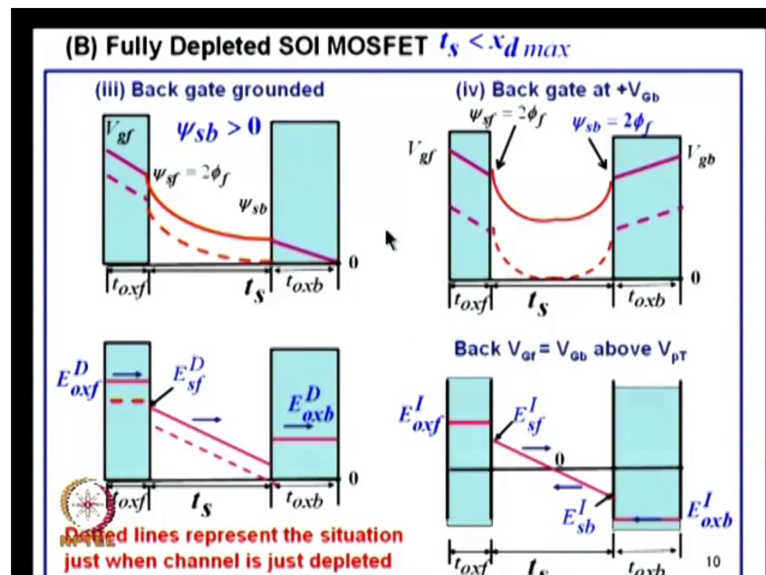
So, this field is not changing this voltage operator is not changing, but field lines have moved up here. So, the distribution now will be this potential is 0 here, why there are plus charges here with very small potential here that is the stilled accumulation is maintained. So, longer there are plus charges here accumulated plus charges are there

where are the plus charges coming from are accumulated. So, longer there are plus charges are present potential is 0, if I go on increasing the plus charger decept here then it started depleting, but there are plus charges at 0. So, from here to here is what is the potential here; we are considering situation as inverted psi f. So, now, we know the potential in the silicon which is less than this 0.3 microns.

Now it is point one micron the potential dropped upon silicon is more is twice phi f, but the length or width in which the potential drops is smaller. So, evidently we see that the field here will be higher. So, that aspect you can see from here corresponding this field will be higher field here will be higher. So, this is SOI MOSFET in the back channel accumulated, we will discuss about the voltage calculation in the next presentation, but this is questioning to understand you can before you scoot to next lecture you can go through this once more and we will see appreciate that lecture, next lecture after seeing this only again going through this. So, it is accumulation condition, but here the field will where surface potential is twice phi ok.

Now, let us see the other condition I will finish these 2 before we wind up for today, back channel grounded see this case that channel accumulated by applying voltage.

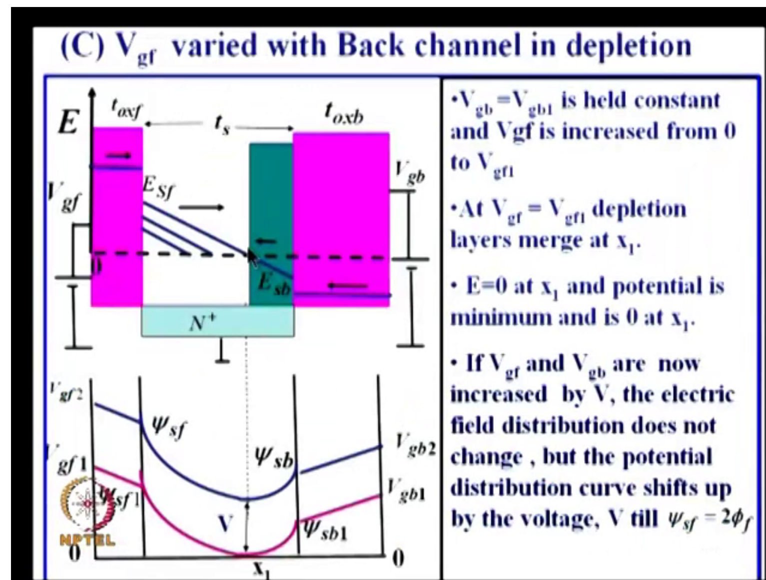
(Refer Slide Time: 52:23)



This is slightly simpler I should taken this first anyway complicated thing finished first go to simpler things afterwards, here I have grounded this connected back channel to the ground no voltage applied. So, as I start applying from the voltage from the back gate

depletion keeps on moving, forget about the solid line observe the dotted line that is the situation when the depletion error has completely depleted this channel, initially depletion error will be narrow it will keep on widening and come up to this point just I will go to 1 slide it will be clearer to you.

(Refer Slide Time: 53:07)



See here for example, I have grounded this point let us say I keep on increasing this voltage then you will have the depletion error narrow initially, higher voltage will widen these are electric field widen electric field like that that situation. So, here I think I have yeah. So, I have parted the dotted line where the depletion error just reached this point not at all from the back gate you have grounded that ok.

So, you can calculate what is the voltage applied voltage is at this point what is the electric field here, q n a into t silicon is the charge divide epsilon silicon is the electric field here. So, from that you can find out this one that is in this case you can straight away see t of s is a charge divide by c oxide is the voltage drop across the oxide. Now, once it is depleted just here beyond that I increase this gate voltage see remember that this is grounded. So, applied voltage now shares between this oxide this silicon and this, once it is just depleted fully if this were silicon what would happen the depletion layer would have moved further down, but now again the same number I have increased the voltage so much that surface potential with respect to ground becomes twice phi f, this is 0 this is potential drop here this is potential drop just when I (Refer Time: 55:13) through

there is drop across the oxide and silicon. When I increase beyond that point at inversion there will be drop here, drop here, drop here and across the front oxide it is linear drop where there is no charge across this is parabolic because charge is constant across this linear drop that is this is 0 that is the rise of potential and the potential is psi s b and this is psi s f. So, if you look into the electric field then psi s b minus 0 that is the e ox b and front oxide is gate voltage that is applied to structure voltage minus twice f that is the oxide, how much voltage I would find how much is the electric field here I can find or voltage I can find out if I find out this surface field.

So, if you want to calculate the threshold voltage of this device all that I have to find out is psi s f, how much is this electric field here when this potential becomes twice psi s f that calculations we will see next time. So, what will you say about the field here compared to the previous case, previous case the drop across the silicon was twice psi f this is 0 this is twice psi f in this case drop across silicon, same silicon thickness 0.1 micron is twice psi f minus psi s b. So, field here is smaller compared to this ok.

Now, let us once again go back to this compare the situation here twice f dropped across 0.3 microns that was depletion layer width. Now, this thickness is smaller, but the voltage drop across that is much smaller twice psi f minus psi s b this can be as close as to that. So, the fields here will be smaller. So, why the I am pointing out this field is we had said that in the bulk MOSFET the mobility is affected by doping, the mobility is affected by the field in a vertical direction. So, vertical direction in this case is like this, but the gate down to the channel. So, you can you can see that in this case because of the difference in the voltage drop across the vertical direction is less the field in the vertical direction will be less than the case of bulk MOSFET.

So, we can see this already there is a pointer telling you that if I use SOI MOSFET the vertical electric field can be used we have to go back later on see where we can reduce the doping concentration also we have to see so this is the situation. Now, let us take the other case where that channel is also inverted, when the back channel is inverted what is surf what is surface potential there means I applied sufficient voltage at the back gate. So, that that is twice psi f I applied sufficient voltage front gate that is twice psi f. So, electric field lines will be terminating here to 0 part of this belonging to top channel part of this belonging to that gate. So, electric field lines will come in this direction left to right and on the right hand side electric field lines will be coming from right to left. So, it

is slightly (Refer Time: 58:45) stage of this where that yeah, I have already balanced with the gate for the depletion error is here let us say.

So, here the deple just when this whole thing is depleted you will have this situation I think I will discuss this in the next lecture what is the scene see here is if both channels are inverted post potential be twice psi f. So, what is the drop across the channel that is difference in the potential is 0. So, drop is low here in this case field is low. So, what we are trying to point out here is in the case of SOI MOSFET we can have a situation where the 4 channels are inverted and the vertical electric field will be smaller if the electric field is small here electric field is small in oxide also you can have that type of situation at (Refer Time: 59:35) voltage we will discuss in next lecture.