Nanoelectronics: Devices and Materials
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Lecture - 19
SOI Technology and comparisons with Bulk Silicon CMOS technology

We begin the discussion on module 2 of the non classical MOSFETs. And in this module, we talk of silicon on insulator SOI MOSFETs.

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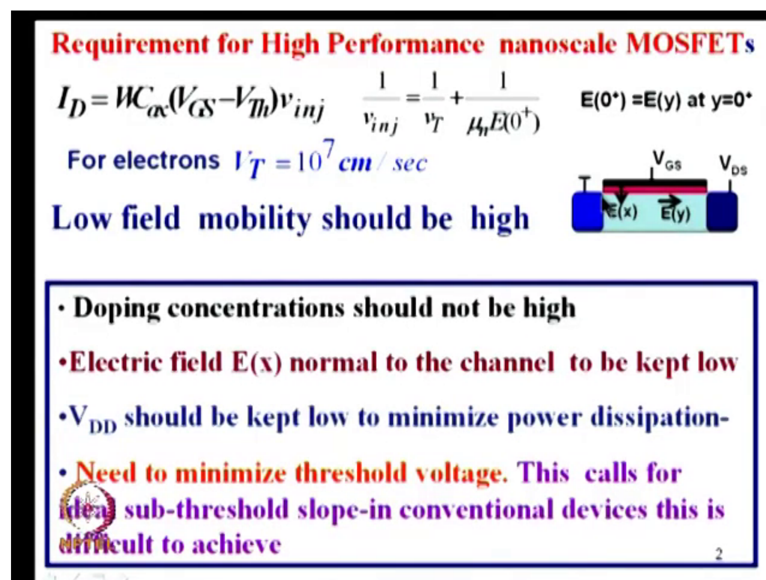

Last time when we discussed, we said or we have seen that the drain current depends upon the injection velocity and that injection velocity depends upon thermal velocity which is 10 to the power of 7 centimeter per second and the product of mobility and the electric field at y equal to 0 that is here at the point of injection; what is the mobility, what is the electric field that is low field.

So, will talk of low field mobility; that means, mobility near the source the end where electric field is low that is the one which controls the injection velocity, you will never get the saturation velocity of 10 to the power of 7 centimeter per second, but it will be less than that how much which is low depends upon the mobility.

So, what we said is if you want to get better performance you need to have higher mobility at low electric fields that is at the source end at everything because everything

depends upon how much is the mobility when it is injected. These are very important particularly when we go to short channel devices because you are trying to get as close as possible to the saturation velocity or the thermal velocity.

So, if you want the mobility to be high what we have shown last time is that a doping concentration in the channel should not be high number one the other factor which affects the mobility of electrons or carriers in the channel is the electric field in the vertical direction or normal direction in a direction normal to the electric to the channel that is that Ex which I have marked x is in that direction that depends upon; what is oxide thickness. And also how much is the doping here is the more are the doping more charges in the dictation layer comes up. So, the electric field in that direction will be higher.

So, you can see that reduce that vertical electric field you need to go to lower mobility. So, both these point to the fact that you need to reduce the mobility of dope ends or mobility of you need to reduce the doping concentration as much as possible. Ideally, you can go to un doped such things are not possible in the classical MOSFET, you have to go to some special type of devices like the SOI MOSFET that is the ideal.

And also of course, supply voltage you must keep low to minimize power dissipation then you need to when you go to lower supply voltages. You will have to have lower threshold voltage and to effectively turn off the device when the gate voltage is 0 when the drain voltage is present, you must have excellent sub threshold slope in the sense, 60 millvolts per decade is important when you want to go for lower supply voltages.

So, that if you have point three volts as the threshold voltage as the time you reduce the gate voltage to 0, the current will fall down by 5 decades 300 by 60. So, that is the idea of that. So, most important thing is to have the mobility as high as possible by keeping the doping concentration as low as possible and for getting these sub threshold slope 60 millivolts per decade just close to its varying, it is impossible mostly in the bulk MOSFET.

So, you have to go to this non classical MOSFETs or what are this high performance non classical MOSFETs.

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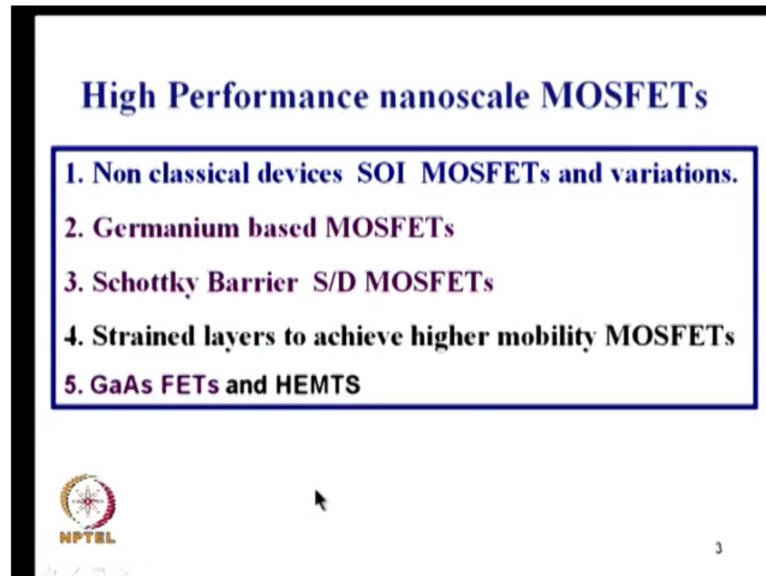

Then one is the SOI MOSFET which we will take up in module 2 there you change the structure. So, it can control the doping concentration and reduce it and you can have multiple gates.

So, that the gate has tremendous control over the channel as compared to the drain see sub threshold slope and all get affected. So, what are the affects come into picture more and more, because the drain take control of this barrier at the source end now if you have a wrapped around a gate which is all around the channel then the gate has excellent control on the channel.

So, that is all in high frequence; high performance nanoscale MOSFETs; when you choose you will see as you go on to the SOI MOSFET, you can ensure that you get the sub threshold slope which is 60 millivolts per decade, the other approach that you used for this high performance devices is basically change the material from silicon to the germanium where you can get high mobilities.

Both electron mobility and hole mobilities can be higher than silicon; only the material like germanium, you can get close to 4 thousand centimeter square per volt second per electrons mobility whole mobility something like about three thousand as compared to 4 fifty in silicon where we can go to materials like gallium arsenide where electron mobility is high, but the whole mobility is not high that all will take up.

So, germanium MOSFET also we will discuss in the at the new material lot of research work is going on that everywhere you will see that you have problem of the interface gates scaling the performance of device the another non classical type of devices the source and drain of the MOSFETs are metal semiconductor contacts. Let us say short key barrier contacts as compared to the P N junction why we should do that we will see.

The main reason to do that is to reduce the series resistance; resistance of the source region and of course, one more thing that I pointed out last time was you can have the channels which are strained. So, that you can control the mobility or increase the mobility by either increasing or reducing the strain depending upon whether it is P channel or N channel ultimately. Of course, you can go gallium arsenide FETs, then there is one class of hetero junction devices called high electron mobility transistor because you can get very high mobilities particularly when you go the temperatures.

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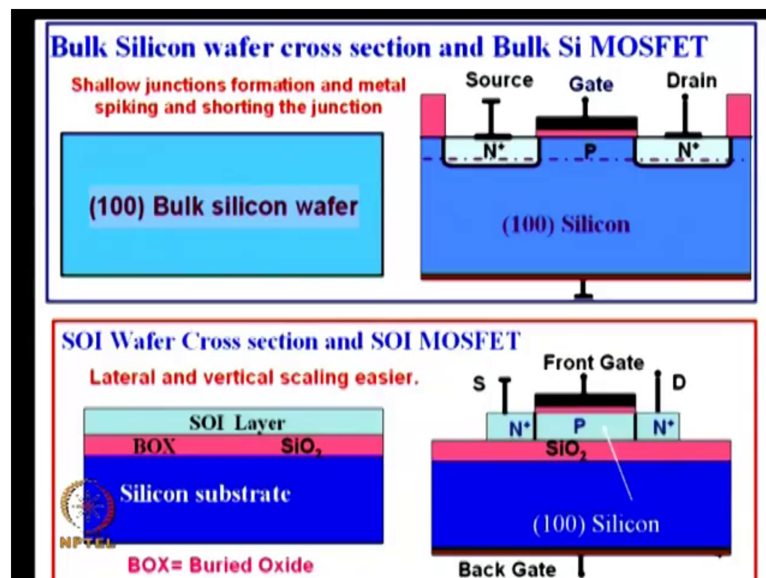

This is the usual bulk MOSFET structure in a very simplified way there are slight variations in all the things we have got the PN junction; PN junction and the gate poly silicon gate. Today, we will talk a metal gate also this is the cross section of the silicon wafer bulk 1 0 0 oriented this were the device cross section.

Now, if you recall the discussion on short channel devices you not only reduce the dimensions in the lateral direction keep on shrinking in the direction, you also shrink in

the direction vertically, because only when you shrink vertically you can get shrinking in a lateral direction possible.

For example in this junction if I make this junction depth 10 microns, let us say, then the lateral diffusion. So, this junction moved in to the channel at least seventy eight microns. So, it becomes very difficult to control the channel length reduce it to 1 micron half micron; 0.1 micron.

So, we need to keep the junction depth very very shallow. So, keep the junction depth very very shallow, you encounter some other problems like when you put the metal here on the top if you have a metal there, if it is aluminium particularly you run into problem because that can it is junction is very shallow it can spike through this junction, it can sort because it is P type material on substrate.

Of course you today you change the material to some senocides, then that problem is reduced drastically main thing is lateral diffusion is the one which you want to control you want to keep the junction at swallow. Now, instead of taking this conventional bulk MOSFET you go make use of a SOI wafer you have the silicon at the bottom you have the red color that is SiO 2, then you have the silicon layer at the top.

So, notice in the case of bulk MOSFET strictly you are using only this portion only top portion only that dotted line, I have put below that it is of no use. So, the SOI is nothing but the top layer cut there and realized on this side on this layer. So, if you go to this device there on the right hand side you can see it is nothing but the same thing cut and put here it is done.

So, you start with the wafer with which is silicon on insulator there are different ways of making this devices. So, if I have this called box buried oxide, it looks as buried oxide before the surface, it may not be buried really, but in some cases when you make them SOI you actually burry the oxide we will see how to do that.

So, SOI layer this you used now once you have this thing how much is the layer the junction depth here there is no junction here where it is diffuses all through there is no P type layer the silicon is retting on the oxide. So, when you put a metal there even if the metal spikes and goes through there is no short circuit because there is oxide below, so embossed aluminium itself very comfortable here.

So, you can see; how much is this junction area. So, in this case a junction area is vertical horizontal vertical the horizontal portion may be at least few micron you must keep it wide enough. So, that the metal that you put here that may be taking 5 microns, let us say then this must take at least 10 microns. So, that extra junction is present in that portion whereas, here the junction is only here vertical that may be point 2 microns point 2 microns very small junction area.

What is a junction area the depth multiplied by the width it goes perpendicular to that area plane of wafer it goes like that depth. So, depth is perpendicular to this plane here. So, w into this t silicon that is a junction area whereas, in the previous case it is w into the total area there this may be large 10 microns or 5 microns, but this will be only about less than the micron you will see its even goes to nano.

Today when you talk of nano devices you talk of the layers which are of nano dimensions 10 nanometers 20 nanometers of that order you will see the benefits of that as you go on. So, junction area is small here and you are not worried about reducing the thickness of the layer you are not worried about spiking or metal sorting.

So, shallow junction formation and metal spiking and shorting in the junction; what is available here will not be there and since the junction depth is very very shallow, here lateral encroachment of the junction into the channel is minimized. So, when what makes smaller devices these are called beneficial.

Now, let us just take a look at what are the different types of SOI wafers which are present classically.

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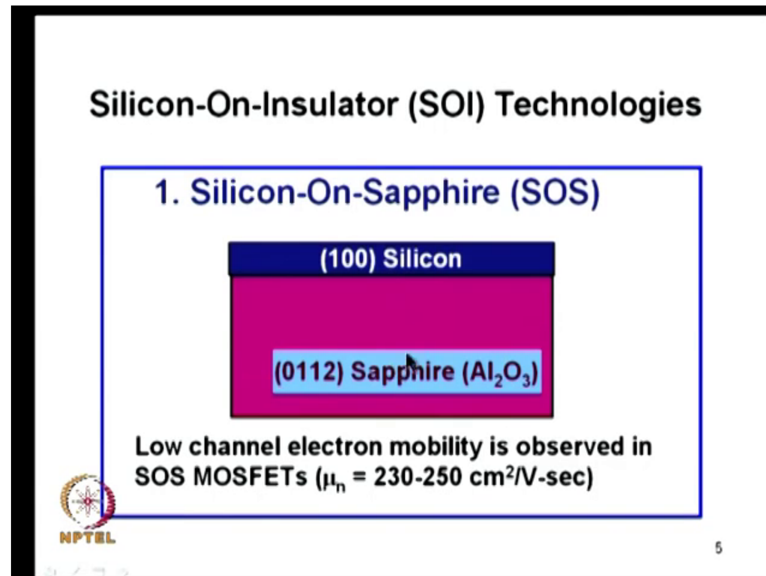

Or historically the SOI was not SOI; SOS not save our soul, it is silicon on sapphire this is sapphire single crystal sapphire Al 2 O3 can crystal chrome you can buy it very expensive much more costlier than silicon several times costly.

On that you grow 1 0 0 oriented silicon epitaxially, you can have this point one microns or of that order use this particular for making the device. Now you see entire layer below that is insulator fantastic if you can get that you can get that people use this even today for some of the very sophisticated radiation hardened type of devices for defense applications they use this, but very expensive.

They get 4 inch wafers not I do not think there are; there is a dimensions are there bigger than the 4 inch because of difficult in going that Al 2 O 3 that is a high temperature process, but there is some issue here the channel mobility here is not very high because the quality of this layer when you make it is thin, it is not as good because this is does not match very well with the substrate lattice match is not so good. So, the quality is not so good.

But if we not looking at the high mobility if we are looking at other performance like radiation hardening and also if you are looking into the you know the rooting capacitance for example, when you connect one device to the another device on the surface of oxide if this insulating layer is very thick the capacitance of this rooting capacitance with respect to substrate is very very small.

So, you know those parasitic capacitance are very small in this case and also when you make a device like that when you make a device like that the junction capacitance also is small because junction area is small. So, here it just make the device there you get junction area small capacitance small stray capacitance small that is why we get much better performance.

Ultimately in the integrated circuits you know that the culprit is a stray parasitic capacitance. So, you want to make reduce that you can do with this. So, most of the defense applications they use that there is this is start crystal see; it is a external structure that is why 0 1 1 2 is the orientation that particular orientation only there is fairly good lattice match between silicon and sapphire.

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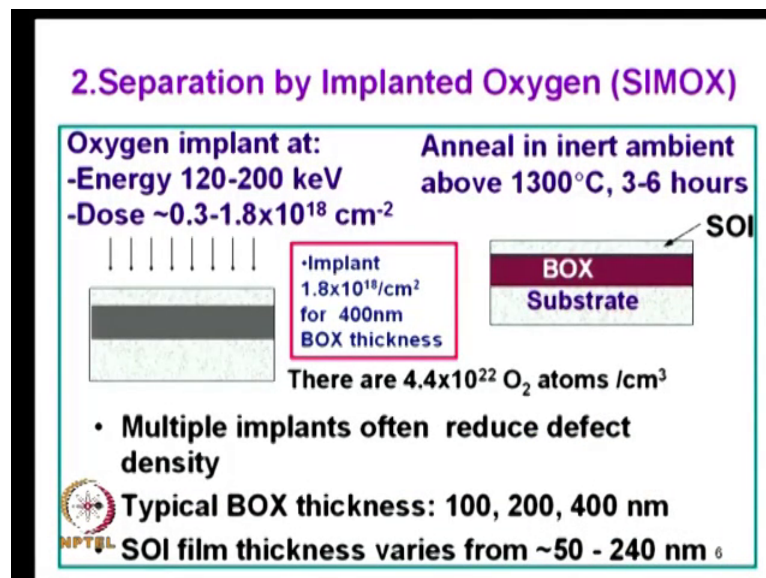

But if you want a cheaper way of doing this you go to this type of structure where the silicon is on oxide you can choose it 1 micron whatever thickness you like not too thick. So, instead of taking whole thing as sapphire you have got SiO 2, there this also will reduce the stray capacitance because the thick oxide below a parasitic capacitance will be reduced.

So, how do they do that this is a very popular way which by which the SOI layers are made in IBM in their main stream integrated circuits they use the SOI layers which are called SIMOX layers; SIMOX is separation by implanted oxygen here actually you are really burying that oxide how do you do that.

Take a silicon wafer the full thing is silicon there cross section implant oxygen atom implant the atoms itself implant; implant comes, it comes at as ion, but it gets neutralized after implantation it is neutral. So, implant it at energies like 100 to 200 kilo electron volt. So, that the oxygen atom gets inside the layer and it is implanted into the bulk of silicon the dark region which is shown here is actually the region into which you have implanted.

Actually what happens is when you implant it depending upon energy the depth at which it is implanted is decided may be half a micron point 1 micron that is depends how much lower energy will be implanted close to the thing close to the surface. Now I put a band of region because when they implant the impurities or any material, it is not going to stay in one place, it goes through a surface most of them land at one particular depth, but there is a spread because after all where it lands depends upon the number of collisions it experiences.

In the sense it comes at let say 100 keV energy, it collides with one atom the host atom it is like a billiards ball. So, it collides with that gets scattered the lattice atom of the host atom also moves you know in a billiards when they play that moves this also get reflected. So, in one collision it loses some energy after undergoing several collisions, it comes to rest.

So, how far it goes to rest depends upon what are the energy how much energy it loses in each collision and how much it loses also depend upon the host atom and the whether it hits atom collision or at a slight angle. So, if it shut down collision then maximum energy will be lost in one collision if it is at an angle cos theta of that energy will be lost it is actually proportional to the product of the 2 masses heavier masses will lose energy further it will be difficult to implant deeper.

So, this oxygen atom you will see at the as a spread because depending upon the angle and the number of collisions it experiences it is a statistical phenomenon its landed in one place there here it will be around that region that is why that depth band is put there. So, when you implanted it was just oxygen atom. Now raise it to high temperature like 1300 centigrade silicon does not melt at that temperature because melting point is 1410 degree centigrade.

So, that i change the color here because it has become a SiO 2 silicon dioxide because of that oxygen reacted silicon. So, what happens is when the reaction takes place there will be swelling volume will increase you know that if you just look at number of atoms per centimeter cubed of silicon is 5 into 10 to the power of22per centimeter cubed.

So, I just put some numbers here just I will come back to the slide. So, if I have 1 micron oxide found there, it has if the thickness of this is 1 micron; I am giving an example the thickness of silicon is 0.44 micron even in thermal oxide, here also 0.44 whatever atoms is there in 0.44 micron would have reacted with the oxygen.

In 0.44 micron there will some number of atoms will be there into 2.27 number of oxygen atoms will react to that into 2.2 into 2 whatever number of atoms is there into 2 for one silicon atom 2 oxygen atoms. So, twice the number of oxygen atoms react to that to get this thickness, but the volume or the thickness will be 2.27 times.

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Number oxygen atoms in SiO_2 layer of 1 micron thickness

1μm SiO_2 is formed by oxidation of 0.44 μm thickness of Si

No of Si atoms in 1μm thick SiO_2 = $0.44 \times 5 \times 10^{22} \times 10^{-4} = 2.2 \times 10^{18}$

No of Oxygen atoms in 1μm thickness of SiO_2 = $4.4 \times 10^{18} / cm^2$

O_2 atoms implanted to achieve 1μm thick BOX layer = $4.4 \times 10^{18} / cm^2$

Oxygen dose required for 400 nm (=0.4 micron) BOX= $1.76 \times 10^{18} / cm^2$

NPTEL

So, what I have just put here is to make it here number of atoms in silicon 1 micron silicon dioxide is 5 into 10 to the power 22 into 10 to the power of this is number per centimeter cubed silicon atoms into 10 to the power of 4 is in 1 micron. So, many atoms are there.

So, in 0.44 silicon that is number of atoms present number of oxygen atoms in 1 micron will be that into 2 see so many number of silicon atoms will react with twice the number of oxygen atoms. So, that is number of oxygen atoms.

So, what I have said is in point for 4 micron thickness of silicon; how many silicon atoms are there. Now the twice the number of oxygen atoms will react with that to give the SiO 2 which is 1 micron that is the idea now whatever was 0.44 into 2.7 is the thickness because it is expands.

So, the in 1 micron that is the thing if it is 0.5 micron oxide, if I want, then will be 4 times that there about 1.8 into 10 to the power of 18 oxygen atom per centimeter of cube centimeter of square I put that number because I have written here implant 1.8 into 10 to the power of 18 centimeter squared of oxygen atoms to get about 0.4 micron that is 400 nanometers that working out I gave here.

So, what we are telling is we put that number of atoms you get point 4 nanometers of point 4 microns thickness of buried oxide. So, this involves high temperature process this is what IBM uses for realizing SOI wafers which are called SIMOX typically how much is the buried oxide is controlled by how much thickness is there controlled by what is implantation dose. So, that is the; because it consumes from with a silicon atoms.

Usually it is 100 to 400 micron nanometer is the thickness this annealing is done for very long time because after all you have implanted the oxygen and the reaction takes place there this is a technology. So, you can see it require lot of implantation system etcetera for this and industries do that; what if I want to do it in our lab in a university level where is we do not have implantation which will cost you several crores and lot of space will take.

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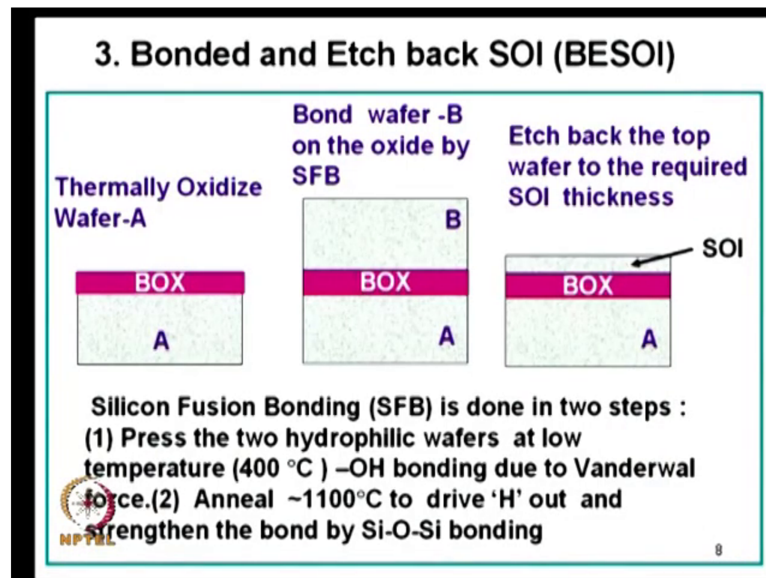

We use simpler methods that is BESOI Bond and etch back, this is very simple the FIBAX implant anneal you get the oxide layer buried here thermally oxidize silicon, we want 1 micron grow 1 micron point 1 micron; grow 0.1 micron, take another silicon wafer, put them together, it will bond provided you; allow it to bond in the sense what you do is this wafer is there another wafer is there both of them you must make hydrophilic.

You give a chemical treatment. In fact, when you use some chemicals like ammonium hydroxide ammonia H2, O2, etcetera for cleaning up automatically that scatters up; so, HCL and hydrogen peroxide you use for cleaning up the wafer then their water cleaning automatically there are oh ions.

So, which is when you put them together it is bonding between the oh and oh from the 2 atoms 2 layers you call it as Vanderwal force a weak binding. So, put them together press it you can heat it 400 degree centigrade; fairly good bonding takes place, take it high temperature like 1100 degree centigrade couple of hours it has, oh, oh, bonding when heat it at high temperature hydrogen comes out you get silicon oxygen silicon bonding. Now it is completely SiO 2.

So, this bonding takes place you have got a single wafer now which has oxide in between few got virtually buried in the oxide, but now this is 300 micron; 300 micron; how do I get a SOI etch that layer to reduce the thickness you can just keep on etching, it

chemically wet chemical or dry etching you can use how much thickness you can depends upon the etched duration they are thick driven where as we have controlling the thickness you can get this exact thickness.

So, this is the process press the 2 hydrophilic wafers what is hydrophilic it is not hydrophobic water heating and water. So, oh ions are there, then after wards anneal, then etch, it this is called bond and etch back BESOI. In fact, this type of bonding we can do in the lab level where there is very clean class 100 even better clean rooms are there you can do the bonding.

This type of wafers are very popular in because you have this thin layer here you remove the silicon from the bottom here you get a membrane, you just etch out somewhere in between the center from all the way you have got the oxide and then this silicon which is a membrane anyway I will not go into that this is in the main course that we talk of.

Other method is not cut see here there is one issue see for making one SOI wafer you have used 2 wafers polished wafers for 2 wafers and at the end of the process you have other wafer you have just dissolved see waste so.

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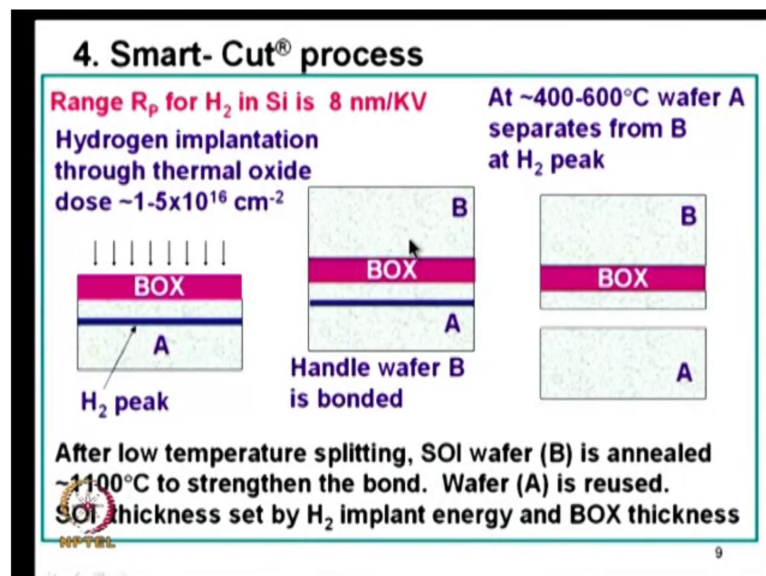

In order to overcome that and also precisely get this thickness here the precise thickness is controlled by the timing of etching which may cause to little bit if you want to if I

want 20 micron thick layer 0.5 micron difference in this 20 you may not very much if you want 1 micron thickness here that becomes very crucial.

So, in those cases and also if you want to use only one wafer per SOI what you do is use smart cut method is patent of some company. So, what you do is take this is dark is coming afterwards take a silicon wafer oxidize, it to get the buried oxide oxidize, it implant hydrogen through the oxide, how much deep hydrogen goes depends upon the energy of the hydrogen it is about one kilo volt energy in implanter if you use it will go about eight nanometers below surface.

That is 80 angstroms, I used 10 kilo electron volts it will be 800 angstroms 80 nanometers. So, what deep you have got this hydrogen below the surface depends upon the energy that is under our control. So, remember I can get this even as low as 0.1 microns or even as low as 80 nanometers very easily.

So, once you do that you take another wafer and bond on the top on the top of that you bond it. So, that bond this is the b is called the handle wafer see for example, here when i get the SOI this is the handle wafer these not doing any job its only the mechanical support for holding this SOI layer. So, that portion will be the handle wafer which comes below.

So, once you do that what happens is when you have hydrogen implanted it, it results in cavities that is hydrogen makes cavities in silicon in this layer you put heavy dose of about 10 to the power of 16 per centimeter square you will get weak link between the this portion and this portion the cavity.

So, hydrogen is a included there in the silicon that is why it makes cavities now when you bond it and anneal it even at low temperatures this; this up because of the weak link there it just comes apart it is like putting a hat and taking it out. So, that comes out like this. So, what is happened now this layer thickness is this thickness and that thickness is controlled by how much energy we had hydrogen atoms? So, you can precisely control the thickness here we precisely control this thickness.

So, you put it upside down you have got the SOI layer on top another wafer like that you put it like that you get the you put it like that you get the SOI layer reverse it . So, now,

you can see this layer thickness of 300 microns out of that; let us say half a micron is gone on to this. So, still you have got 299.5 microns of silicon which is separated.

So, once this is separated out you have got the silicon on insulator already you have to put subset on of course, and this wafers which were there its available for you for reusing all that you have to do is you may have to slightly polish it polish it, reuse it start all over again oxidize and go through the thing. So, in effect what have happened is you have used 2 wafers with, but one wafer is available for you produce ultimately only one wafer is used one advantage other advantage is the thickness is precisely controlled by the implantation energy.

So, this is very popular commercially available. So, you can buy SIMOX wafer you can buy smart cut now only thing that you will be concerned the one for memes application, I may need a thick membrane say 20 micron, etcetera that you may not able to get because you will not able to have energies of that height implant in deep below 20 microns.

So, in that case; what you do is take this wafer which is 0.5 microns grow epitaxially 10 microns of silicon, then you will get 10 microns of SOI layer. So, if you want 10 micron of smart cut this wafer you can buy it, but if you want thicker ones better way to go is this one because you do not worry about slight change in the thickness, but waste one wafer because you have used 2 wafers to get one.

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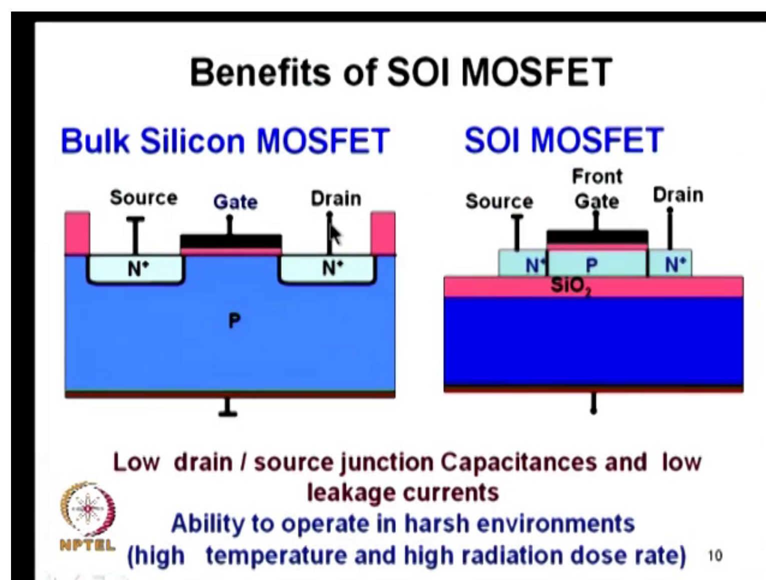

So, now let see the benefits of these are the technologies some other technologies also have come, but these are the most popular techniques. Now already I have mentioned to you some advantages of the bulk silicon MOSFET and the SOI MOSFET clearly the drain and source junction capacitance are small here. Because junction area only this much into the w channel width. And here that plus all these setting it will be an order of magnitude the area of this junction will large compare to that because, this will be sub micron this will be several microns. Because it has accommodate also to metal contact there you cannot have this nano here this will be one will occupy.

So, this junction capacitance is small straight away one stray capacitance is reduced to the routing capacitance from one device to the other device because of the buried oxide below is also reduced plus the junction leakage current junction leakage current depends upon the area of the junction in the SOI layer the junction area is smaller. So, leakage current is smaller. So, if the leakage currents are smaller even at room temperature we will be able to use this for high temperatures.

So, the bulk MOSFET when you can use for 100 degree centigrade probably per devices you can go to 200 degree centigrade fairly comfortably. So, higher temperatures if you want to use SOI MOSFET is the way to go also you can use it in radiation environment because in a problem in radiation environment is when the high energy particles like the gamma radiation etcetera comes into impinges here it generates hole electron pairs in the silicon.

When the hole electron pairs are generated here in the depletion layer below this point it is collected it gives rise to t drain large drain current plus it will also if you have a CMOS structure, it will also lead to latch up problem that we will see what it is because of coupling between the P channel and N channel MOSFET you will have that problem you will not have other problem.

So, this type of device can be used for high temperature and operation in harsh environment like the radiation environment capacitance is low other benefits.

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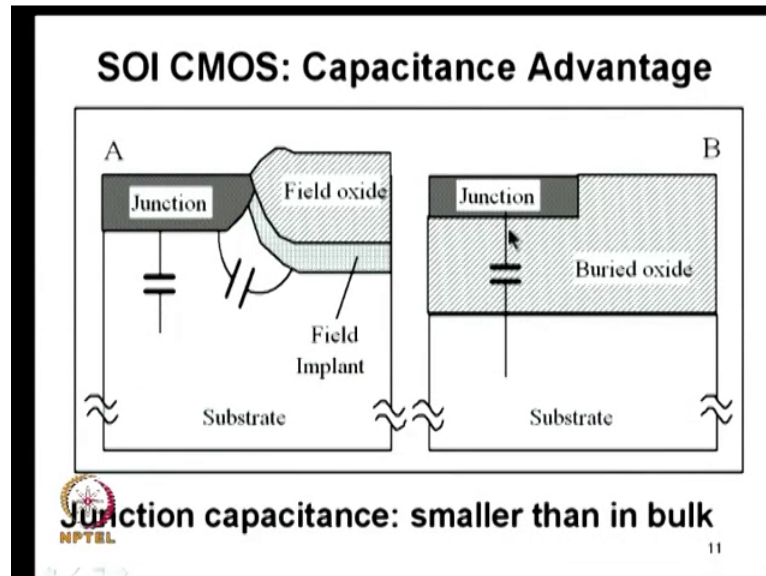

This is actually show whatever I have said here you can see this is junction capacitance which depends upon doping and this is a junction capacitance which depends up on the buried oxide which is very thick. So, capacitance will be small.

In fact, there is no junction here it is a capacitance this layer and this substrate and this area can be small here and the junction is the only here, I am sorry if only the buried oxide we are showing it is easy to see here. So, only buried oxide this capacitance from here to down between this and this is reiterating whatever I have said before.

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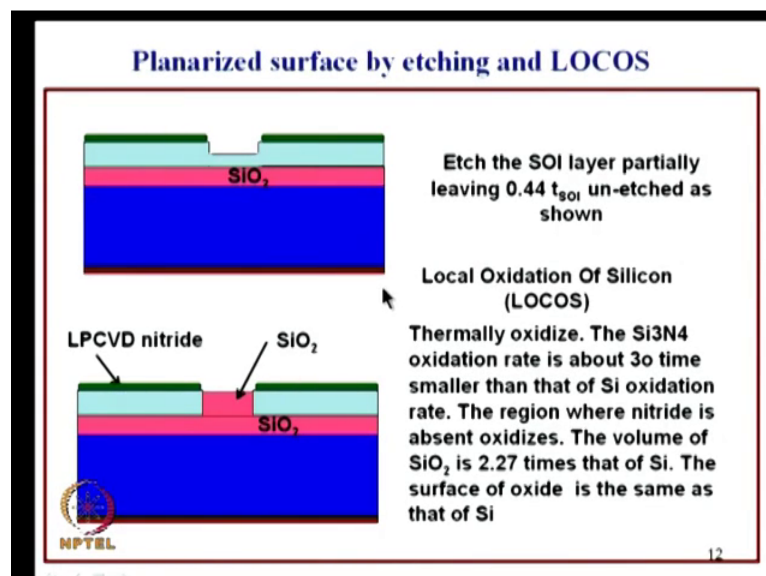

And also here you can have capacitance between this and that below the field oxide field implant additional capacitances.

See here what we have shown is that the full layer is there you can etch the silicon to have the MOSFET completely isolated from other MOSFETs, if you go back into whatever you had discussion in the case of MOSFET integrated circuits below that between the 2 transistors you have that P plus implantation to prevent it from inverting.

Here you have got a thick oxide very thick oxide you have below that. And if you want any plantation you put it down there, but you do not need that because complete isolation is there it is no silicon. Now what you can do will be on my question there is a step here from one device to another device, but you want to have a planar structure why do you want planar structure lithography becomes difficult if the there are steps big steps.

So, what you do is suppose, I want etch silicon from here if I do not have the red it is a step. now instead of that what I do is I etch the silicon from here suppose is this is 1 micron silicon just as an example SOI layer is 1 micron I etch it leaving 0.44 micron and this is nitrite deposited on the top.

So, that while etching it can protect etch SOI layer partially leaving 0.44 micron of SOI layer on etched as shown here. Now oxidize it; see if I did not have this nitrites low pressure CVD, it is a technique by which you deposit by the reaction of silane and ammonia you can get silicon nitrite that nitrite is tough one tough in the sense if you put it in the oxidizing ambient it oxidizes very very slowly.

For example, if I have nitrite here and a step here and I subject it to oxidation on this surface this layer will get oxidized the oxidization rate depends upon the temperature. So, when this oxidizes this portion hardly gets oxidized because nitrite is there nitrite the oxidation rate of nitrite silicon nitrite Si_3N_4 is about 30 times smaller than that of that of silicon.

So, even by that time if I grow 0.1 micron of oxide nitrite will oxidize one by thirtieth of point 1 micron hardly any oxide is there. So, nitrite is impact silicon is not getting oxidized protecting it from oxide so; that means, what you are doing is you are oxidizing locally here that is called local oxidation of silicon or locos at the sometime we are

discussing and the field oxide you see a local oxidation, it may get inside slightly here, but ideally it will be the same.

So, now if I had used 1 micron silicon and 0.44 silicon is left by etching, I oxidize it these silicon after oxidation expands 2.2 to several times and this thickness becomes equals to 1 micron. So, 0.44 micron of silicon when you oxidize thickness becomes one micron.

So, you can see that oxide thickness here is 1 micron and this is in touch with this you can shift of that nitrite afterwards or the atmospheric oxide auto etching you can remove this nitrite. So, you can have the plane parallel structure silicon isolated from each other with oxide all around, you can see that the silicon layer is isolated from the bottom silicon layer like that and each island is isolated by oxide in between and there is no step all these advantages are there.

So, that is what I have shown here.

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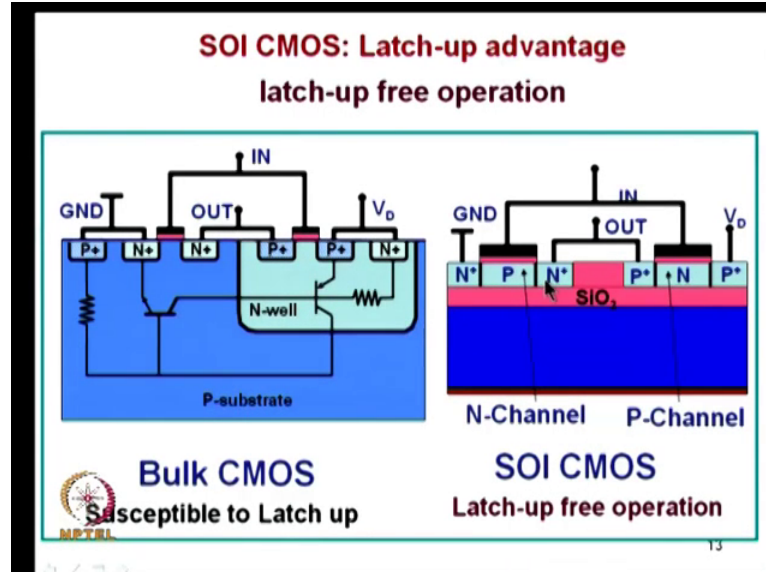

I want to make CMOS, how do I make you can first create this island one island another island that may be very lightly doped P type all over. So, what you do here is protect this side completely you can implant the source drain regions always you implant under any rate, I am not going through those steps you can create make this transistor by protecting the other side implanting source drain region.

Now, you can protect this side with photo resist you can use photo resist as mask for implantation that is the nice thing about that through lithography leave the photo resist some portion implant wherever pho resist is not there implant it see if I want we have a P type layer here completely I can implant on to this N type dopants make this entirely N channel N type material.

So, instead of making P well N well, etcetera, you make this P type and N type P type originally make it N type, then the usual procedures to make the source drain regions here source drain regions here those steps are same I will not going through go through that this is poly silicon this will be path poly silicon. So, this is the structural CMOS schematic what about the when the bulk MOSFET this is schematic simple version if it do not do anything exotic what we will have will be this is the N channel MOSFET.

That is a source drain of the N channel MOSFET and the source is connected to a guard ring they ground it. So, because after all you see substrate is connected to the source in the MOSFET that is always there when you make a MOSFET if you just remember you always connect the substrate to the source so that the bipolar action that comes out of action.

So, you have this connected to the ground that is the N channel MOSFET and to create the P channel MOSFET you have to implant N type regions N well and here also you make this N plus to terminate it. So, that you make ohmic contact and these 2 together substrate connected to the source substrate connected to the source. So, these are these are usual structure there may be variations of these arrangement.

Now, you can see what happens here I do not know whether you are aware of the thyristor action PN-PN structure you can see here you got P N; P N is a thyristor wherever you get that type of structure the thyristor characteristics is its not usually, but to some spurious pickup somewhere let us say this injects holes into that supposing this take voltage from spike there may be voltage spikes coming up or some noise pick up.

This voltage goes up this gets forward biased more this injects holes and this PNP transistor that is P N and P that is what I have marked here if PNP transistor injects electrons into the emitter to the base collector and collector is driving the base of the NPN transistor this is the N P N; N P N. So, this PNP transistor drives the base of the

NPN transistor if there is spurious pickup even if there is a variation that can generate hole electron pairs and that can be power bias this; this will be injection.

So, if it drives the base of the transistor what happens NPN transistor you drive the base this transform. So, this emitter current increases that drives the base of the PNP transistor. So, it is a positive feedback situation PNP somehow got triggered base driven other base also goes on building up and current goes on building up till the external current is limited by till the current is limited by external resistance either that or device will get damaged there is no limiting factor.

In logic circuits there will be malfunctioning of the logic state. So, you want how to prevent that prevent this base collector driving the base of the transistor there may be spurious response here prevent it from driving the base of the transistor how to do that isolate this by putting shallow trenches even remove this portion completely put a trench there put a oxide do not know whether we have the diagram here you can see here.

So, you have to put tranches in between here you see already by the way you met there very thin layer is there you can local oxidation you can do you can isolate them physically isolated electrically isolated completely from each other. So, you do not have to worry about latch up problem this is called latch up, because once it have driven positive it went on building up it gets thyristors get turned on drivens in on state.

How can you turn it off either you have to remove the supply you cannot do it in a integrated circuit you cannot turn off or you must have commutating circuits where that force the current gain operator to bring it up all that you can do in power electronics probably, but here you cannot do here in the ic.

So, you must prevent that latch up phenomenon which is generic problem in the bulk CMOS, it is not there here. So, in bulk CMOS you know you do this.

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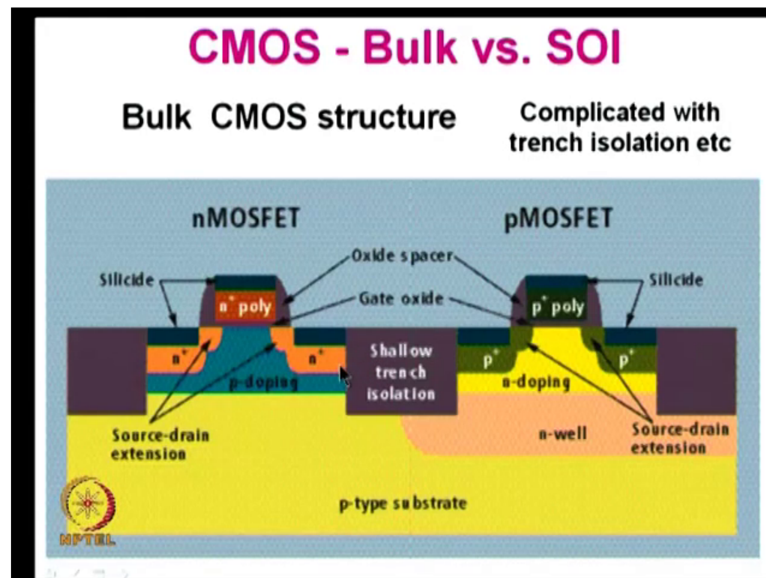

Type of things you can see that you see how complicated theories, you have got slightly doped regions you have got these regions all these things and in between you have got a trench created, it is not enough if you create a trench you have to again fill up that with oxide.

This is shallow trench, but it has to go deep enough. So, that it covers all these portions. So, what they do is trench you create fill up the oxide then you have to make it plane by lapping and polishing. In fact, the Intel does not go for a SOI that is what they say they believe in shrinking the dimensions in the bulk MOSFET, but the process is. So, complicated that you to get the planar structure you have to lap it lap it means that apprisive reduce it by force holding like that rubbing it.

So, yield may go down in that. In fact, we are talking to some other people in Intel, they say that applies to our yield so, but still I think everywhere they try to see how far SOI can be used. So, these problems are not there in the SOI and this is another version of that.

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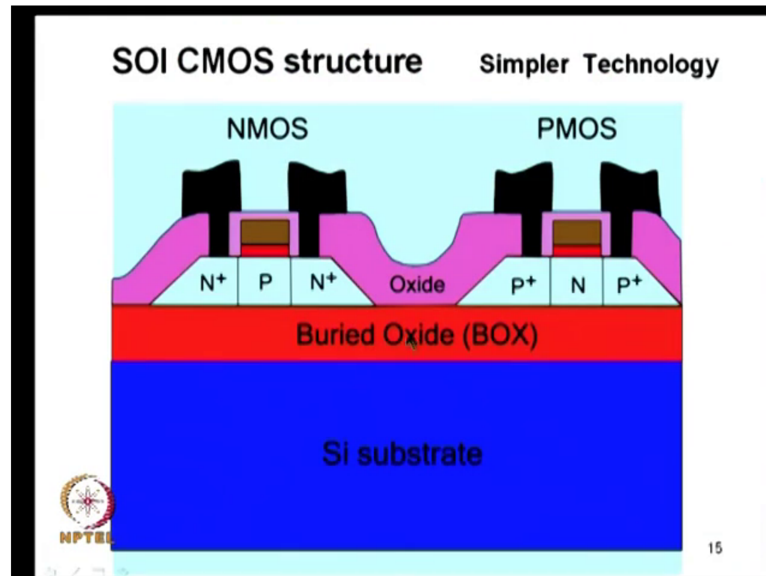

I just show this is more simplified way or different way they saw like this N channel y channel metal contact metal contact oxide everywhere.

Redraw in different way that if there thick layer you can go like that, but you; you can have them planar structure almost like that if it is very thin layer usually you will see that you will go to very thin layers the integrated circuits now.

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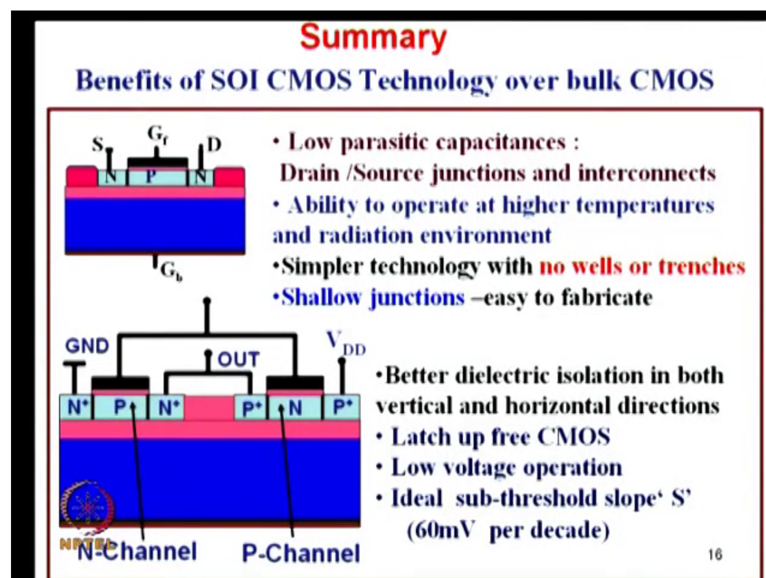

With summary of these things about the SOI, we have seen the technology of that how to make them we have also seen what are the benefits. Benefits are low parasitic

capacitance drain source junctions and interconnects all those capacitance are reduced because of the thick buried oxide ability to operate at high temperatures and radiation environment.

I will show you we when we talk about the single MOSFET; it is that simpler technology no wells and trenches shallow junctions easy to fabricate because there is no junction here its only at the another junction here, it is only here that is the what makes this capacitance also less, then better dielectric isolation the devices are isolated P channel and N channel MOSFETs are isolated that is dielectric not PN junction isolation if you go to the bulk thing it is a PN junction isolation N well and P well things in both vertical and.

So, the isolation is both in the vertical direction substrate is isolated and in lateral horizontal direction the latch of free CMOS we discussed that low voltage operation I dint we will understand that; when we go into the analysis of this device that is you can if you if you need low voltage operation low supply voltage you need to have low threshold voltage you will be able to go for low sub threshold voltage if the sub threshold slope is ideal 60 millivolts per decade.

You can never get that in the bulk MOSFET which will be seventy 80 or ninety here you can go right up to 60; 63 millivolts and that of the order in the SOI you cannot get 60 may be 63. So, very close to that that is why you can go to low supply voltages and; that means, low power devices when you want to go for low power integrated circuits in variably you will go for this wider approach ideal sub threshold slopes 60 millivolts per decade.

Now, that we will just continue few things now on this get the summary of summary of what we have discussed now. So far now what is the structure of SOI MOS MOSFET?

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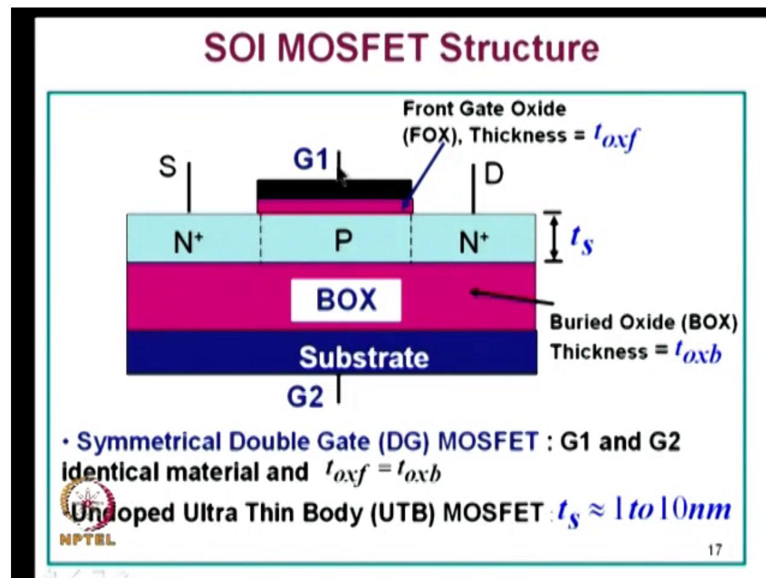

Which quickly see that with there is some few minutes are there we can discuss that we can take on from their next lecture.

So, substrate as shown it is thin, but thick one buried oxide N channel device gate oxide gate notice there are a structure is different from that conventional bulk MOSFET, I can have gate on the top, I can have gate on the water because there is a oxide here, but you will say this oxide can be made thick thin and have good control on that I can make this also thin, but you will lose some of the advantage that you have in the isolation, but we will see that can be overcome by appropriately choosing the structure called pin fact.

In a still thick buried oxide what you can have both top and bottom, it will be not bottom it will be coming on the sides if I have a SOI layer like that. Now we are talking about a gate from here gate from here I have the SOI layer like that I can have the gate like that and I can have thick oxide below. So, gate from this side, this side, this side all around after all. So, that type of structure you can get.

So, understand that before you understand we will just. So, you still can have the thick buried oxide get that type of structure what you are pointing out is you can have more than one gate or wrapped around gate you can have in the case of the this type of thing that is really not conventional structure. Now we can have symmetrical means if I have 2 gates symmetrical means what the work function of G 1 and G 2 are same the thickness of this oxide and this oxide are same that is symmetrical

Dimensions are here and here are the same thing that is symmetrical is anyone of not same we can call nonsymmetrical, but now notice one thing if the; if I do not talk of anything else; I use this as this layer is thick enough; I can have the MOSFET structure with the inversion at the top, I can have the MOSFET structure by applying this bottom gate inversion at the bottom. So, with the same channel length I will have to double the length current from this top gate current from the back gate, but you remembering what is the use of that, but if I have a gate like this, I have wrapped around gate this is the sequence of top gate this is bottom gate this may be thin thickness will be that whatever you got there.

So, you can have current mach more than that and you can keep on reducing the thickness entire layer is inverted see the in inversion layer, we take it as a charge sheet actually there is a charge from the surface you see going down below. Similarly if this gate is not inverted, there is a charge extending in to the bulk this is the thickness is very small the entire layer will be inverted that is called volume inversion you can have bad type of thing there are terrible or terrific advantages tremendous advantages of volume inversion.

We will see that we can get mobility which are very close to ideal value un-doped case you may say make the whole thing un-doped that also you will see how it is see if I have 2 gates here that 2 gates are competing to have control on the channel. So, the gate the drain is prevented from having control on the channel to less extent because these 2 are there from both side coming. So, the short channel effects are definitely reduced here qualitatively

You can have if that is the thing you can have un-doped ultra thin body MOSFETs also those are the different types you have got today we will talk of un-doped layers here we will have very interesting features which we will be discussing now.

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Common types of SOI MOSFET

• Partially Depleted SOI MOSFET

•Fully Depleted MOSFET

Reference:
J.F.Colinge, " Silicon On Insulator Technology:Materials to VLSI" Kluwer Academic Publishers , 1991 (first edition), 1997 (second edition)

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You will have you will have fully depleted or partially depleted MOSFETs see if you go to bulk MOSFETs what happens the thick layer is there only a top gate there is inversion part of it is depleted rest is bulk here part of this layer will be depleted from the front gate part of layer will be depleted on back gate if the both the depletion layer meeting together that is fully depleted.

If not meet together they partially depleted. So, you can have fully depleted or partially depleted partially depleted we will see that operation is same as the bulk MOSFET why part middle region is not depleted only. So, you have entire theory that discussed for the bulk MOSFET top gate is you can discuss and the bottom gate you can discuss add the 2 there is no need of new theory, but if it is fully depleted the entire theory will be different. You have to go into the modified discussions on this particular type of device.

I think, I will get back to those full details of these SOI MOSFET operation theory involved etcetera in the next lecture. So, we have gone through the many advantages that this sort about is there and how to achieve that what are the characteristics of the devices. We will discuss in the next 1 or 2 lectures.