Nanoelectronics: Devices and Materials
Prof. K. N. Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture - 17
Interface state density effects on "S". Short Channel Effects (SCE) and Drain Induced Barrier Lowering (DIBL)

So, we will continue our discussion on the non classical MOSFETs which I explain what it is last in my last lecture.

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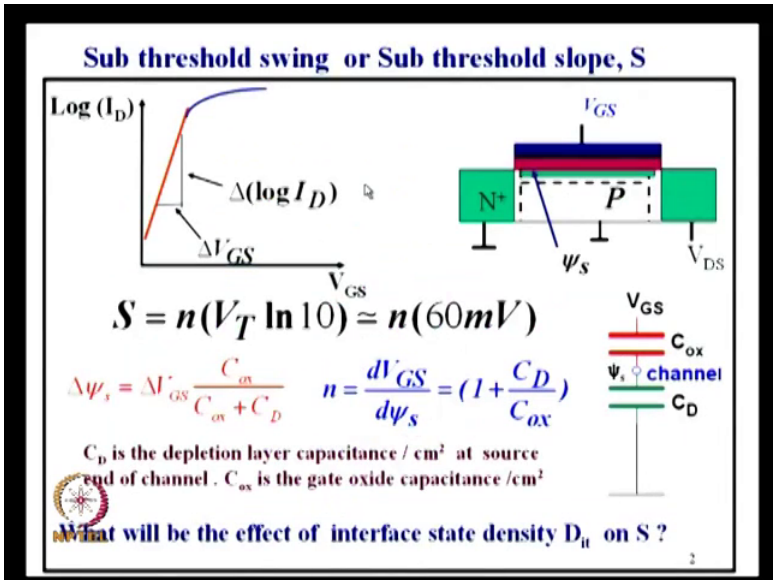

So, this is module 1 continuing on the carrier transport in nano MOSFET. So, we discussed last time just this is a repetition of what I said last time because I am continuing on that so the sub threshold region has an exponential characteristics which already you have heard number of times and on log scale it will be linear and we also saw that a sub threshold slope or sub threshold swing is 60 millivolts into n; 60 millivolts is k t by q long term and we also saw that this n is nothing but an indication of how good is the coupling of the gate with respect to the channel.

If delta V GS is exactly equal to delta psi of S, the coupling is excellent. But because of the sharing of the voltage between the gate oxide and the depletion layer the coupling is not that good. So, what you get will be V GS will be shared between these two and we also wrote since V G, psi S is less than V GS we wrote V GS by n is equal to psi of S. So,

then delta V GS by delta psi of S will be n so that n is actually the coupling factor ratio of these two psi of S and V GS. And from these two capacitances you can see that the voltage or any change in the gate voltage with will result in a change in psi of S decided by the capacitance ratios and that is delta psi of S is equal to delta V GS divided by sum of the 2 capacitors multiplied C oxide there is a standard basic relationship.

So, from here delta V GS by delta psi of S is 1 plus CD by C oxide, where CD is the depletion layer capacitance for centimetre square, I call it centimetre square but per unit area and C oxide is oxide capacitance per unit area. So, you can see that if the depletion layer width is smaller CD will be larger and then n will become larger that is one indication of this sub threshold slope will be much more that is you want n as small as possible ideally one, you will never get one but you will see you can have some special structures where the n can be bought very very close to 1, 1.1 not one like that of that order.

Now we what to see is this is the ideal situation where there are no surface is excellent, but in fact is you have got interface states, interface state density is there between the oxide and silicon particularly if you are talking of high k dielectric, it will be unbearable so you have to see what will be the effect of that.

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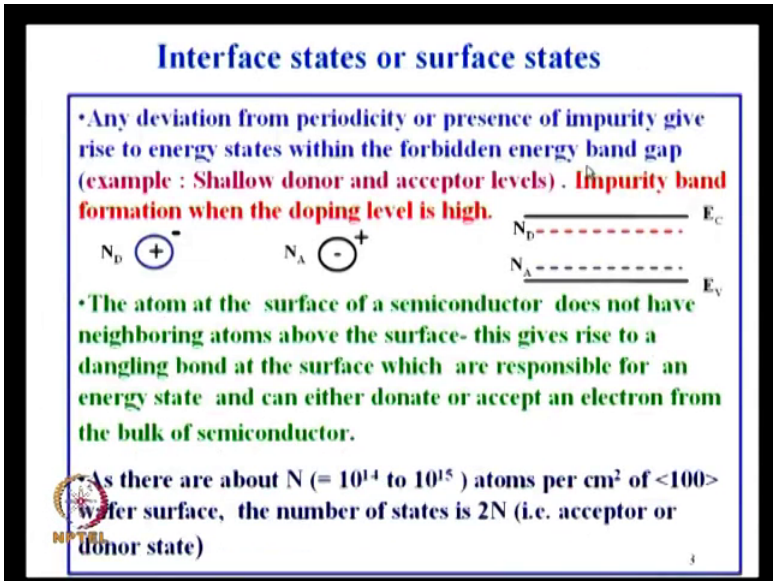

So, just before going into that I thought I will be give a quick glance of what is implied by this surface state density and how it arises I know that was a (Refer Time: 03:55) can

but has already discuss some aspects of this may be some other things which I would like to elucidate I just quickly go through. So if you take a semiconductor, energy band diagram has no states in this between the conduction band and valence band let us say a forbidden band.

Now, any loss of periodicity or presence of any impurity will give rise to levels between the conduction band and the valance band. So, to give you a very good example of that donors, donor is a fifth group element which has one valance electron which I shown here and the core is plus charge and this one valence electron is a fifth electron of the fifth group which will be revolving around that which is very loosely bound.

So, you can give even if you give very very small energy even at room temperature this electron can be raised removed away from this parent atom and you can go to the conduction band. So when you put the energy level here corresponding to donor level a shallow level implication is you can give you can raise the electrons from this donor level to the conduction band with very smaller energy some 50 milli electron volts for that is called shallow donor ok that is why put it near the conduction band I have a why I am going through this is because we want to see what happens in interface state density. If you take acceptor, see here the donor is the core is plus if you remove the electrons from there is positively charged, acceptor the core is negative there is a site where plus charges can it can look into as a vacancy you can assume that there is a plus charge so that whole thing as it is a neutral.

So, if this plus charge is removed from there that is how can it be removed by accepting an electron from the valence band that plus charge is neutralized, so you will get negative charge, so here you donate electrons, here you donate plus the donate plus charge and this donative plus charge by taking electrons in the valence band. So, when it accepts an electron this is plus charge it counts with negative charge so that is what we to put it once more if the electron is occupying the donor level it is neutral, if the electron is occupying the acceptor level it is negatively charged, because the plus charge is not there that is the thing to understand to understand the interface density and its impact.

Now, let us see what is the so these are the shallow donor or the shallow acceptor implying very small energies are required for interaction between the donor level and conduction band and the acceptor level and the valance band.

Now if you take a surface I take this surface this is the bulk, this is on the surface if I take the atoms are in surface from semiconductor, atom does not have neighbouring atoms. Usually, in the bulk of the silicon the atom is surrounded by 4 neighbouring atoms, so all the bonds are continuous it is stably staying there. The atom on the surface has got 2 on the side, 2 on below it is a very qualitative description, but the there is no atom on the top surface. So, above the surface there are no atoms so there is an electron which is not forming the bond completely.

So there is a possibility that you can knock out that electron and take it into the semiconductor make it available for conduction if possible, so that means that silicon atom on the surface can act as a donor if you donates the electron. Now what will where we will locate this energy level is a question, see the shallow donor the electrons can be knocked out with very small energy, so you locate it very close to conduction band.

Now let me ask you if you have if you knock out the electron from the valance band that is the electrons from the bond you have to apply volt energy equal to 1.1 electron volts, that is why the conduction band, valence band is difference but if the silicon which is on surface from there if you want to knock out electrons you may not be required as much as and you have this required for the electron band gap, but it will not be as small as what we required for this pentavalent material.

So, it is actually this level corresponding to this donor will be very close to valance band, it will not that the near the conduction band implying it will require large energy much more large energy than the shallow donors. They are called deep donors which are far away from the conduction band. Similarly you can argue out that for the valance or the acceptor type, deep levels can be on the upper band from the same argument. So, why I am bringing out donor and acceptor is the surface atom can either donate an electron or it can take an electron to complete another bond.

So, it can act as a donor or acceptor if it is acting as a donor that donor level can be located with near close to valance band somewhere in between the mid gap and the valance band. The acceptor level on the same argument will be on the upper half of the band gap or closer to conduction band. Now one more thing that I want to point out is there are about 10 to the power of 14 to 10 to the power of 15 atoms per centimetre square in silicon that means large number of atoms are there.

Now let us go back to the shallow donor or shallow acceptor theory. If there is shallow donor you do not put that donor level as continuous level you put it by dotted lines what is the implication of that the implication is very simple it is very dilute in silicon, the number of atoms per centimetre cubed in silicon; silicon atoms are about 5 times in 10 to the power 22.

Now, the donors which are there in dopants when you dope them are 10 to the power of 18, 19, 20 about if a 10 to the power 16,17 etcetera it is very very dilute out of 10 to the power 22 atoms from silicon that are 10 to the power 16 or 17. So, these 2 atoms do not see each other see the conduction band was at band of levels why it was interaction of the energy levels of the 2 silicon atom. How the interaction comes up the spacing between the atoms is very very small from 5 angstrom so break it that is why these from Pauli's exclusion principle you can say that no 2 energy levels can be at the same level corresponding that so its splits up.

Similarly, if the donor level now you put it dotted lines saying that it is not interacting these with that they are isolated from each other. Now if you raise the donor levels donor, concentration to about 10 to the power of 20, 10 to the power of 18, 19, 20 and all that then number of atoms are very large and number of divisions between the atoms donor atoms is reduced there can be interaction between the wave function of these 2 atoms; that means, the 2 electrons trying to occupy the same energy level, but they are not able to occupy the same energy level this split up. So, this donor level which you put it has donor level, one level with no longer there will be 1 level, it will split up into a band of energy it is split up band of energy and can even merge with the conduction band.

Similarly, the p acceptor levels also can split up into a band, so now going back to this theory of surface states you would have seen already now I argued out that if there is one atom and there will be one acceptor level and one donor level it can go either way it is import array. For example, if you put gold into silicon it has one single electron, valance electron it can either donate or accept. So, in the same way surface states electrons can go and occupy or it can donate that electronic it is available there. So, now that is one atom has got to one acceptor one level and one donor level and we said donor level will be below and acceptor level will be up because of we argued it out. Here donor level is up acceptor level is below there, deep levels will have donor level is down, acceptor level will be up.

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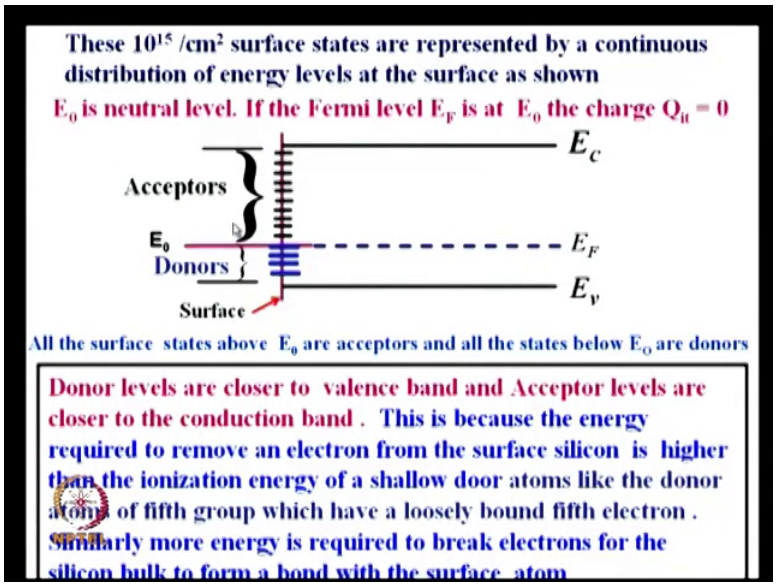

Now if there are large number of the surface atoms like this each of those donor levels will split up into a band these donor levels are below. Each of those acceptor states is split into a band so that is why you put these acceptor states closer to the in the upper half or nearer the or above and donor levels below and all of them are not to one levels, several levels split up at band of energy levels, because large number of surface atoms are present. Each one of those surface atoms correspond to one level here, one level here.

Now other thing that you would see here is these acceptor level will be actually occupying from top to bottom completely, fed out that when you come down here there are large number of donor atoms which are compensating that. So we can say that predominantly there are acceptor levels up to a point, predominantly there are donor levels in this region between the level called E naught and E V they are are all donors , between level E naught and E c they are all acceptors, I hope that is understood.

Now this argument whatever I discussed about here, what is this charge state of these see so I am not showing the intentionally doped shallow donors and the hallow acceptors, this particular material if I put the Fermi level here. What does it mean it is a P type material and I have taken the doping such that the Fermi level actually coincides with the E naught level which separates the acceptor level and a donor levels. So, this E naught level is called the neutral level.

Why it is called neutral level? In this particular case which I have shown the Fermi level is coinciding with the neutral level through with the level E naught, what is the meaning of that what is the charge state of these acceptors from the definition of Fermi level if you recall all the levels below the Fermi level are mostly occupied, the levels above that are not occupied mostly.

In fact if you go to the 0 degree Kelvin all the levels below the Fermi level are occupied all the levels are empty, but at room temperature if you go slightly deviation will be there. But for qualitative understanding you can say no almost all the levels are occupied below all the levels are not occupied, so if you take that abrupt model for the Fermi level distribution these are all not occupied.

Now go back to what I mentioned all the donor levels are occupied because they are below the Fermi level. So, what is the charge sheet of that just go to this and see they are occupied means it is neutral. So, these levels are neutral because they are all occupied and the acceptor levels are not occupied by electrons which means that is neutral, if it is occupied it is negatively charged.

So, in this case you call this as neutral level because if the Fermi level is coinciding with that level the levels below that which are donors are occupied so it is neutral, levels above that in what which are acceptors are not occupied so that neutral so charge net charge on the surface is 0, so energy band electrons will be flat. Now let us go further down I am going bit slow because this is very though you had gone to some of these things is quickly, I will see go through that.

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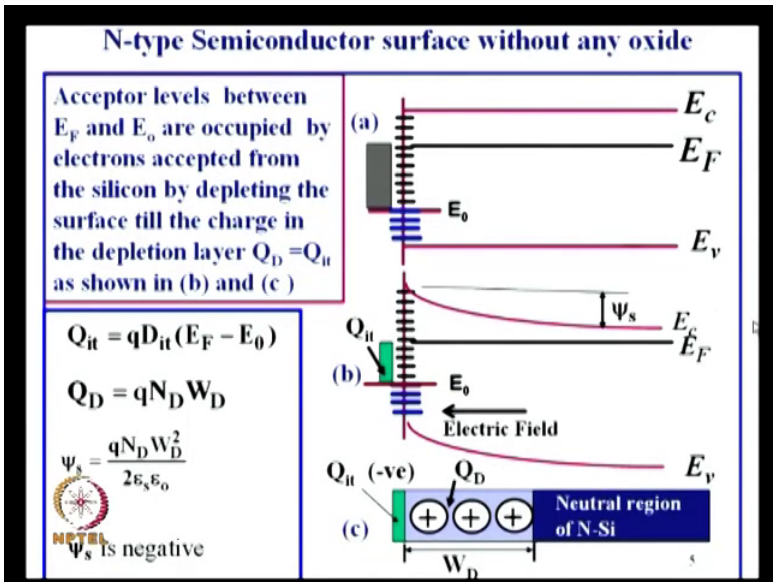

Now I will take a situation where see here it was a situation where it is a P type, Fermi level doping adjusted, bulk doping adjusted such that Fermi level is coinciding with the E naught. Now I go to a N type material doping something is like 10 to the power 15, or 16 Fermi level close to the conduction band decided by the shallow donors. Now surface is free there are no oxides, there are very large density of states.

So, if it is like this all the if I draw the energy band as like this. Now all the levels below E F are occupied what will be a charge sheet of this, take a look at these levels below E naught, they are are donors they are occupied. So, the charge there is 0, donors charge is occupied if it is donated, it is plus charge it has not donated electronics are occupying it is neutral and these are acceptors electron is occupy that mean electrons, it has accepted electrons that means, it is negatively charged.

So, on the surface of the semiconductor there will be net negative charge, donors are donating acceptors, acceptors where I say this electron comes from that is comes from semiconductor that means, this N type silicon removed some of this electrons from the nearby region from surface and given it to this acceptors donated which means the surface the region nearer the surface will be depleted of donors.

See these are the donors plus charges this is a depletion layer the electrons from here have gone to this surface, surface is negatively charged and there are donors which are positively charged. So, once there is depletion layer like this electric field is in that

direction. So, what happens in the 2 energy band diagram I hope you are familiar about energy band diagram, so electric field is in this direction that means, the band bending takes place, see is if there is the electric field band energy band diagram is flat.

Wherever there is a depletion layer there is an electric field and the energy band diagram will bend like this so, up to this point there will be a band bending and see the electric field is in this direction, energy band diagram will bend upwards like that. How do you figure out that when a electric field is like this you have to spend energy it will take electrons from here to here. So, if the electron is here it is at a higher energy level that why energy band diagram will bend here that is why I have drawn like this.

Now that is a very some important thing that you have to understand here before we go next into the argument on some of these things is what happened see there because of this band diagram because of the electric field there is a potential drop from here to here that means this is neutral surface there is a potential equal to psi of S from here to here if you go there it is a potential which is negative with respect to this point that is psi of S that is surface of potential.

Potential of surface with respect to neutral region and that potential is actually equal to the voltage drop across the depletion layer which you know is on the first order theory q N D W D squared by twice epsilon S and epsilon 0, that is well known thing. Now charge in this region is N D is number per centimetre cube and computing charge per centimetre square, so first centimetre cubed if it is centi cubed multiplied by W, I get total number of charged per centimetre per square into q. Now what will be a charge on the surface now that we will come back after discussing one particular point here, I mentioned that the energy band diagram will bend.

What will be the state of affairs for the Fermi level? Fermi level here was decided by the donors concentration in the bulk. So, in this region where it is neutral the energy between the conduction band and the Fermi level remains the same as before it does not change, but as you move to the surface because it is depleted it becomes less N type electrons have been donated that means the Fermi level will be further away from this point. Two point, here the Fermi level is decided by the doping concentration, here the Fermi level difference between the conduction band and Fermi level depends upon how much band

bending is taken place, it is less N type here you can think about that less N type means Fermi level distance between these two will be larger.

Other point that you must notice the Fermi level is horizontal it is not bending you recall some of the discussions or earlier models the Fermi level will be continuous, there will not be any deflection or deformation in the permissible Fermi level if there is no current flow it is a thermal equilibrium situation there is no current flow so that is why E F is constant. So, all that happen is band bending takes place upwards, this remains constant. What happens to neutral level, see if you go back to this the neutral level is assigned is fixed for a given material if you take silicon the neutral level is one-third of the band gap here.

If this is the band gap energy E g this is E g by 3 it depends upon the particular material. If you take silicon it is about E g by 3 that is E naught minus E F, if you take gallium arsenide it is also almost that if you take germanium it is very very close to valance band. In fact 0.66 electron volt energy is the band gap of germanium and E naught E V will be 0.06 electron volts very close valance band depends upon the material let me not get you to that details of that we will locked in that otherwise.

So, the location of E naught with respect to EV is fixed EV or EC is fixed, so if there is band bending taking place like that on this band bending has taken here Fermi level has the gap as changed from here but the location of E naught with respect to valence band is same on the surface which would mean see if towards like this here because of the charge transferred from the semiconductor to the interface the Fermi level has this has moved up.

So the distance between the Fermi level and the E naught has reduced on the surface so the band bending is such that charge here is equal to the depletion layer charge. So all these discussions is to go into what happens further this is N type please remember it moves it always moves closer to the interval so that the charge here is equal to charge in semi in semi conductor.

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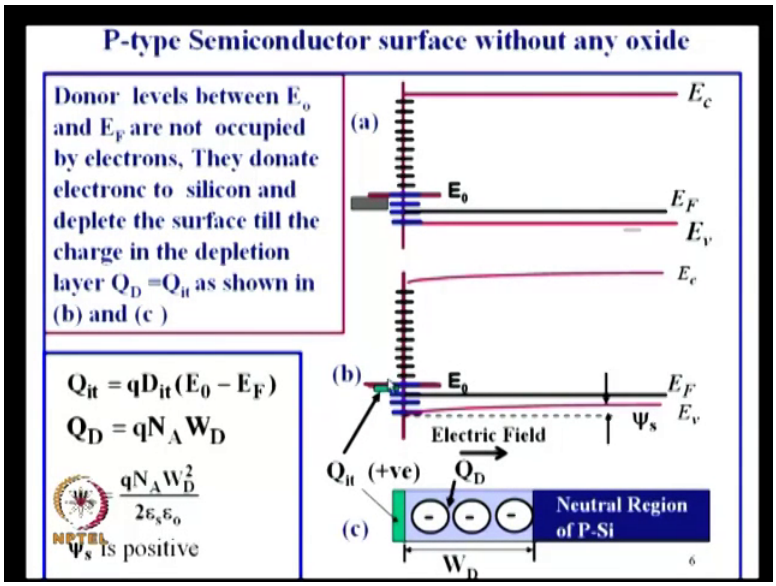

See the other case of P type where if the Fermi level is below the E naught, what would happen these are in neutral level is above the Fermi level. Now, the levels below the neutral level are donors that means, these donor levels what happened to these donor levels, above the Fermi levels here they are Fermi level so you can see donor levels between E naught and E F are not occupied, levels above E F are not occupied.

So, these donor levels would have donated electrons to this P type material, so P type region if it is made negative it will be depleted plus charges see donor electrons have gone and neutralized the P type plus charges so there will be depleted layer. In the previous case N type as depleted it is P type as depleted, so you get depletion layer once it is depleted because it has donated electrons surface is positive and this is negative and electric field in this direction you can see band diagram is up like that to the right because fields is in that direction.

So, ultimately you can see that the band bending takes place and the voltage drop in the depletion area is such that net charge in the surface that is equal to charge in this depletion layer.

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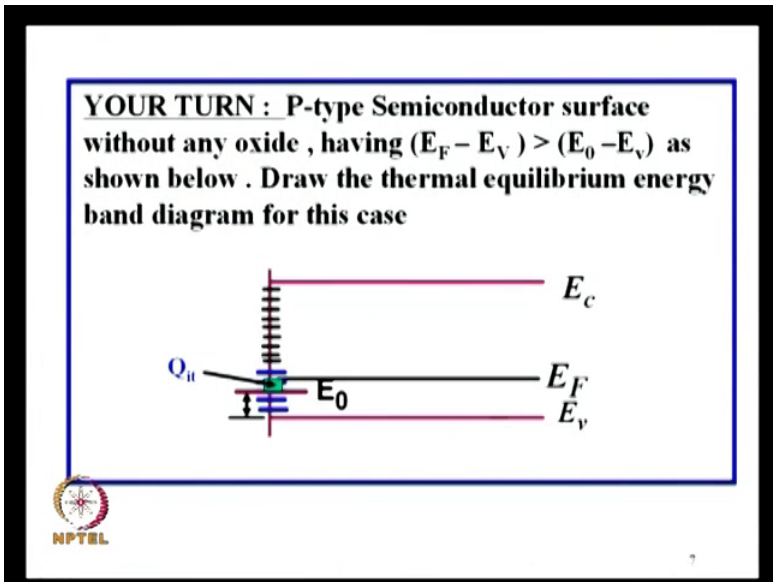

This I will give one more instance which I will not discuss this you at your leisure time, you think of that what will happen this is not equilibrium situation. If there are surface states were not there I have a situation where Fermi level is above the E naught that in these are the acceptor states which are occupied there. What way the energy band diagram will be bend? What will happen to the semiconductor surface that I think I let you to discuss when you go back?

In fact, what will have to realizes is the levels below the Fermi level are occupied that means these acceptor levels are occupied that means it has taken electrons from the semiconductor that means, it has given more holes to the semiconductor that means it will become more P type in the semiconductor. If it has become more P type in the semiconductor the Fermi level moved and there are surface is move closer to the valance band. More P type means Fermi level will be closer so here it will be bending like that, you will have an accumulation layer, Fermi level will be flat but this will bend if a Fermi level and valence electrons are closer together it is not the Fermi level it bends it is the valence electron valence band which moves up. So, you will have accumulation layer that you discuss I just ah give a hint on that it will go to accumulation, but please understand that it is not Fermi level bands it is the either the it is the conduction band and valence band which bends. If the valance band bends more close to the Fermi level, it is accumulation it moves away from the Fermi level that is depletion in the P type material.

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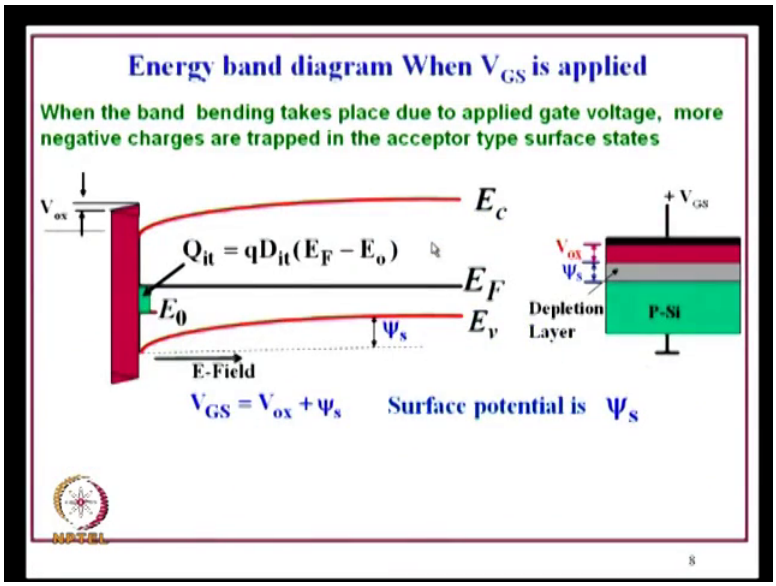

Now, get down to the I think I have taken look quite a bit of time on this particular thing, but I and long running we will see it is for it is for us to analyze any situation. So, now I will take a situation where I apply voltage these particular case that I discussed was Fermi there are no volt oxide, there are no voltage applied. Now when I apply and I oxidize it then many of those interface states will be removed reduced surface states will be reduced, now when you have but still some surface states is there depending from whether it is thermal oxide high K dielectric. Now when I apply voltage plus here it is getting shared within the oxide and silicon even when though there is no interface state. So, V oxide you can see now electric field is in that direction from the surface metal to the interior.

So, wherever this plus to minus if you go plus to minus energy band diagram will be like that because it difficult for electrons to move to the minus direction. So, you can see the energy band diagram bends up there is voltage drop in the oxide, you will see quietly in textbook they have put the diagram here going up like that imply there is voltage drop across the oxide in that direction and semiconductor here also bends like this, because plus on the left hand side I am sorry plus on the left hand side plus minus V oxide and then plus minus V silicon.

And what is V silicon, instead calling V silicon, it is history physics people always call it as psi, we call it as V silicon (Refer Time: 29:33) silicon, so they call it as psi of S,

surface potential is nothing but the potential of surface is with respect to the neutral region. So, see this diagram now you can see the E F in the bulk interior here neutral region here is decided by the doping P type material doped, how much doping that decide the this distance.

Now on the surface the distance between the E F and the valence band edge is more than this one because it has got depleted and is a depleted you can a very casual way of telling is it is less p type. Because the depletion is not abrupt, it becomes less and less holes are present, very few holes are represent here who are less p type. So, the distance between the Fermi level and this increases.

But the neutral level location is always fixed with respect valance band edge, silicon this E g by 3. So, how much charge in this interface state density is present depends upon how much is the distance between E F and E naught is, how much is the distance between these two it depends upon, how much is this E F and how much is this psi of S total thing. See I have here only the E F minus E V. Now here E F minus E V will include this psi of S and that E naught that distance.

So, the charge here will be how much will be the charge here, will it be negative or positive? Because these is the neutral level not confused to that is the band bending and E naught is below the Fermi level, so these levels which are above E naught and within that Fermi level are acceptors they are occupied, there is negative charge and what will be the charge in the depletion layer that is negative the P type depleted negative. So, there will be negative charge here, there is negative charge in this surface both are negative. If there were no interface state density state density the to all the charge would have been in the depletion layer, now part of it goes into this is occupied by this. So, whatever the charge in the gate oxide is present is shared by this interface state that q D it a D it defined as number of states per centimetre square per electron volt.

I hope you don't know about that because I did not mention about that D it implies how many states are there number per centimetre square per electron volt. So D it if it is uniform throughout this distance E F minus E V is the energy, per electron volt there are D it number per centimetre square and energy gap is difference between the two is E F minus E V.

So, if you I don't know whether I am pointed out there it is left off, but here D it number into number of levels you see total number a charges occupied q gives me the charge. So, q D it into the difference that gives me the charge, now that is not equal to depletion layer charge because this charge negative charge corresponding plus charges here on the gate oxide and there are depletion layer charges which corresponds to this band bending corresponding to how much is the depletion layer width q N a into the depletion layer, but that is a number of charges per centimetre square in the depletion layer. All that you are knowing that the charge here preside by the D it and the gap between the two that negative and the discharge in the depletion layer.

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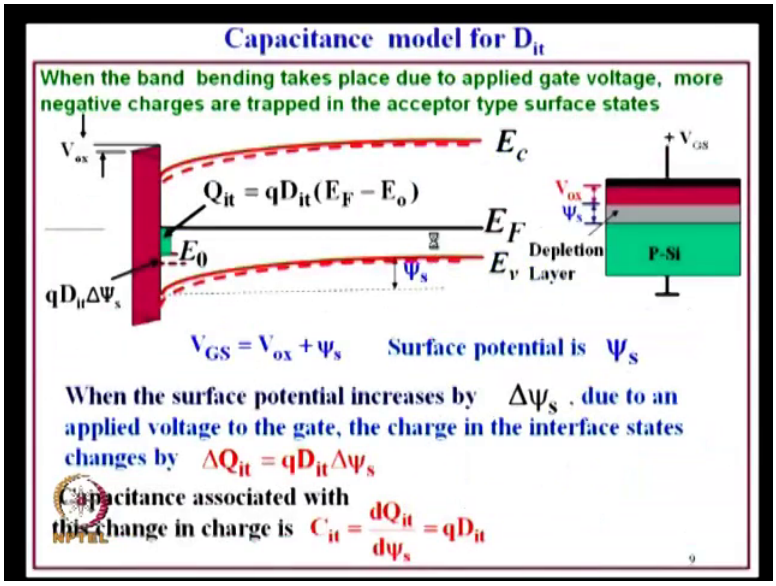

Now if that gate voltage is changed by delta V G, that delta V G will be shared between the oxide and also psi of S that diagram we have drawn here. I have increased that V G by delta V G. So, due to that there will be delta V oxide addition what so voltage drop delta psi of S, silicon voltage drop changes by delta V silicon or delta psi of S.

Fermi level does not change, but this band bending because which was originally solid slightly gets bend more by amount equal to delta psi of S, corresponding to extra drop across the silicon, conduction band bends down, valence band bends down by additional delta psi of S. Now watch very carefully Fermi level has not shifted that remains with respect to neutral position same it is flat, but the neutral level what was here I shifted down by an amount equal to how much this conduction band has moved on both

conduction band and valence band moved together like that, it has deflected by an amount equal to delta psi of S, so if that I depleted by delta of S the E naught moves by an amount equal to delta psi of S.

Because E naught is always defined with respect to the valence band edge or conduction band edge both are same in the sense if I in order to avoid confusion I will say E naught in the case of silicon is one-third of E G. So, earlier with respect to the valance band it was here one-third E G above that, now the band bending the valence band as shift moved down that delta psi of s that means, this level has moved from here to here by an amount equal to delta psi of S. Because when the valence band edge has moved by delta psi of S, this level also would I have moved down by delta psi of S because it is written with respect to valance band edge, so this has moved with respect to this band delta psi of S.

What happens with charge on the surface? Originally, but the Fermi level has not moved because that is there fixed with respect to the bulk itself so there will be additional charge coming because this neutral level has moved down further down with respect to the Fermi level and how much it has moved as delta psi of S. So what is the charge now extra charge coming from the interface state density q D it, number of levels multiplied by this shift in that extra charges coming out because due to this shift. So, you will have extra charges coming from the interface state density equal to q D it into delta psi of S and because the delta psi of S is an additional drop in silicon depletion layer width would have moved by an amount equal corresponding amount.

So, there will be additional charge in the depletion layer width. So, there are 2 things happening because delta q in the gate you have increased delta q in the interface state density has increased by this amount q D it into the shift in this position delta psi of S, and the charge here accepted by whatever original charge was there by delta q D. Now let us see I can define a capacitance corresponding to this always you remember delta Q by delta V is the capacitance and delta V is the voltage which changes.

So, here the voltage changes is the psi of S, so when psi of S changes by delta psi of S the charge changes by delta Q it which is given by q D it into delta psi of S. So, you can think of it as a capacitance in the equivalent circuit as circuit as C it which is delta Q it by delta psi of S, which is q D it, it is a constant because we assume that the q D it is

same everywhere across the band gap. So, you can write C it which think (Refer Time: 38:26) but that already pointed out in some in a different manner maybe is delta Q it by delta psi of S.

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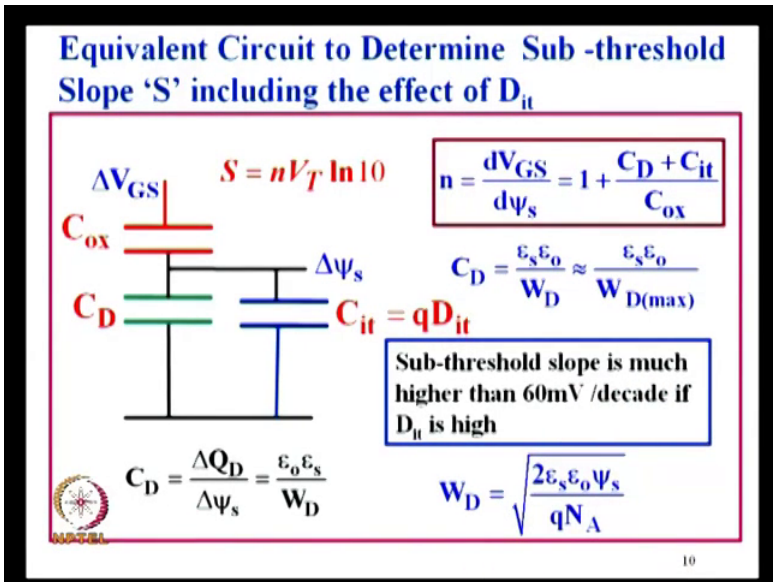

Now what will happen originally interface state density was equal to 0, we found out the sub threshold slope S equal to n V t lon 10 and n was equal to 1 plus C D by C oxide. Now when you change the delta V G the charge change was only across the C D because of the widening of depletion layer.

But now because of this change in the potential here not only the charge in the depletion layer changes, charge in the interface state density also changes that gives rise to an additional capacitance which you put across this. So, delta V GS by delta psi of S, now instead of 1 plus C D by C oxide you have got 1 plus that affective capacitance which is sum of C D plus C it, so you have got sub threshold slope now given by 1 plus 50 milli volts into and there is 1 plus C D by C it by C oxide, so what I am trying to point out here is I did not want that to come there.

What we are trying to point out here is the interface state density will increase the sub threshold slope if you go back and see when you face sub threshold slope this is 1, 50 millivolts per decade that is this will be 50 millivolts and the current changes by 1 decade that is if n is equal to 1 ideal case, now if there is no interface state density it may not be 50 millivolts it may be 70 millivolts. But if there is addition interface state density

you will have additional capacitance C it that will not be 70 millivolts, it may be eighty millivolts 90 millivolts, 100, 120 depending upon how much is your C it.

How much is your C it depends up on the D it and D it depends upon the quality of oxide, in the case of thermal oxide the D it can be very low people both stop even as low as about close to 10 to the power of 10 percent metre square per electron volt. But in the case of high K dielectric it can go to 10 to the power of 11, 10 to the power 12, unless you use the additional persuasion techniques, this please remember that this will be very important parameter when you go to non classical non silicon Fets.

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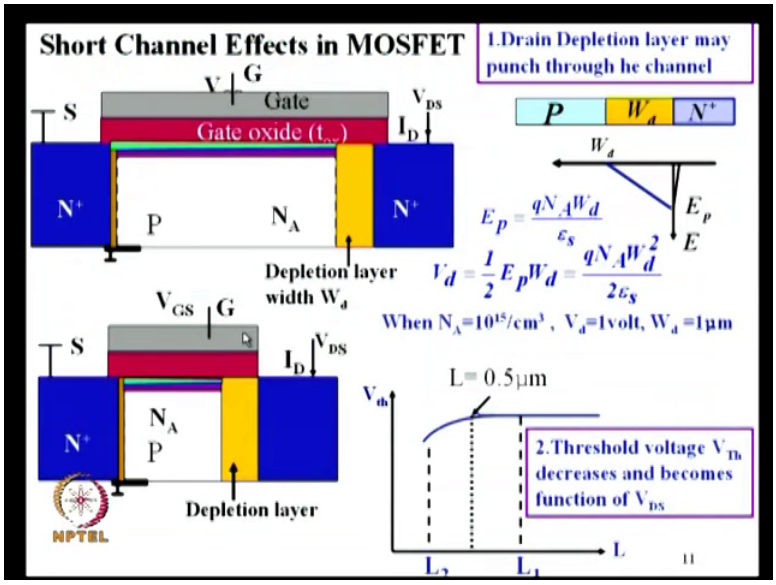

Now a quickly run through some of the things before I go into some more details this is being done thoroughly by processor now (Refer Time: 41:45) that is short channel effects I have only one slide with just completed just for the sake of completion. When the channel length becomes small you can see the depletion layer on over drain region can encroach into the channel in the convention structure.

So, the width of the depletion layer depends upon how much is the total voltage across the drain is total voltage is V V I plus applied voltage I called it has V d that is equal to q N a W squared by this is the standard formula. So, depending upon the voltage you have got the depletion layer width for example, if I have 1 volt, total voltage then doping is 10 to the power of 15 per centimetre square to give an idea depletion width will be 1 microns. So, if I have a channel length of one micrometers, the whole channel will be

depleted of carriers which would mean that the entire channel is dominated by the effect of the drain and the gate has no control.

So, you want to make it you increase the doping concentration to do that is why you go to 10 to the power 16, 10 to the power 17, but you know that as other percussions like reduced mobility and increase the threshold voltage so you reduce the gate oxide thickness all those things are there, now so that is if the channel length is 0.1 micron, even if you go to higher doping concentration so it can deplete all the way or at least partially therefore, I will not get into that discussion due to that charge be taken care of by the drain you will be able to invert the channel with lower gate voltage that is the threshold voltage will be lower that is one of the short channel effect which I am not getting down for detailed discussion.

So one is punch through depletion region, other one is the because of the depletion layer occupying the channel here this charge does not belong to the gate but to the drain therefore you get you can invert the channel with lower gate voltage that is the threshold voltage gets reduced that is another short channel effect. Both the things can be reduced by increase the doping of the substrate.

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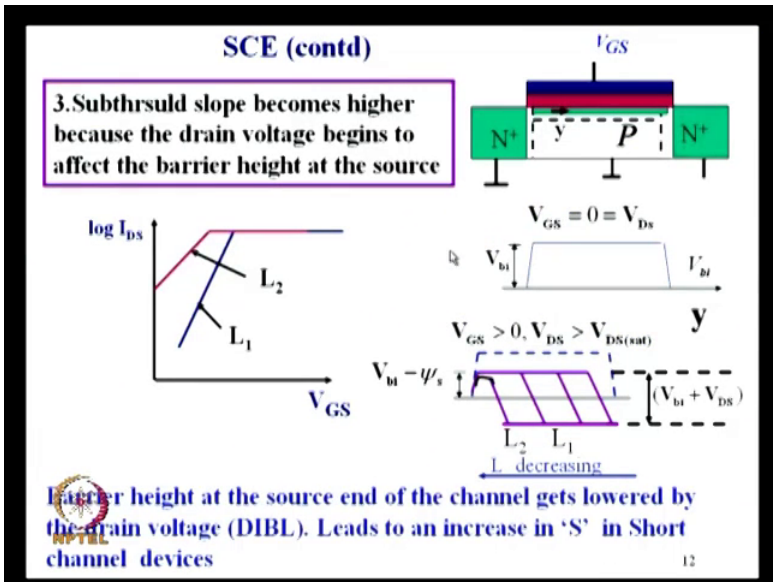

Now, I just wanted to bring in this the other effected during induced barrier lower this also have been discussed, I just drawing what happens here in the sub threshold region. In the sub threshold region there is no drop across the channel because the carrier there is

no drift current. So, potentially if you see V bi no drop V bi when you apply voltage to the gate below threshold what happens to the barrier height it gets reduced. Because plus voltage apply plus minus plus minus so these three gets forward biased so V bi gets reduced. If the depletion layer width is only here the first curve here you will have a reduced barrier height from V bi by psi of S flat there and going like this so this barrier height reduction is completely controlled by the gate.

Now if that depletion layer occupies a good portion of the channel shorter channel and which was shorter channel I will say lower doping, this is the depletion layer width encroaching see this edge of the depletion layer here the depletion layer edge is here if we increase the voltage, if I increase the voltage is here if I increase further if it is reaching very close to the source end it is merges it will reduce it the barrier height here completely.

So, what was getting reduced by psi of S by V GS gate voltage now will be a combined effect of the gate voltage and also drain voltage which would mean the reduction in this barrier height which gives rise to your current is controlled by gate and also the drain so the gate loses it does not have complete control over this reduction part of it is care of by the drain region, so if I that means if I change the gate voltage now it suppose it was changing by 60 millivolts per decade it was changing by 0.1 volt it was changing.

When I change the gate voltage now by 0.15 volts the psi S will not change the 0.15 volts because part of the change takes by drain, so because of the combined effect gate will not be if you reduce the gate voltage from the threshold voltage if your gate has got a good control it comes on the 60 millivolts per decade in ideal case. But because of the short channel effect threshold will take as got reduced that is why I have drawn it here gate has lost control because the drain also controls that barrier reduction. So, the reduction in the current is not as much as you get in this case.

So, the sub threshold slope will not be 60 millivolts, it will be worse than that if it were earlier let us say 90 millivolts per decade in the shorts channel it may be 100 millivolts per decade, or 120 millivolts per decade depending upon how much is the encroachment. So, these are overcome by this encroachment can be practically reduced in percentage devices by providing a lightly doped region in the n plus region called extended drain

region. So this is not so important, but I just pointed out this for continuity, now for continuity I pointed it out.

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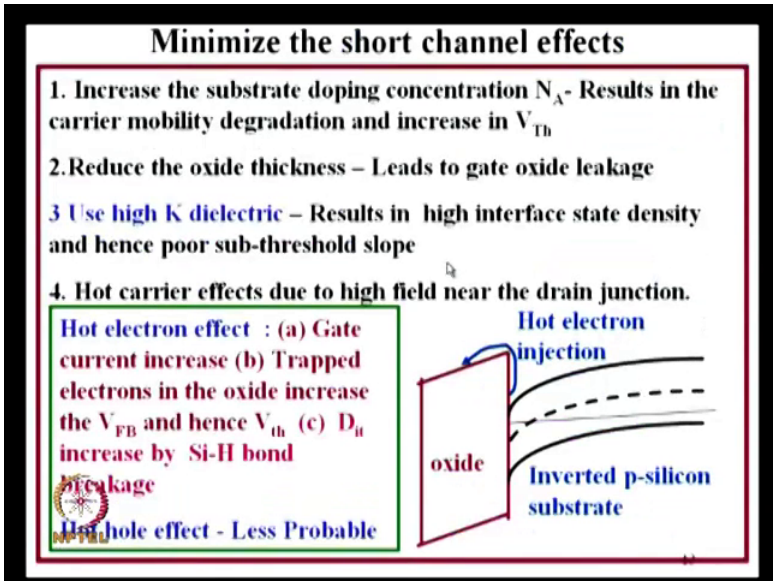

Now, the last 1 that I wanted to say here is the sum up short channel effects I know that I am re doing stating what was done earlier, you need to increase substrate doping concentration to reduce the short channel effects that results in carrier mobility degradation and increase in threshold voltage. To reduce you have to reduced the oxide thickness to overcome this effect but this of course, leads to get leakage current when you go to nanometer level.

But to overcome that we have discussed already that high K dielectric is used, but when you use high K dielectric you know that there are a lot of interface state density effects, so we encounter those effects so you need transform passivation techniques also done there. Now when you also use high K dielectric you must ensure that this energy between the conduction band of silicon and the conduction band of the dielectric must be high enough, if it is not high enough the electrons which are here can climbed up here get into the dielectric.

In the case of silicon they do get into that region when you go to large voltages large electric fields, but today you don't have to worry much about that in the case of silicon because you talk of low voltages so fields are not that high or a velocity energies are not that high energy is q into V, V is small energy core not that high. So but still if this height

may not sufficiently large you can have electrons injected into this dielectric you can consider them as hot electrons and once they are injected into the dielectric, they can act as additional trapped in the dielectric that can change threshold voltage, that can change give us to reliability problems.

So, what you have to take care when you go for dielectric materials is not only that it has could have good band gap it must also have this gap between the conduction band and that there is the chi you know this depends upon how much is the distance between this conduction band of the dielectric and let us say the 0 level, there is a 0 level is there between that and this how much is the gap how much is the gap between the conduction band and the 0 level, silicon it is 4.05 electron volts and you in the case of oxide this gap is 3.3 electron volts, if the gap is 4.05 that is 0 level and this gap is 4.05 minus 3.5 electron volts so this gap is more.

Supposing this is also 4.05, this is 4.05 band gap may be large, but the inverter electrons can get passed through the oxide there will be gate current and or they can get trapped in the oxide. These are some of things one has to remember and when one gets into when one things here thinks of going to high K dielectrics.

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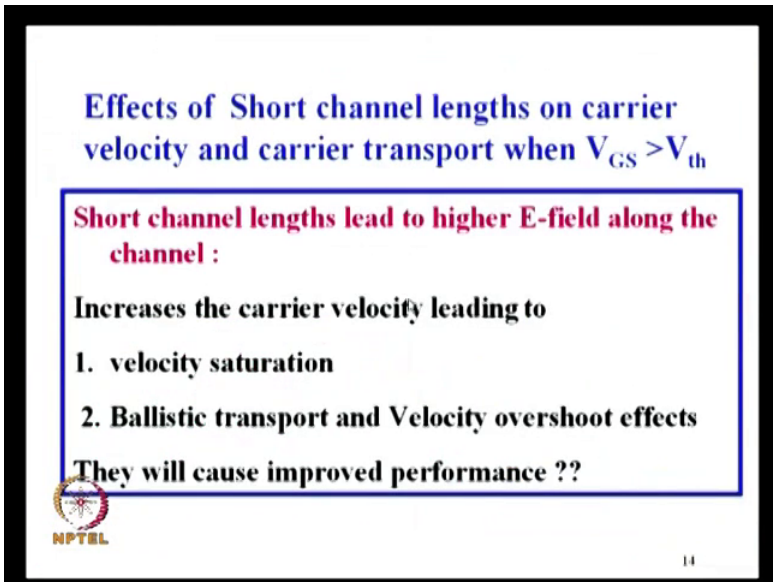

Now the effects of short channel I just come to very close to en of the thing there is there are different effects coming up. How elements I get some elements, I will just at least

few things I will do now so this is the one which I want to discuss one more detail I need one more session on this, but I will just get into at least what is this meaning.

You remember in the beginning itself we said the first order theory of MOSFET we assume that Ohms law holds good, when we said Ohms law holds good we said V is equal to I into r which again means that the velocity or carrier will proportional to electric field, velocity is equal to mobility into electric field.

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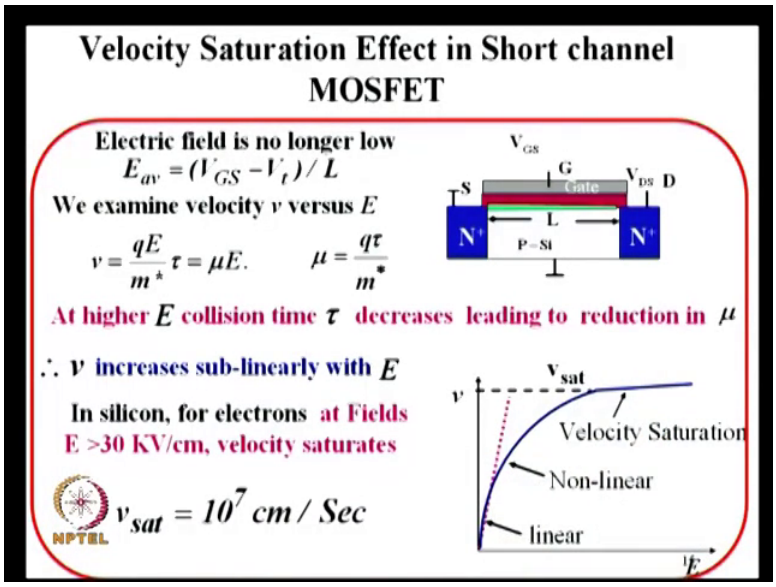

Now if you take a look at the silicon, MOSFET or any other MOSFET for example that is the way the charge distribution is charge is more here, charge is less that because of voltage drop across the channel and because of that because the because of this change in charge you also remember you wrote the current is I D is equal to q into V, q is charged per centimetre square, when you when you move from the source with a drain we took q is varying, we took velocity is equal to mu into V electric field that way we derived the equation.

Now you take a look at this when you move from here to here q is falling what would happen to the velocity, current is q charge into q into q N into V, N is decreasing velocity must increase. So, if I am saying V is equal to mobility into electric field what happens to electric field, mobility is constant if I take electric field is increasing. So, what you say is as I move from here to here evidently the electric field is not constant, electric field is increasing.

Now what will be the electric field if I take an average electric field, you can say that what is the drop across the channel and it is opened here the channel potential is V GS minus V threshold be in the threshold so that divided by channel length is the electric field.

So, average field depends upon how much is the voltage drop across the channel, average voltage drop, so average voltage drop is on this channel drop this V GS minus V threshold is we saw after saturation so that is the average field. Now let us see what happens to as with keep on reducing the channel length for a given threshold voltage, average electric field actually for a given threshold voltage let us say this is not changing, for shorter the channel length more is the electric field average electric field.

Even at the centre to take the average electric field everywhere it will be high, if it is varying then the high electric field. So, what happens when the electric field is high can you take mobility is equal to or mobility is constant can we take. What is velocity? If the velocity, is actually force divided by the mass that is acceleration into time so acceleration to time so as the electron is accelerated it experiences collisions that is you gets scattered.

So, at that when the collision takes place it comes back to rest it accelerates collides it accelerates collides so the velocity the average velocity we can put it as the force there is for this acceleration there is force divided by mass the force of q into E average field but in collisions divided by mass into the time of collision so that is called mobility to access electric field.

Now but the electric field goes up acceleration goes up, so time between the collisions decreases so if the time between the collisions decreases q tau by m decreases. So, when you write mu here q tau by m is a mobility so you have got the mobility which you assumed constant is no longer constant it decreases as the electric field increases because the tau falls or the put it in simple terms if I plot velocity versus electric field, the velocity because of reduction in the collision time for an average electric field the velocity does not increase linearly with the electric field it goes on increasing rather like that and saturates.

So, I will not go beyond that this saturation why it comes we will just discuss very briefly next time. So, today I will stop that ultimate velocity of the electrons is limited by

the saturation velocity so that velocity is about 10 to the power 7 per centimetre per second powers silicon and also even for gallium arsenide and also for many materials and the electric field at which it saturates is about 30 kilovolts per centimetre. So, with that I think we will close down today we will discuss more details in my next presentation all these aspects starting from this slide.

Thank you.