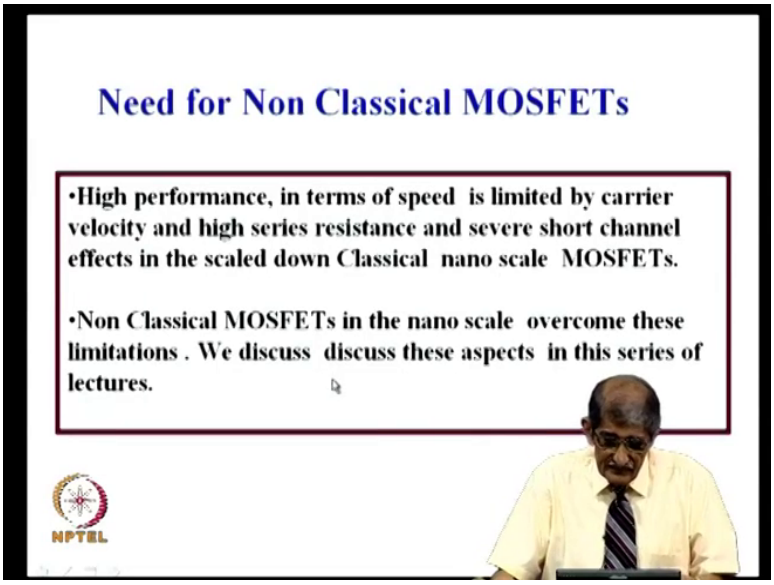
Nanoelectronics: Devices and Materials

Prof. K. N. Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture - 16
MOSFET Analysis, sub-threshold swing "S"

(Refer Slide Time: 00:16)

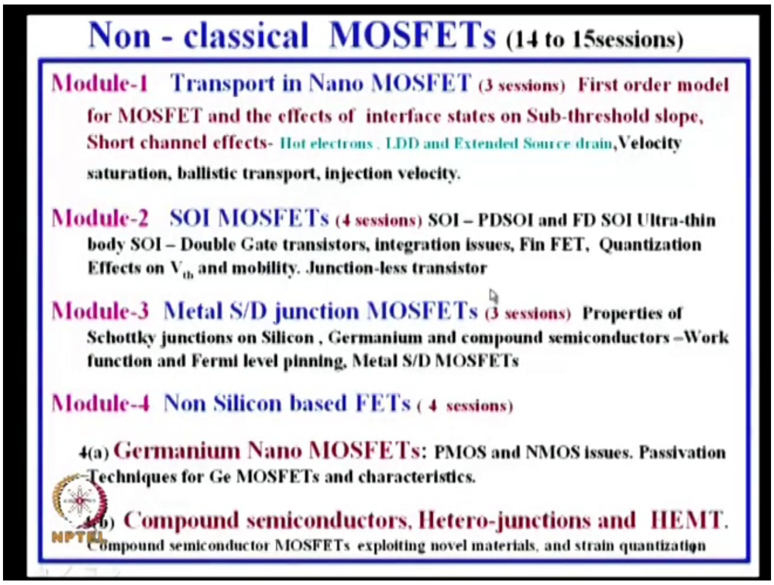


Need for Non Classical MOSFETs

- High performance, in terms of speed is limited by carrier velocity and high series resistance and severe short channel effects in the scaled down Classical nano scale MOSFETs.
- Non Classical MOSFETs in the nano scale overcome these limitations . We discuss discuss these aspects in this series of lectures.

So, we discuss these aspects in the series of these particular lectures which will be in this 15 sessions. Now in this I have just summarized, what it is going to be like in this series of non-classical MOSFETs.

(Refer Slide Time: 00:29)



Non - classical MOSFETs (14 to 15sessions)

Module-1 Transport in Nano MOSFET (3 sessions) First order model for MOSFET and the effects of interface states on Sub-threshold slope, Short channel effects- Hot electrons , LDD and Extended Source drain,Velocity saturation, ballistic transport, injection velocity.

Module-2 SOI MOSFETs (4 sessions) SOI – PDSOI and FD SOI Ultra-thin body SOI – Double Gate transistors, integration issues, Fin FET, Quantization Effects on V_{th} and mobility. Junction-less transistor

Module-3 Metal S/D junction MOSFETs (3 sessions) Properties of Schottky junctions on Silicon , Germanium and compound semiconductors –Work function and Fermi level pinning, Metal S/D MOSFETs

Module-4 Non Silicon based FETs (4 sessions)

4(a) **Germanium Nano MOSFETs:** PMOS and NMOS issues. Passivation Techniques for Ge MOSFETs and characteristics.

4(b) **Compound semiconductors, Hetero-junctions and HEMT.** Compound semiconductor MOSFETs exploiting novel materials, and strain quantization

I have put 14th to 15th having a bun buffer lecture it necessary. Module one which we start today we will have transport in nano MOSFETs. And of course, when we do not get down into the a transport straight away, we will first discuss a first order MOSFET model.

And go through some of the effects of interface states in sub threshold slope. Highlight some of the short channel effects which have already been discussed, hot electrons LED, likely load drain extended source drain, all that has been discussed. So, I will not I will just rush through them. Velocity saturation, ballistic transport, injection velocity. These are the things which one has to see particularly, because you will see that the ultimately the performance of the classical MOSFETs is decided by the injection velocity rather than any other parameters. And the injection velocity you will see that it is controlled by a low field electrical low field mobility of electrons or holes. So, the goal in all these devices non classical devices will be to realize devices which will result in high carrier mobility ok.

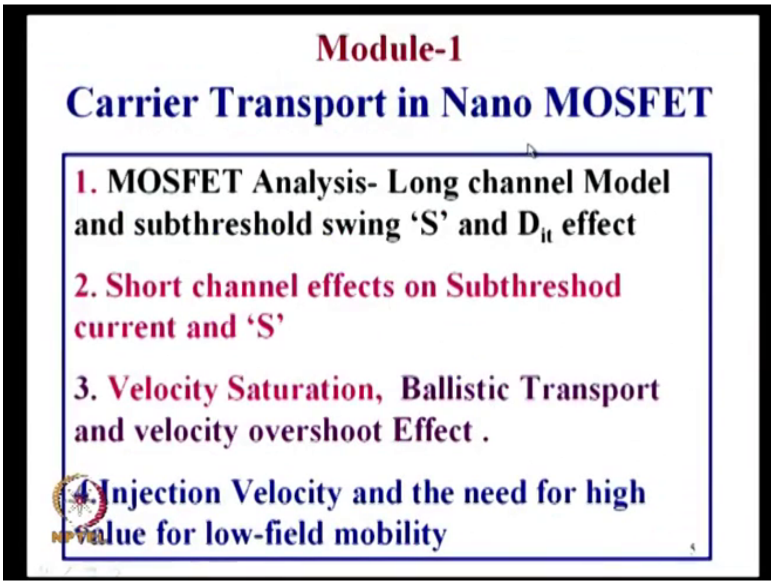
Which automatically will give you high injection velocity. You can also switch through devices like gallium arsenide where you can get velocity overshoot effects. You can over you can have velocities in additional over and above the velocity saturation; that is the module one. Once we see what are the problems and what is required for high performance, we get on to the mostly we will cover about 2 3 lectures. Then we go down to module 2 which is a special device which is very popular today even in industry. Like, I B m they regularly used SOI MOSFETs for their integrated circuits when as and when it is required. Silicon on insulator MOSFET SOI MOSFET.

And here we discuss variant different versions of this type of MOSFETs including the Fin FET and also discuss the quantization effects on threshold voltage mobility, and ultimately we also get down to discuss the latest version of these devices called junction less transistor. Then we have the module 3 in which the focus is on metal source drain junction MOSFETs. Instead of pn junction we will have metal junction, short key barrier junctions. Or omhic contacts, that type of thing. Here we will have to focus quite a bit on the properties of short key junctions on silicon, germanium, compound semiconductors etcetera. Because we will be discussing about the non-silicon based MOSFETs FETs in the next section, that is the module 4. So, there we take on germanium.

So, in order to improve the mobility of the carriers, one way of doing is you use silicon itself. And ensure that doping levels are below. You know, in conventional devices you have to go to very high doping levels 10 to the power 16 17 per centimeter cubed so that the short channel effects are reduced. Now that is achieved by the SOI MOSFET. Now further if you want to improve the mobility, you have to change the material. Materials like germanium, materials like gallium arsenide. Those are the 2 major contenders for high performance devices. Germanium, devices PMOS NMOS. That is what we discussed germanium MOSFETs. Then compound semiconductors based on gallium arsenide, aluminum gallium arsenide, and hetero junction devices.

We will try to cover all that. So, this is where I kept option of going 4 or 5 sessions. So, depending upon that depending upon the availability of plots, we will put 14 or 15 lectures.

(Refer Slide Time: 05:14)



Module-1

Carrier Transport in Nano MOSFET

1. MOSFET Analysis- Long channel Model and subthreshold swing ‘S’ and D_{it} effect

2. Short channel effects on Subthreshod current and ‘S’

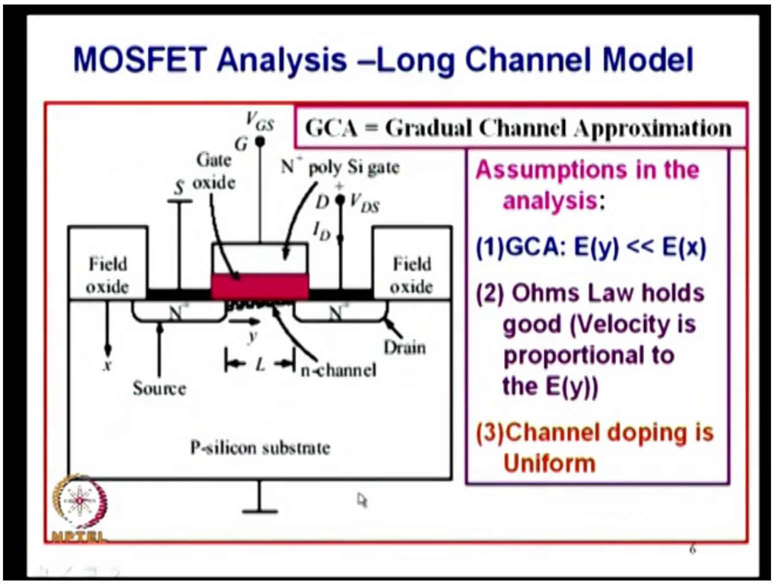
3. Velocity Saturation, Ballistic Transport and velocity overshoot Effect .

4. Injection Velocity and the need for high value for low-field mobility

So now we take the module one. The module one we begin with some sort of a review. So, that your focused on this topic. So, we will talk take the conventional MOSFET, and conventional analysis long channel model, and sub threshold swing, and the effect of interface density state density. On the sub threshold swing I was informed that the D it effect on sub threshold slope was not covered in the previous presentation, though the D it is discussed in the great detail. Then short channel effects mainly on sub threshold swing and current.

Where it will touch upon this, then we will go on to the velocity saturation ballistic transport and velocity overshoot effect. Injection level velocity, and need for high value of low field mobility, those are things which will covered. So, you will see that there is a bit of overlap in this particular module, but when I go to next these are required. So, I just I am just quickly running through this thing today it will be mostly some of these thing I will not be able to cover the entire thing today this will be covered in 2 3 lectures.

(Refer Slide Time: 06:32)



MOSFET Analysis –Long Channel Model

GCA = Gradual Channel Approximation

Assumptions in the analysis:

(1)GCA: E(y) << E(x)

(2) Ohms Law holds good (Velocity is proportional to the E(y))

(3)Channel doping is Uniform

So, this is the diagram which you will see everywhere in textbooks, all text books. We can see that you have got a substrate which is made up of silicon in the conventional MOSFET. And you have got the red color is the oxide, then this is the polysilicon gate. If it is a n channel MOSFET it is n plus heavily doped, and you have got the source drain n plus source n plus drain. And when you analyze this, you will actually not bother about the entire region.

You your focus will be only on this portion. Because that is the portion which gives you the MOSFET action. And these are the thick oxides which allow you to isolate one device from the another device in a integrated circuit. So, if it is a n channel device, you use p type substrates. And when while analyzing you have some simplification is done. The most important simplification which is done in the schottky analysis is GCA; that is gradual channel approximation.

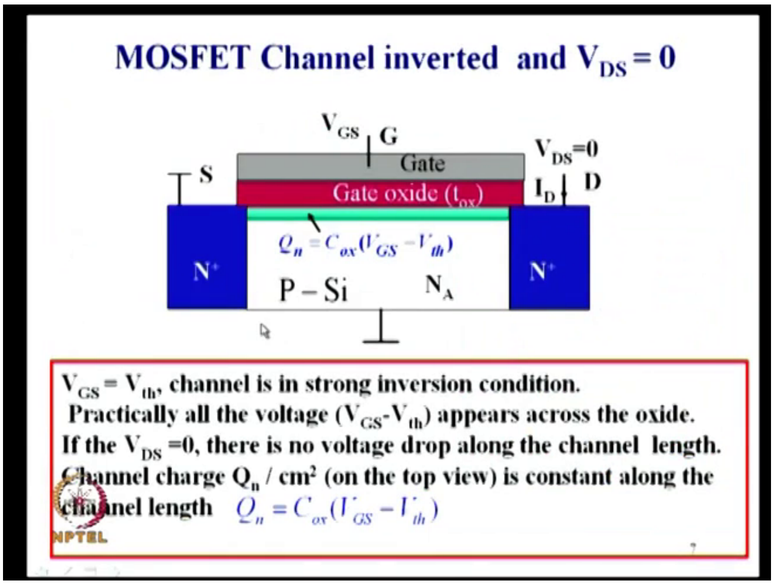
What is the meaning of that? The electric field GCA gradual channel approximation says, or considers or assumes; that the electric field along the channel, I marked it as y direction, along the channel is much smaller compared to the electric field along the vertical direction; that is x is marked as vertical in my case. Which would mean that, you can ignore the 2 dimensional effects. For while you solve for the carrier concentration in this direction. You solve the poissons equation along the x direction, that is top to bottom. I have marking it on conventional, y is in the horizontal direction x is in the vertical direction ok.

So, you can solve poissons equation in one dimensional direction, because you consider the electric field only in the E x, because E y field is small. This assumption will fail when you go to high fields in the y direction; that is where you have to think other methods of solving it. Then also you assume that ohms law holds good. When you say ohms law holds good what is the meaning immediately you say, V is equal to I into R. When you say V is equal to I into R what you assume is that the velocity of electrons or carriers is proportional to the electrical field; that is the meaning of ohms law holds good.

So, if you know the mobility and the electric field, I can straight away say the velocity is equal to mobility into electric field. Others it is proportional to electric field; that is a ohms law. Now other assumptions in this analysis is channel doping with uniform. That are minor modifications on this if you have non uniform doping concentration, that I do not get down to discussion, I just took this up for continuity sake. So, here these portion I have shown that is where the channel is present. You can see that when the voltage is applied here, the or when you apply voltage to the gate the p channel p region.

Gets inverted and becomes n types. I would say electrons are collected here, that is a inversion layer is present here. If there is a voltage drop along this direction by means of applied voltage, you will see that or you know that the potential available for inverting is less than V GS ok.

(Refer Slide Time: 10:23)



MOSFET Channel inverted and $V_{DS} = 0$

$V_{GS} = V_{th}$, channel is in strong inversion condition.
Practically all the voltage (V_{GS}-V_{th}) appears across the oxide.
If the V_{DS} =0, there is no voltage drop along the channel length.
Channel charge Q_n / cm² (on the top view) is constant along the channel length $Q_n = C_{ox}(V_{GS} - V_{th})$

So, we will see what it is. Now quickly notice we have taken only this portion of that because that is where the transistor action is, and what are this portion to the bottom portion? It is in the mechanical support. When you have a after all this region will be as thin as point 1.2 microns, but this whole thing is the vapour which will be 300 microns 400 microns depending upon the vapour thickness. If you have a 4 inch vapour effect you can say so; that is 100 millimeter diameter vapour that would be about 400 micro meters thickness.

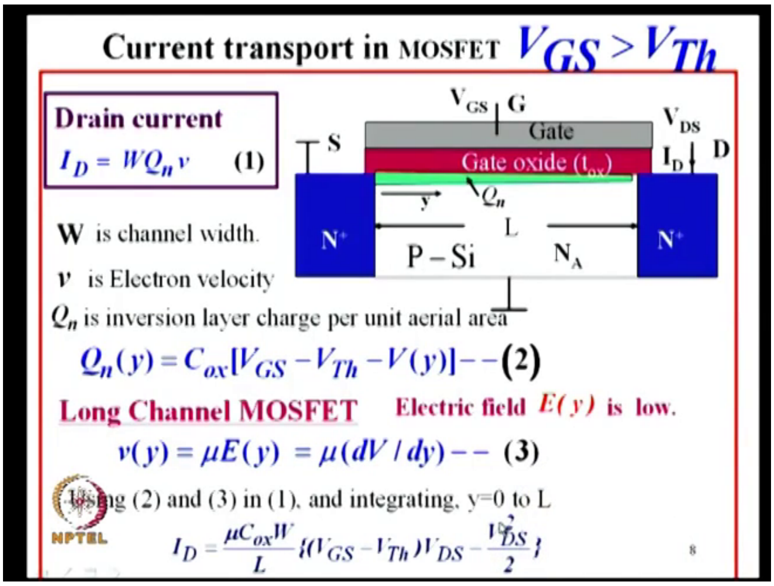
So, that is to give an idea. So, that is why this portion is of the mechanical support. See the entire action is on top portion it would put only that layer. Source, drain, that is the region between p type. A gate oxide which is very thin. Whole transistors had about 100 nanometers. Today you go down to one nanometer to avoid the short channel effects. And this is a gate. The gate can be metal, but usually it is poly silicon doped very heavily. Now you can see if there is no voltage applied between the source and drain V DS equal to 0. The voltage applied in the gate and substrate, I shown in the contact here, but it is a far away from that. Then plus voltage will apply. A field length terminate on this semiconductor here it will initially deplete.

And then finally, when the voltage is large enough there will be electron is accumulated. These are been illustrated in detailed in the last series of lectures, your electrons which is know nothing inversion here. So, you say that it is inverted when the gate voltage is threshold voltage; that is V threshold voltage. So, see one till you till the channel is inverted, the voltage applied voltage to the gate is shared between these oxide and the top depletion layer. V oxide V G is equal to V oxide plus V silicon V silicon is depletion layer voltage. But once this there is enough electrons accumulated in the n channel device, then the plus charges which are generated here due to the applied plus voltage required negative charge they come from this channel itself

That is the voltage over and above the threshold voltage appears totally across the oxide. So, the charge in inversion layer, here will be V G minus V threshold; that is the voltage that appears this oxide. So, V G minus V threshold into the capacitance of the oxide. So, that is what is written here. V G minus V threshold into C oxide C oxide is the oxide capacitance per unit area. So, one may say if this is unit area the Q n that inertia area charge that will be charged per unit area unit area not looking into the plane of this, like this, it is a charge looking for a top per, unit area looking for the top. So, we conclude the area of the gate charge gate region; that is the channel length or the gate length into the depth of the gate w; that will be the total area.

So, this is when the V D equal to 0, or you can see when V D equal to V DS equal to 0 there no drop across the channel. So, whatever voltage you apply the V G minus V threshold is available for creating these charges.

(Refer Slide Time: 14:18)



Current transport in MOSFET $V_{GS} > V_{Th}$

Drain current
$I_D = WQ_n v$ (1)

W is channel width.

v is Electron velocity

Q_n is inversion layer charge per unit aerial area

$$Q_n(y) = C_{ox}[V_{GS} - V_{Th} - V(y)] -- (2)$$

Long Channel MOSFET Electric field $E(y)$ is low.

$$v(y) = \mu E(y) = \mu (dV/dy) -- (3)$$

Using (2) and (3) in (1), and integrating, y=0 to L

$$I_D = \frac{\mu C_{ox} W}{L} \{(V_{GS} - V_{Th}) V_{DS} - \frac{V_{DS}^2}{2}\}$$

Suppose you apply V DS positive what happens? Immediately you have got plus voltage here, and this is connected to the drain, all through that is inversion layer. Therefore, depending upon the voltage that you apply, there is current flow from the drain to the source, due to flow of electrons from source to drain. So, source is the supplier of electrons, when the source is half send this supplier of the electrons is the p type region, minority carriers they will not be able to respond high frequencies, but when you have this source here supplying the carriers, they may be minority carrier here, but their majority carrier here there is large resolvers of electrons present in the (Refer Time: 15:02) region. So, that can supply this, and this drain collects those electrons here. So, this is a source channel and the drain.

Now notice that difference between the previous diagram and this diagram. I have drawn the channel charge maximum here tapering down to close to 0 here. How much close to 0, it is here it depends upon the voltage dropped across the channel, why? At this end the voltage is 0. There is the voltage is 0. From here to here if you go V DS is 0 here, maximum here. So, if this is 0, but where even though this is 0 due to the gate voltage there is a potential, which you call it as some psi of s, you call it as some psi of s. So, there are some there is some potential due to that, but that potential is used for creating this inversion layer. What I am talking of is applied V DS is 0 here.

Therefore, voltage available for this inversion here is equal to V G minus V threshold. If you move in this direction from here to here there is a voltage rise equal to V DS. If I take the any point y here there is a potential rise from here to here equal to V y. So, if this was 0, this is V y. At this points the charge the voltage available for creating the inversion layer was equal to V G s minus V threshold. But out of that voltage V y s gone to this. So, the voltage available here is equal to V G s minus V threshold minus V y. So, charge that any point y is equal to C oxide into instead of V G s minus V threshold.

We have got minus V y because the part of the voltage is gone into this portion. Let us go to this end it is equal to V G s minus V threshold minus V DS. So, that is a charge. Now what is a velocity at any point? Velocity at any point is equal to mobility into electric field; that is ohms law. So, I can write electric field magnitude as d V by d y, y is in that direction. So, mobility into electric field mobility into d V by d y, that is equation by 3.

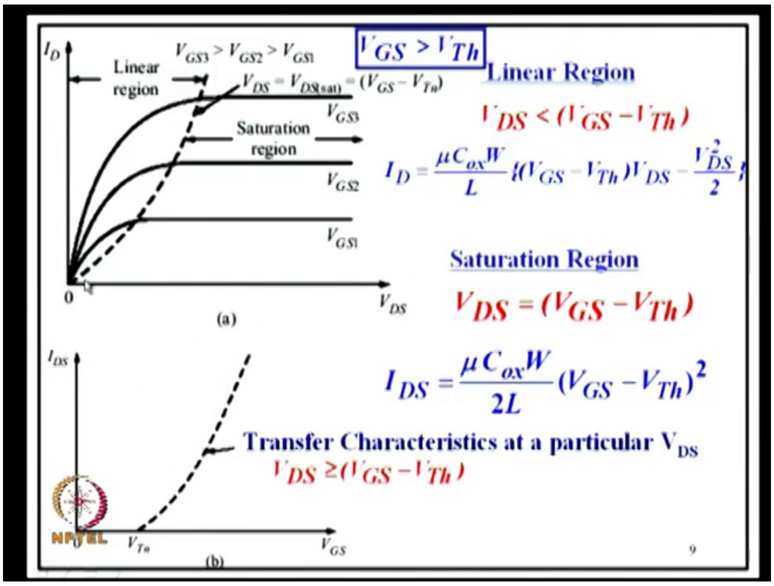
Why are you looking at this Q and velocity? The current drain current is given by this this expression. Because Q n is a charge per centimeter square here at any y, and that that is actually charge sheet. If I multiply it by w, and d x that is the total charge available in the d f x, Q n is per unit area into w depth into d f d of x d of y, that gives me the area. Now I have w into Q n into d y by d t, what is that? So, Q n into w into d y by d t is equal is the velocity. W into Q n into V is Q n into w I am sorry, Q n into V v is d y by d d w d y is a total charge where d t is the current. So, in time d t charge moves by distance d of y. So, whatever of percent in the depth d y is collected in the d T. So, this is the standard equation I am sure you have discussed this in the previous presentation. Otherwise it is a whatever transport phenomena mechanism you talk of you can write this equation. Supposing the velocity is saturated velocity, then you can write this as w into charge into saturation velocity.

Now we are talking of case where velocity is proportional to electric field therefore, we find out the Q n multiplied by this velocity. So, putting these 2 together I will not go through the simplification, you can just work it out very easily substitute these 2 here; that is w into Q n is this quantity into mu into d V by d y. And integrate that from y is equal to 0 to l, and V is equal to 0 to V DS, you get this equation. Let me not go through it spending a time.

You can sit down and work it out. It is substituted on these 2, integrate from y is equal to 0 to l. And V D equals from 0 to V DS. So, this is the equation for the drain current. So, long as this path is there right through this region. So, whatever V DS we apply appearance between these I have shown a small opening here, actually there will not be any opening it will be continuouss there. So, it is a continuouss path. It is equivalent path of putting a resistor between this point, and that that simplification of this law. You have put a resistor here. If the V DS equal to 0, the resistance the channel charge is constant, it is equivalent of resistance which is from uniform depth. Now when you apply voltage the charge concentration here keeps on reducing.

Because of voltage drop, which you can look into as a resistor whose area of cross section decreases. So, as you apply the voltage V DS the area of cross section of this resistor keeps on falling. What happens to the resistance value? It increases. Rho l by a. Rho is the same. Rho l by a, the area of cross section decreases. So, that means, as we increase the V DS, the resistance does not remain constant, but the resistance keeps on increasing. It should be in that if I keep on increasing V DS, the current will not be linearly increase in the V DS, it is reflected from this equation. In this equation you can see the second term is not present. The I D and V D that is linear. So, that is the point at which the voltage drop is small V DS is very, very small. So, as the V DS becomes more and more, this portion takes care of the varying cross section to say, it is not really cross section. It is the charge that is varying.

(Refer Slide Time: 22:18)



$\boxed{V_{GS} > V_{Th}}$

Linear Region

$V_{DS} < (V_{GS} - V_{Th})$

$$I_D = \frac{\mu C_{ox} W}{L}\{(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}\}$$

Saturation Region

$V_{DS} = (V_{GS} - V_{Th})$

$$I_{DS} = \frac{\mu C_{ox} W}{2L}(V_{GS} - V_{Th})^2$$

Transfer Characteristics at a particular V_{DS}

$V_{DS} \geq (V_{GS} - V_{Th})$

So, if you see the characteristic now. So, this is linear, you can see initially it is linear. Then as I increase the V DS, the current does not increase linearly, because the resistance does not remain constant, the resistance keeps on increasing. So, a current does not increase correspondingly. Now at a particular V DS, the V DS becomes equal to V G s minus V threshold voltage, the current saturates. What happens is; go back to the next slide, what happens is, when that happens when the V DS is equal t V G s minus V threshold, the voltage drop from here to here is equal to V G s minus V threshold.

When the V G s is equal to V DS equal to V G s minus V threshold, what is the meaning? The voltage drop across the channel is V G s minus V threshold. What is the voltage drop across the gate and the channel at that point? V threshold itself. Because this is V G s out of that V G s minus V threshold is there. So, subtract that, you get this voltage V threshold; that means, the channel is just about uniform there. If I apply more voltage there is no channel there, but there is a depletion layer. So, you can see now, when the channel has just opened, it is a very interesting phenomena I over simplifying it and telling you when the channel is just opened. The voltage drop across the channel is V G s minus V threshold this is the channel potential. If I increase the V DS beyond that point this voltage drop where it is channel is opened up remains the same thing V G s minus V threshold. What about the resistance value between this point, where is opened and this point?

That is the same, because this is C oxide into V G s minus V threshold this is just equal to V G s minus V threshold is the drop here. So, the charge here remains the same as when at as just opened. If there is a lightly doped region on drain region depletion level move into the drain region. But this opening will be remaining there how does the current flow from this to this one when there is a opening; that is because this is n plus there is a depletion layer here the electric field is actually from the drain to the channel the depletion layer. So, as a result the electric field is from the n plus to the channel depletion layer. So, electrons reaching this edge of the depletion layer you will collect it there right, like the bi polar transistor, see these are almost like a bi polar transistor. The difference is here the electrons are injected and they flow by drift, and they are corrected by this collector here, we will call it as drain.

The bi polar transistor, there is no field in this region, electrons are injected from n plus region to the p region. There is no inversion layer because there is no gate. They move through the this region by diffusion, they are collected here that is the difference the transport mechanism. In fact, you will see if the carrier concentration very, very low as it happens in the sub threshold region you will see that the current flow is by diffusion. So, there is the difference in the mechanism of transport when there is inverted and just below the inversion layer.

Now coming back to this point, why does this saturate? When this has just opened, and beyond that point the if you consider this as the resistance that resistance value remains the same thing because charge distribution remains the same thing, because this voltage at this edge is V threshold, voltage at voltage at this edge is V V G minus V threshold. Which is available for for charge. So, total charge is the drain thing, and the voltage drop from here to here is remaining the same thing.

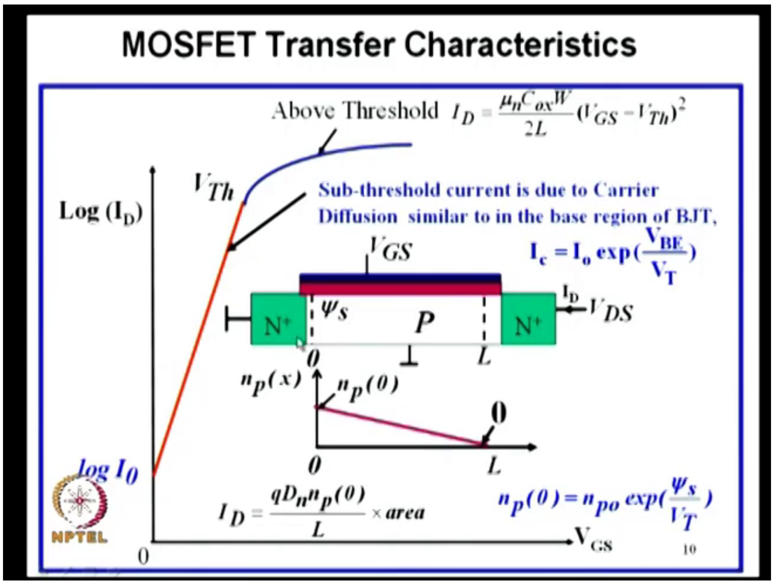
So, what would you say? That means, drop across the this region is something, the resistance the current is the same thing. Because rest of the voltage that you applied to the gate does not go into this channel, it goes into depletion layer. So, there for you get beyond that point current saturates and flat is the over simplification, but there is a first order theory. So, that is happening when V DS equal to V G s mu threshold? So, current at saturation is I have just rewritten this equation here, and at saturation you substitute V DS equal to V G s minus V TO. So, when you substitute that you get this equation. Just a substitution is you can just sit down and work out that. Substitute V DS equal to V G s minus V threshold we get that, then the standard (Refer Time: 26:55) law. You can see this is independent of V DS.

Because all that V DS does not go to the channel it goes into the depletion layer. Now from here you can see that we get better current, better performance if the mobility is high. So, from here you will say I would choose a material which has got high electron mobility or high hole mobility, very indicative of this is there. And of course, you want to have larger I D. Why do we want larger I D? Because trans conductance defined as delta I D s by delta V G s is proportional to C oxide and w. You would increase w you get larger current and larger trans conductance you do not like that. Why do not you like it? Because it occupies lot of space width and it also give rise to the capacitance. So, the way you do it is you will see that you will already that you increase the C oxide.

And may be reduce w, increase the C oxide and reduce the channel length, all these increment give rise to better drain current and better trans conductance; that is delta I D s by delta V DS which is proportional to this quantity. So, the transfer characteristic is at any voltage here if I go along this direction for a constant V DS. I take I D s like that. For V DS less than V threshold voltage current is practically 0. This is over simplification telling that when V threshold V G s equal to V threshold current is 0. Strictly it is not true. It is finite there, that is sub threshold we will discuss that later already some discussion have been done. And this is the curve which will tell you which gives V DS is V G s minus V threshold.

Because larger the V G s larger will be the saturation voltage; that is what is presented here. In fact, this also will tell you that you may I will not discuss that aspect you can try there drain and the gate to the together, and you can get the characteristic, 2 dimensional characteristics. Drain and the gate. V DS equal to V G s practically. So, that is what I wanted to mention here.

(Refer Slide Time: 29:32)



MOSFET Transfer Characteristics

Above Threshold $I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{Th})^2$

Sub-threshold current is due to Carrier Diffusion similar to in the base region of BJT,

$I_c = I_o \exp(\frac{V_{BE}}{V_T})$

$I_D = \frac{qD_n n_p(0)}{L} \times area$

$n_p(0) = n_{po} \exp(\frac{\psi_s}{V_T})$

Now, above threshold voltage therefore, you have got in the saturation region. What do you mean by saturation? That region. V DS greater than V G s minus V threshold you get this characteristics. Now in the same region if I go down here, at a particular point you have got a threshold voltage V G s equal to threshold voltage.

In the previous diagram we have put this as 0, but if you plot it on the logarithm scale, it is not equal to 0. It will be finite and go down to very low values like this. That is a sub threshold current and that is due to the transport of carriers from the source to drain when the carrier concentration is low. There are not sufficient carriers so that the drift current cannot hold good, cannot support that current. Drift current depends upon the carrier concentration and electric field, and that carrier concentration goes down drift current goes down. In fact, even when you take the previous case I will just go back through quickly to the next slide here, even in this case the carrier concentration Is high here, and it is 0 there. There is concentration gradient, which would mean that there is diffusion current.

But the drift current is very high compared to the diffusion current, because the current drift velocity is high compared to the way they carriers move by diffusion. That depend from upon concentration gradient that velocity is low. So, here the drift current is dominated, you can comfortably neglect diffusion current. But when you go to this region. Where there hardly very I say I have removed that inversion layer there. I have removed the inversion layer here. But there are carriers. They are they are still electrons. If you re call when you keep on applying plus voltage to the gate it becomes less p type; that means, it is depleted on the surface, and then what it more depleted then becomes n take in electrons are attacked to surface. So, when you go just below the threshold voltage there are not enough electrons.

They are taught density is less compared to the hole density in the bulk that is a sub threshold region, but those electrons cannot move by drift; that means, there is hardly in a voltage drop across that. So, it is like a bi polar transistor. Now it is acts like a bi polar transistor. So, you have got the source, you have got the drain, instead you can call it as this emitter, you have got the collector, and emitter injects electrons to this region. And from here to here the drift current is negligible therefore, current flow is by diffusion.

Now what is the state of for this junction is concerned? See when I apply voltage plus here, ground here or ground here, but in the gate and this point there is that V G S. You can see that at inversion you watch this carefully at inversion you applied plus voltage the carrier concentration was equal to the electron concentration was equal to the hole concentration at this end. Now what is the potential here? The surface potential was you call it as surface potential.

There is potential here at the top surface is twice phi f or twice phi b. You know what it is. When inverted potential is twice phi B phi B is k t by Q logarithm of doping by n I. So, you have got the potential plus minus, plus minus, this is plus. So, with respect to this ground the source here the potential there is a depletion layer across the source always, even when it is inverted case, there is a barrier here. Carriers are injected across the barrier, because that is forward bias. See when you go to this particular situation here, carriers are injected from the source to the channel across the barrier.

And when the channel is not present what is the barrier built in potential. When the channel is present, if the potential is twice phi f what is the barrier built in potential? Minus phi s. So, barrier is reduced by phi f. So, carriers are injected across that same phenomena there bipolar transistor. The difference is instead of that here is drift when you go to this the barriers still present, but barrier is slightly more than V B I minus twice phi f. It is V B I minus phi s surface potential. There is a barrier is reduced by phi f s. So, still because it is forward bias equal to phi s surface potential there will be carrier injection. So, that is transported. What is the carrier concentration here? I call it as n p. N p 0, 0 is y equal to 0 here, and y equal to l here. Both ends you can see their depletion layer.

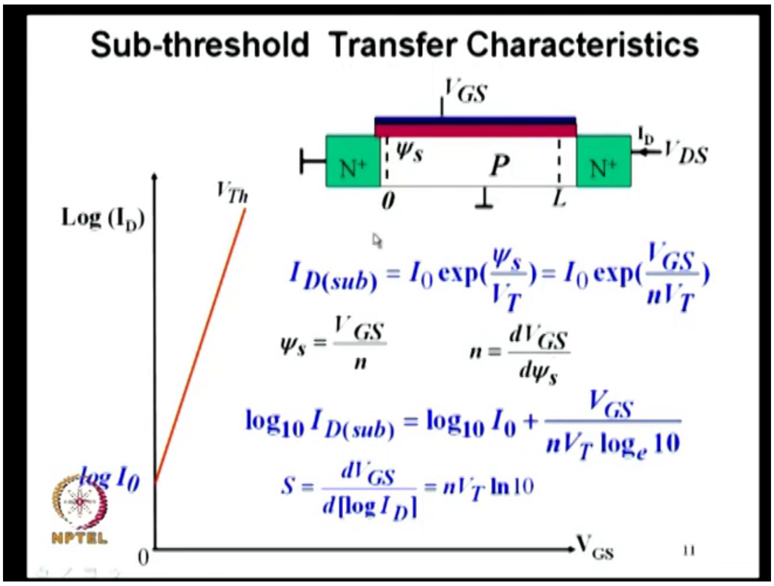
This is forward bias junction, this is reverse bias junction, this is a depletion layer width if it is heavily doped 0 l the carrier concentration is n p 0, and this is a boundary condition of a junction. So, n p 0 will be related to the minority carrier concentration in the p region. That is minority carrier concentration under thermal equilibrium condition into exponential whatever potential forward bias is there across the junction divided by k t by Q B. T is k t by Q thermal voltage. This is a standard boundary equation, boundary condition. Boundary condition for minority carriers here. Because electrons are minority in the p region. The boundary condition is whatever thermal equilibrium boundary condition is there, that is n p 0, into exponential whatever voltage is there forward voltage there divided by k T.

Forward voltage is psi of s, is it all right? So, you can see that carrier concentration that what is carrier concentration here? 0, because reverse bias collecting. Whatever is reaching is collecting. In between there is no base contact. Here I am showing the base contact, but there is no contact into this particular region there. So, there is no recombination, there is no bias base current. And partly when this length is small there is no recombination. So, whatever carriers are injected here, will be collected here. Carrier concentration is n p 0, carrier concentration is 0 here. And the current flow from here to here if it is by diffusion, what is the current flow equation, current flow is governed by Q d n n p 0 divided.

By divided by l, what is n p 0 divided by l? That is the slope. So, the diffusion current is Q d n d n by d of x is current density into area. I do not know what the area is if the junction if the whole thing is injecting and current flow done it will be entire depth. But in the case of bulk MOSFET what we are talking of it will be inverted only near the top. So, area will be actually w into the depth of depth where the charges are present. So, this is the carrier distribution linear. It is linear because the slope here and slope here will be same thing. Where ever you take the current is the same thing, there is a current continuity; that is the meaning of that. So, I can write it as Q d n n p 0 by l that Q d n d n by d of x everywhere into area that is a current. And I substitute for n p 0 this quantity.

What we get? We get a term which depends upon the charge, diffusion coefficient and what is n p 0, it depends upon doping level here. N I square divided by doping concentration. So, this is the doping dependent quantity. So, some constant term into exponentially E to the power of psi s by V t, you see that there.

(Refer Slide Time: 38:28)



Sub-threshold Transfer Characteristics

$$I_{D(sub)} = I_0 \exp\left(\frac{\psi_s}{V_T}\right) = I_0 \exp\left(\frac{V_{GS}}{nV_T}\right)$$

$$\psi_s = \frac{V_{GS}}{n} \qquad n = \frac{dV_{GS}}{d\psi_s}$$

$$\log_{10} I_{D(sub)} = \log_{10} I_0 + \frac{V_{GS}}{nV_T \log_e 10}$$

$$S = \frac{dV_{GS}}{d[\log I_D]} = nV_T \ln 10$$

So, I have read it on that equation. I D sub, that is sub threshold current. I D I am just rewriting that by substituting this there I naught it can be written as I psi naught E to the power of psi of (Refer Time: 38:44) where I naught actually depends upon Q d n by l and n p 0. N p 0 is the depend doping. Now let us see how this would affect the threshold.

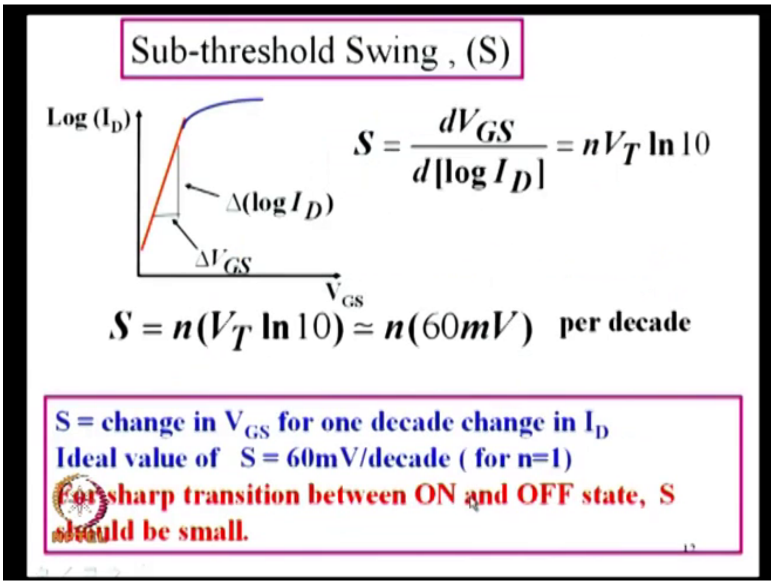
I am sure this has discussed in some detail, but I want to bring in that other factor that is why I go to going through. So, this is the sub threshold current. Psi s by V t, now psi s is part of the V G s. V G s gets shared with the oxide and this silicon this junction. So, I can call it as V G s by n times V t, where n is greater than 1 or equal to 1. It is greater than one usually so that there is a; if it is equal to 1 whatever V G s is there goes to psi of s. Thinner the oxide more voltage will go to the junction. So, thinner the oxide n will be closer to 1, that is a meaning of that. So, psi s is psi s by phi s I have writing it as V G s by n. What is n? N is delta V G s by d psi of s from here. I just assume some factor I do not know what it is write now we will see what it is.

So, I substitute here. N is equal to given by this equation. Since it is logarithmic. So, you know that this is a exponential. So, in the log scale I can put t as linear curve that is what is the sub threshold. So, you saw when you previous curve you saw it was like that. After threshold duel threshold, it is linear in logarithmic scale. Now I take logarithmic on both sides. Logarithm of this current is equal to log I naught to the base 10. Because it is easy to work out in the decades log 10. Log I naught to the base 10 plus V G s by n V T since it is log 10, you have a dividing factor log 10 to the base E mathematics. So, you have got this term coming up, because it you have taking it log 10.

If your log 10 base e would had only V T by V G s by n V T. So now, we define the term sub threshold slope, which is delta V G s divided by delta of this quantity. So, delta V G s, divided by this quantity is take this whole thing on to that side, and bring this this side, that is n V T log 10. So, from this equation (Refer Time: 41:25) we can see that sub threshold slope, or sub threshold swing is delta V G s. Delta V G s divided by delta of logarithm of I D; that is n V T log 10. That is a sub threshold slope. And from here you can see what is V T log 10? V T is k t by Q about 26 millivolts at room temperature.

Lower temperature so of course, it will be reducing. So, and V T log. 10 we will see what it is. So, sub thresholds swing is n V T log 10.

(Refer Slide Time: 42:10)



Sub-threshold Swing , (S)

$$S = \frac{dV_{GS}}{d[\log I_D]} = nV_T \ln 10$$

$$S = n(V_T \ln 10) \simeq n(60mV)$$ per decade

S = change in V_{GS} for one decade change in I_D

Ideal value of S = 60mV/decade (for n=1)

For sharp transition between ON and OFF state, S should be small.

You can essentially inverse slope; that is delta V G s by that delta log I D. So, sub threshold swing, or sub threshold slope is n into V T log 10. And V T log 10 26 millivolts into log 10; that is about 60 millivolts. So, sub threshold swing is 60 millivolts into n what does it mean? Delta log I D is equal to 1. When you take this slope Log I D when lon I D is for example, delta lon I D may lon 100 divided by lon 10.

The lon 10, that is log 10 that will be equal to 1. So, that is a when it is one you get 60 millivolt per decade. So, if you take this as one decade how much is this that is the sub threshold swing. So, the best value that we can get. What is the best value? When n is equal to 1 sub threshold swing is 60 millivolts; that is the change in V G s for one decade change in I D, that is a meaning of that one decade change in I D how much is the V G s required. Now this is a very important parameter in the MOSFETs particularly when you go for low voltages. What you need is when you want to go for low pole devices and low voltages, you need to have this threshold voltage as low as possible.

Now, if the swing is 60 millivolt per decade, I will give you an example to understand this. If the swing is 60 millivolts per decade, that is if n is equal to 1. It is 60 millivolt per decade. What is a meaning of that? The current will far reduce by one decade, when the voltage is reduced by 60 millivolts. Gate voltage is reduced 60 millivolts below threshold voltage. So, for example, if the threshold voltage is 300 millivolts here. When you reduce the gate to and if let us say current is one micron I am just for example, I am taking if the current there is one micron it is not 0, it is finite that is a catch here. So, it is at threshold voltage let us say that there is one micron current flowing.

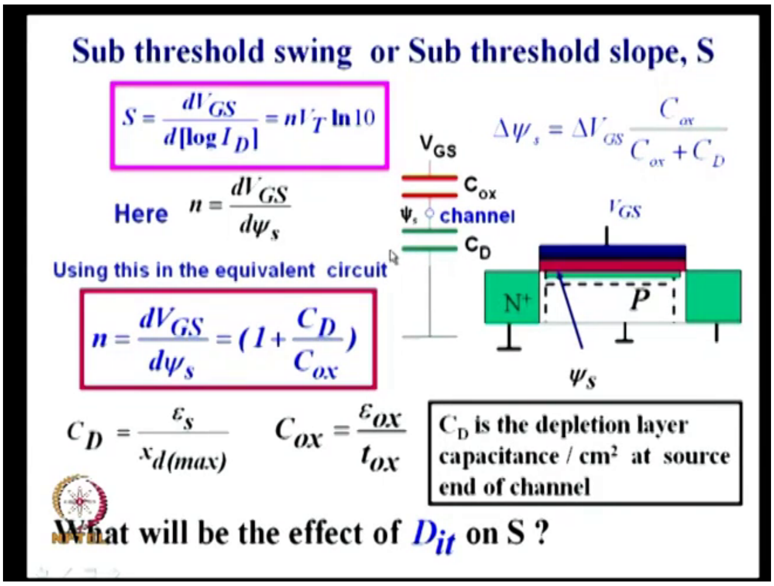
Now, when you and if the n is equal to 1, how many decades must the current come down here? This is 300 millivolts. So, I have to reduce the gate voltage from by 300 millivolts. So, if the slope is equal to 60 millivolt per decade, it have to fall by per decades. 300 millivolts divided by 60 millivolts, that is when the voltage falls from 300 to 60 the current will fall by per decades. So, that is ideal case. If n is equal to let us say 2; that means, the current will fall by one decade if it is 120 millivolts. So, let us say it is 0.362 to make it easy.

Let us say threshold is is 360 millivolts, and n is equal to 2. So, one decade current falls, the voltage will fall 120 millivolts. So, if it is 360 millivolts, by the time you reduce the voltage to 0 0 volts, 360 by 120, current will be fallen down by 3 decades. So, from one micron minus 6 should have gone to 10 to the power minus 9. But if the in the previous case it has fallen down to 5 decades. That it will have gone down 10 to the power minus

6. So, what you are telling is; if you want to reduce this threshold voltage down it should be steeper. If it is not step per if it is falling down like that, the current will be at 0 voltage will be finite it will not be 0 actually drain voltage. So, there is need for having sharp threshold voltage sharp sub threshold.

We will see how that works out here by taking this in this example this has been discussed in detail.

(Refer Slide Time: 47:07)



Sub threshold swing or Sub threshold slope, S

$$S = \frac{dV_{GS}}{d[\log I_D]} = nV_T \ln 10$$

$$\Delta\psi_s = \Delta V_{GS}\frac{C_{ox}}{C_{ox}+C_D}$$

Here $n = \frac{dV_{GS}}{d\psi_s}$

Using this in the equivalent circuit

$$n = \frac{dV_{GS}}{d\psi_s} = \left(1+\frac{C_D}{C_{ox}}\right)$$

$$C_D = \frac{\varepsilon_s}{x_{d(max)}} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

C_D is the depletion layer capacitance / cm² at source end of channel

What will be the effect of D_{it} on S ?

So, I will quickly run through that; I will not discuss the I will not be able to discuss the effect of D it today. But still I will just see what we can discuss here. So, there is need to reduce threshold voltage. So, therefore, need to keep this sub threshold swing as sharp as possible. There is need to make n as close to 0 as close to one as possible. So now, we will see what are the factor which effects is n. That can be done that will making this equivalent circuit. So, you see that below threshold voltage, the applied voltage is gets shared between the oxide and the depletion layer. And between the gate and the substrate, you can draw an equivalent circuit of C oxide in series with the C depletion.

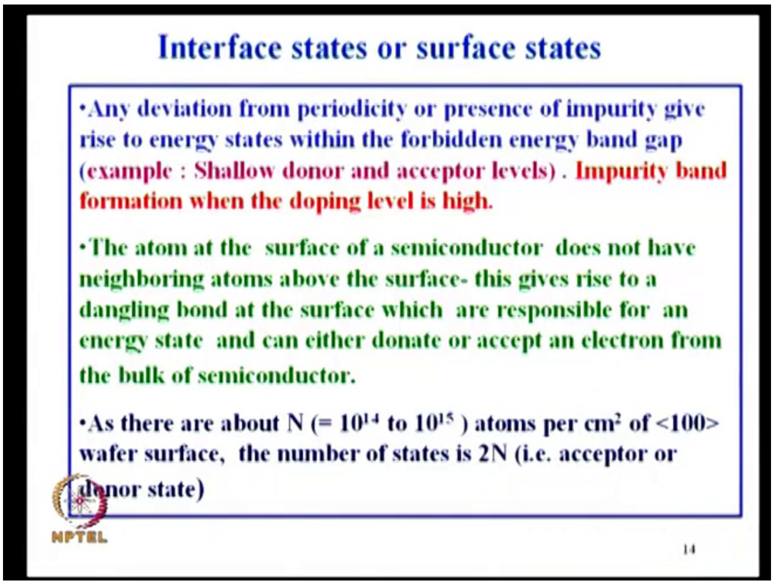
Now that is the that is the equivalent circuit. Now from here what is that n? N was what we defined is recall back we defined, it as V G s by n delta V G s by delta psi of s. N is that now if you have this equivalent circuit like this, you can immediately see at a given V G s, if I change it by delta V G s, what we are interested in this the slope. So, what we are interest in is actually this slope; that mean what we are interested in this delta V G s by delta psi of s, that is n. So, delta V G s if I apply here over and above that V G s, the voltage here is delta V G s into C oxide divided by sum of these 2. This is the basic voltage carrying between the capacitors. V G s divided by C ox plus C D into C oxide is the voltage here with respect to substrate. So, you know that delta V G s by delta psi f s is actually equal to delta V G s by delta psi f s is take this at side C oxide plus C D by C oxide, which is that. So, immediately you can see that the ideality factor, if you can call it, n is delta V G s by delta psi s equal to 1 plus C D by C oxide. This is a very, very useful information. You know without going into the device physics we can understand this using this capacity equivalent circuit. So now, what will you say? What is C D? C D is the depletion layer capacitance. Remember all these are referred to per unit area.

Because both areas are same, this is per unit area. Therefore, per unit area C D is epsilon silicon epsilon 0 of course, I am assuming absorbing that into that. Depletion area capacitance is epsilon silicon divide by x t maximum. I call st maximum because you find out that at this point, where depletion area maximum goes to that side it will be different take it very close to the you can say s t at the source end and C oxide is epsilon oxide divided by t oxide remember epsilon oxide includes is actually epsilon 0 into epsilon r. So, that is the thing.

So, what would you do to improve the sub threshold slope? That is what we are just want to see here. Straight away it is clear. Best that you can get is 60 millivolts, it is lon 10. I have to make C D very small compared to C oxide. One way of doing that is reduce the C D. I can reduce the C D, how can reduce the C D? By reducing the doping here. If the doping here is reduced depletion area width is larger C D will be smaller, but you can not tolerate that in the short channel devices. Because you look for reducing the effect of channel engrowthment into the channel region therefore, you would keep doping concentration higher. So, what is alternate? Increase the C oxide. How can we increase the C oxide? By reducing t oxide.

So, this actually goes along with your requirement of improvement of trans conductance and the drain current, where you can increase the C oxide and increase the both trans conductance and the drain current for a given device symmetry, sub threshold slope also can be improved by that.

(Refer Slide Time: 52:15)



Interface states or surface states

- Any deviation from periodicity or presence of impurity give rise to energy states within the forbidden energy band gap (example : Shallow donor and acceptor levels) . Impurity band formation when the doping level is high.
- The atom at the surface of a semiconductor does not have neighboring atoms above the surface- this gives rise to a dangling bond at the surface which are responsible for an energy state and can either donate or accept an electron from the bulk of semiconductor.
- As there are about N (= 10^{14} to 10^{15}) atoms per cm^2 of <100> wafer surface, the number of states is 2N (i.e. acceptor or donor state)

Now, I just want to just begin with this, but I can not go anyway further. What you will see will be. I will just not go through that now. What we will be seeing will be this is most ideal case. Only the doping effect is included n this capacitance. When you have interface state density which give rise to states at the interface. They you will see that. And additional capacitance come into picture that additional capacitance will actually appear across this. I will not discuss that in detail today, but we can take it as additional capacitance comes across this.

And if you say additional capacitance comes across this, due to D it interface trap density since you have discussed that I can use the word D. It that comes in across that what would you say the effect of interface state density on sub threshold slope, it will actually increase. Because instead of C D you will have additional capacitance coming across the C d. So, you will have sub threshold slope increasing with the D.

We will see how it comes about in my next presentation. For today I will closed down with this we will continue on the threshold voltage effect of D it on sub threshold slope, and continue on the transport mechanism in the next two sessions on this.

Thank you. We will see next time.