Nanoelectronics: Devices and Materials
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Lecture - 15
MOS Parameter Extraction from I-V Characteristics

Today we will look at transistor parameter extractions, namely.

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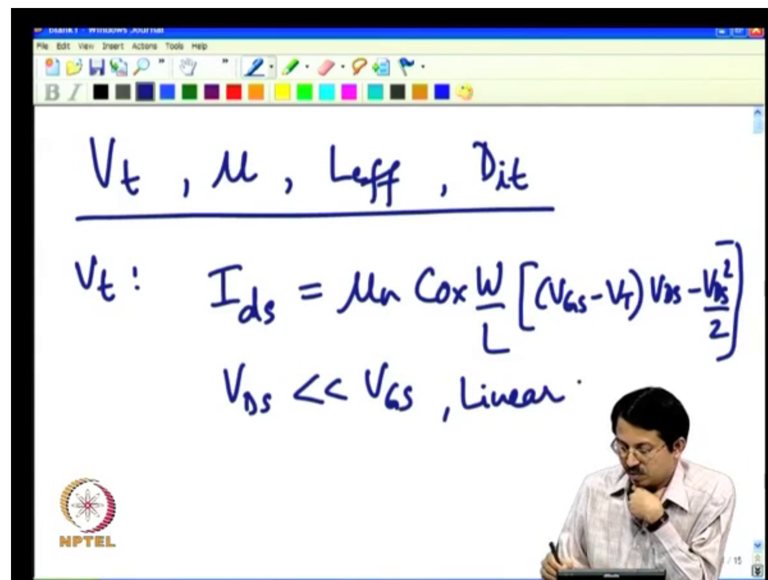

We will look at threshold voltage extraction, mobility extraction, which is a very important parameter when you are talking of transport in a fet. So, in addition to that, we will also look at what is called effective channel and ten extraction and finally, again the interface trip density extraction using a transistor structure, not using a capacitance voltage technique, but using the current measurement technique. So, then let us get started with the threshold voltage extraction. You know the, if you recall the drain current of a field effect, transistor is essentially a given by this equation.

So, you know it depending on again, whether you are in linear region or saturation region, these currents could be approximated; for example when you are in linear region. We say that the transistor is in linear region, you know when VDS is very small compared to VGS, then it is linear region of operation.

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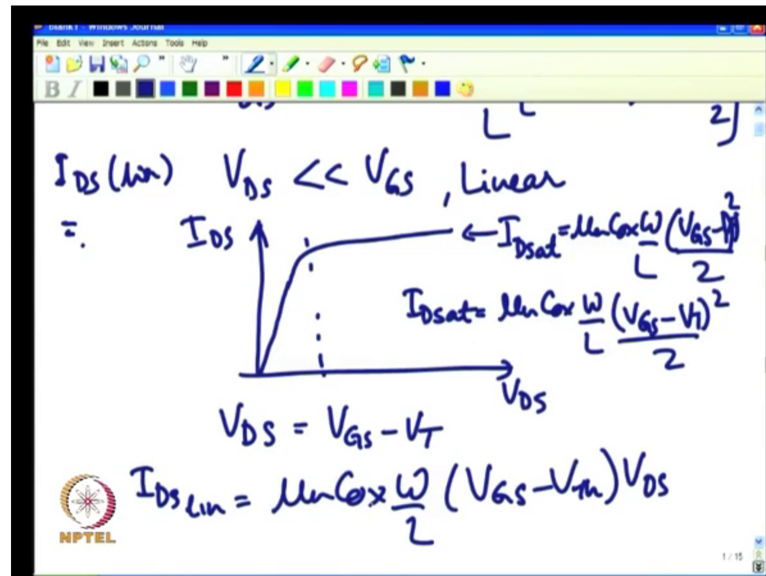

In other words in linear region, if you were look at IDS versus VDS characteristics, you know the current, will initially increase in the linear region and hence that is for the small VDS values and hence the name linear region and eventually the current will saturate.

And that is when we say, we have reached a saturation region, we reach a saturation region when VDS makes a transition to this value VGS minus V T at some value of VDS. VDS becomes equal to the gate voltage that is applied on the transistor minus the threshold voltage at that point, you know the transistor current start, start saturating and the saturation current value is essentially obtained by substituting, VDS is equal to VGS minus VT in this equation and hence, you know, you get IDS at or saturation current value as u n c ox w by l, which is essentially a dimensional parameter and the transport parameter, how good is a mobility for the transistor right.

And now you put VDS is equal to VGS minus v t and you have VDS square by 2 here VGS minus VT square by 2, and hence you essentially get VGS minus VT square divided by 2; that is your you know current in the saturation region, and let me re write that IDS at is mu n c ox w by l VGS minus V T whole square divided by 2. Now, notice that you know both in the linear region of course, in the linear region one can again make an approximation, you can ignore this VDS square term, because VDS is so small. So, in the linear region you can also approximate your drain current as what is called IDS linear that can be approximated as you know just this first term.

Mu and c ox w by l VG minus v t times VDS . So, let me write it here, IDS linear is u n c ox w by l VGS minus VT times VDS, I am ignoring the quadratic part of VDS, because VDS is very small and remember, the c ox here, is per unit area capacitance. It is not total capacitance in this equation, that is oxide capacitance per unit area and now, notice that whether you look at the linear region current or the saturation region current. There is an important parameter, which is the threshold voltage here. So, you know; obviously, it also indicates that if we can do A I V characterization, either in linear region or in saturation region, from that we should be able to extract the threshold voltage. So, let us see how one can do that.

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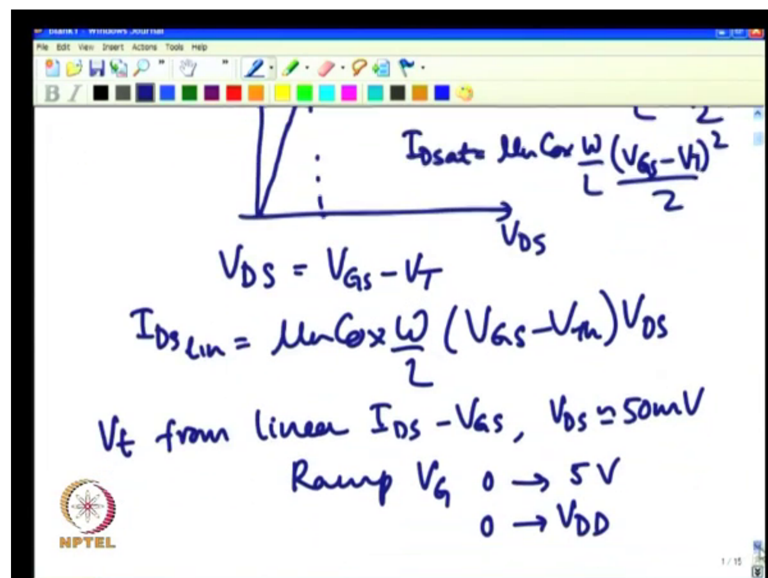

Now let us look at the VT extraction from linear IDS versus VGS characterization. So, in this measurement technique, what you do is that you put VDS as very small voltage. Let us say of the order of 50 millivolt, very small value on the drain voltage source is of course, ground end and you ramp VG from 0 to some large value 5 volt. What is that value depends on? What is the dimension of the transistor? Of course, if the dimension of the transistor is in 20-30 nanometer, with one nanometer get oxide you; obviously, do not go to 5 volt, because you know that operating voltage of the transistor itself is going to be 1 volt or 1.5 volt.

You go from 0 volt to in general, what I call VDD? Where VDD is the operating voltage of the transistor, the threshold voltage is somewhere in between. It is; obviously, more

than 0 for n channel transistor of course, less that the operating voltage and we need to determine, what is a threshold voltage value?

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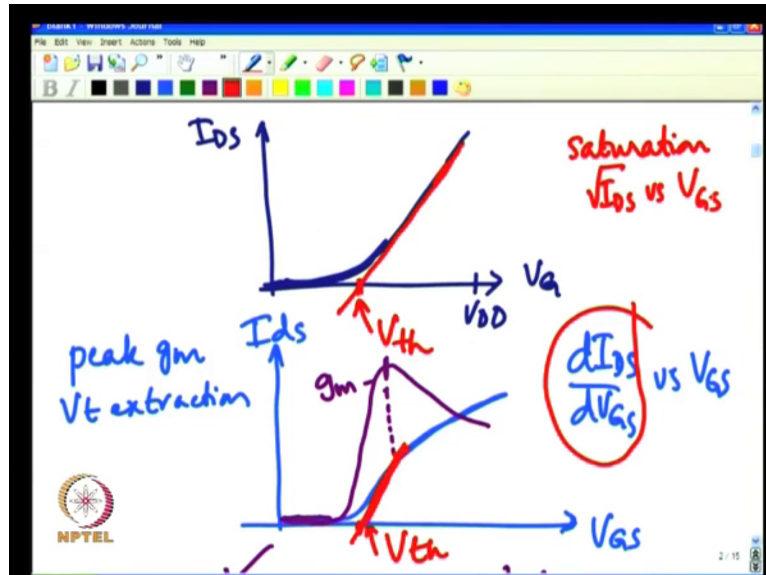

So, when you do this measurement, what you will end up getting is a characteristics which looks like this, typically this is 0, here almost 0, we know that sub threshold current is never 0, in a transistor even when VG is equal to 0, the transistor current is not 0, we have all studied that now, I am ramping from VG 0 to some VDD value. Here, this is the maximum value that the transistor can sustain and accordingly, you have different values of the current, when I plot this in a linear scale, the current here looks very small.

Now, what we also note here is that these equations that we are writing for the transistor are really valid only when the transistor is turned on, not when the transistor is of right, only when the transistor is on, we write these current voltage equation, that is when I approached the gate voltage value, which is very close to Vt. Obviously, you see, start seeing departure from these equation right, whether it is a linear equation current equation or a saturation current equation, when Vt approach is comes very close to VGS right, you start, you know having departure, but if you look at the linear region current, what this indicates is that current is expected to be a linear function of VGS. When VGS is larger than threshold voltage value so then what one could do is that, one could look at this IDS versus VGS value and try to extrapolate, this linear region behavior this looks almost like.

A straight line and say that if I extrapolate it, it is as if, that equation where to be true at this value of VGS, the current would go to 0. You see and hence I would say that when I extrapolate it, I get value here and that I call as threshold voltage . So, far. So, good, but you see in this equation even though you have this relationship, I said that IDS is linear function of VGS, I am making an assumption. You see here of course, VDS is constant, but I am making assumptions that, WLR constant, which is; obviously true, c ox is constant, which is obviously true, but more importantly, I am making an assumption. Mobility is constant, when I am ramping is gate voltage. Mobility is not changing right, but in practice, that is no longer the case, when you actually ramp gate voltage as you start increasing the gate voltage to larger and larger value, your mobility starts degrading.

We have discussed, this in one of the earlier classes, because mobility depends on large number of parameters catering due to interface and so on and so forth impurity scattering, for example, and it also depends on the vertical electric field. In the vertical electric field, which is set up by applying a gate voltage, becomes larger and larger. It will impair the free moment of electrons in the lateral direction right. So, mobility will not be constant. So, in other words, what you will inferably see when you do this kind of an IV, measurement is that you will not really get a very nice straight line like this, but instead your IV measurement will look something like this. Off course, here it is very small current and here you start having like this.

Now, the question is I need to do the extrapolation correct to get the threshold voltage for, when VG is greater than V t, but where do you want to do extrapolation, if I do a tangent here, that will give a different intercept, if I put a tangent here, that could give a different intercept and so on and so, forth. Now, there is this confusion in estimation of threshold voltage. So, a curve found for this is what we define as something called peak gm V t extraction. What it means is the following.

Now, I have got a measurement of id IDS versus VGS, now based on this IDS versus VGS, you also generate d IDS by d VGS versus VGS curve. What is d IDS over d VGS? It is called trans conductance of a transistor, you vary the input voltage and you look at the variation in the output, current and the variation of the output, current to the variation of the input voltage has a unit of conductance, but it is defined on two different ports output port and input port and hence, it is a trans conductance. So, once I have IDS

versus VGS, I can very easily create d IDS versus d VGS plot and that will look something like this typically.

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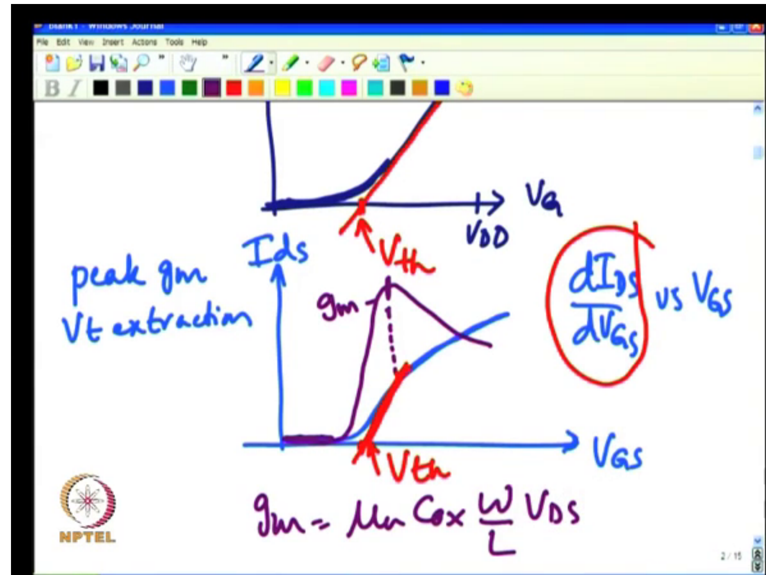

If you actually do this in the lab, your trans conductance, this is what we call gm or trance conductance and what this procedure tells us; that you do Id VG measurement and from the Id VG measurement, you also create this trans conductance curve and you locate the point, where trans conductance goes to a peak and go to that point on this axes on this curve.

Rather IDS VGS curve and at this point you put a tangent, I mean you put an extrapolation here and if you have this extrapolation done and that will intercept, this VGS axis and this is what I call threshold voltage, in other words what this peak g m V t extraction procedure is telling you is to locate a point on IDS VGS curve to put a, you know tangent there and so, they do a extrapolation to get a, you know threshold voltage value right. So, this is what is you know very popularly used in all. These you know, when you do a circuit simulation, for example, there is a V t h 0 parameter in circuit simulation and that V t h 0, parameter is typically obtained using so called the peak g m v t extraction. So, this is how, we essentially defined the threshold voltage or compute the threshold voltage from the curves.

Here, now once you have the threshold voltage, how do you get mobility? Mobility can be obtained from this d IDS over d VGS right. I have already created d IDS over d VGS

and if you go back to this equation, what is your d IDS over d VGS, you differentiate this. So, it is essentially this factor correct times, this factor I am differentiating with respect to d VGS. So, you know this goes to unity and this is essentially a multiplication factor for this VGS minus v t h. So, as a result of that my gm that I am computing here, the gm is essentially mu n c ox w by l times VDS, you know what is the VDS, because you are applying that drain voltage for your measurement.

And you know what is your w, because you have now printed that transistor and you know what is your l and you also know what is your oxide thickness, you know, you can extract oxide thickness using c b measurement. As I have already told you and you also found out what is gm and from this you can extract mobility and you know you will be able to precisely estimate the mobility of the transistor and the fact that the gm is going down here and that is essentially a reflection of the fact that mobility is actually degrading as an increase in the gate voltage to larger and larger value. Now this is one way of doing a V t extraction and the peak gm extrapolation technique that I mention.

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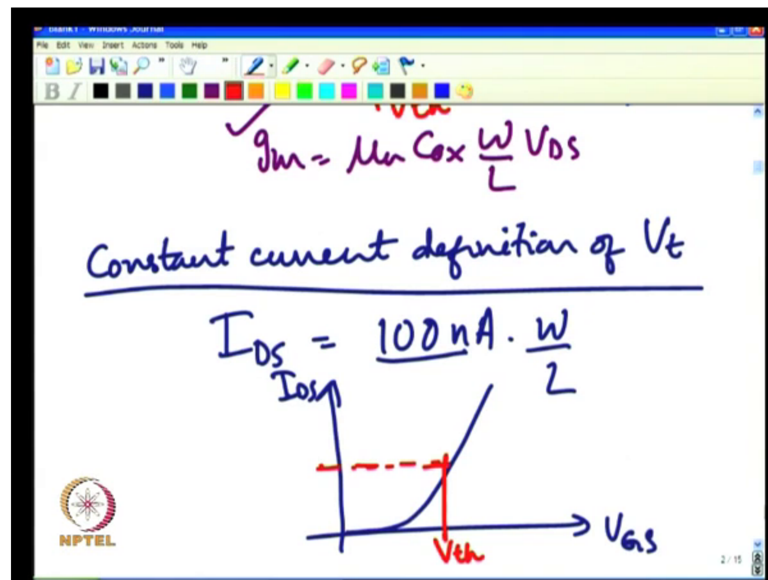

And there is another way of define V t, what is called constant current definition of V t.

What we mean by this is that, you know rather than doing all this extrapolation, we will just say that look, when my transistor gives a current of say 100 nano ampere. I call that as a threshold voltage point and that current can be chosen, you know the way based on the experience, you can fix a current, if you have to fix a current, all you need to do is

that look at that current value and you know, go to the appropriate voltage value and hence, you know what is a threshold voltage value, but you see the current is also a function of w and l of the transistor. So, what you do is the current that you choose, you normalize that current by w by l ratio.

In other words, if w by l of the transistor is more, you also have to multiply that current with the w by l factor. Only then, you will be able to get the appropriate threshold voltage value, using this constant current definition. In other words, what you are saying is that you are saying that I define VDS as that value, let me just, so, let us say I am going to define my constant current as a IDS is 100 nano ampere times, w by l what it means is that, if I choose a transistor of 1 micron w and 1 micron length, I looked at 100 nano ampere current, but instead if I choose a transistor of 2 micron length and you know 1 micron width, I would essentially be looking at a 200 nano ampere current, because w by l is large, you will get larger current and that will anyway happen.

So, you need to have this factor taken into account. So, then what you do is essentially, you look at your IDS versus VGS plot and you say, you have chosen this current, you know what is a w by l and you get the right current value and you say that, look for this transistor whenever I have a value of this current, whatever that current I have defined, I say that this is my threshold obtained, this is say another very simple way of defining a threshold voltage, wherein you do not have to worry about extrapolation and all that.

So, in literature sometimes, you will see threshold voltage defined by multiple ways, either using a constant current definition or using peak v g m V t definition peak, g m V t definition is the most commonly used. The practice of extraction of threshold voltage, there is another way of doing this threshold voltage extraction.

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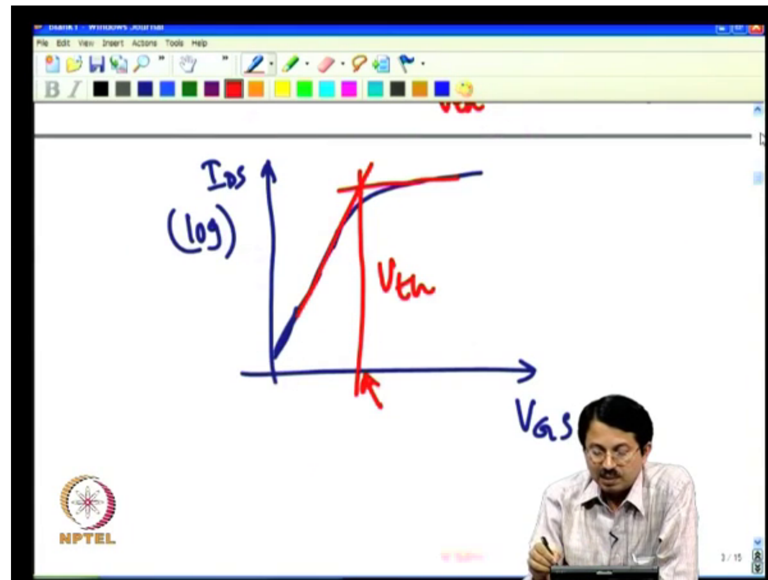

And that is if you recall, when we do IDS versus VGS measurement and if we plot that IDS with the log scale, for current remember this current looks, you know this is linear, because below threshold, current will be exponential function of gate voltage and once you reach the threshold, the current will be maybe linear or quadratic function. If the measurement is being done in a linear region, it will be a linear function of VGS, if the measurement is being done with the saturation condition, it is a quadratic function. Certainly, this quadratic variation is much gentler variation compared to this strip variation, which is an exponential variation. So, what one could say is that look, there is a transition from sub threshold to linear or sub threshold to quadratic.

I pick the transition point and call that as a threshold voltage. So, then one can define, you know then again the question is where will you put that point right. So, what one could do is that, may be one could sort of. You know extrapolate, these and sort of extrapolate this and say that look this is the point of transition, below this point it looks like a sub threshold region and above this point, it looks like a above threshold region. So, this transition point is my threshold voltage of a transistor. So, this is another way of defining the threshold voltage. Now, there are multiple ways, one can use and define a threshold voltage and accordingly, extract the value of the threshold voltage as I said, this can in linear region or as well as in saturation region. And similarly, this constant current thing can also be done in linear region or in saturation region.

And similarly, this extrapolation can also be done in linear region or in saturation region except that, when you do this extrapolation in saturation region, because the saturation current is quadratic with respect to VGS minus VT, which we have written here. So, you do not plot IDS versus VGS, you plot root IDS versus VGS that is the only difference, because root IDS will be a linear function of VGS, because of this quadratic dependence. So, that is the only difference as far as extrapolation technique is concerned for saturation region. So, the saturation extrapolation, you look at root IDS versus VGS and you know extrapolate, some that curve and then you know as a result of that you get the threshold voltage and in order to get mobility, this is the technique.

Essentially, obtain d i d over d VGS and from that you can extract trans conductance and from trans conductance, you get the mobility right and even to get. Now, when we did that, we said that you know, I know c ox, because I have computed that t ox from capacitance voltage measurement, you need not do that on a most capacity, we can do that c v measurement, on a transistor itself and once you do the c v measurement of transistor, you can get the c ox and you can do the use that c ox in this competition and you can get the mobility fine.

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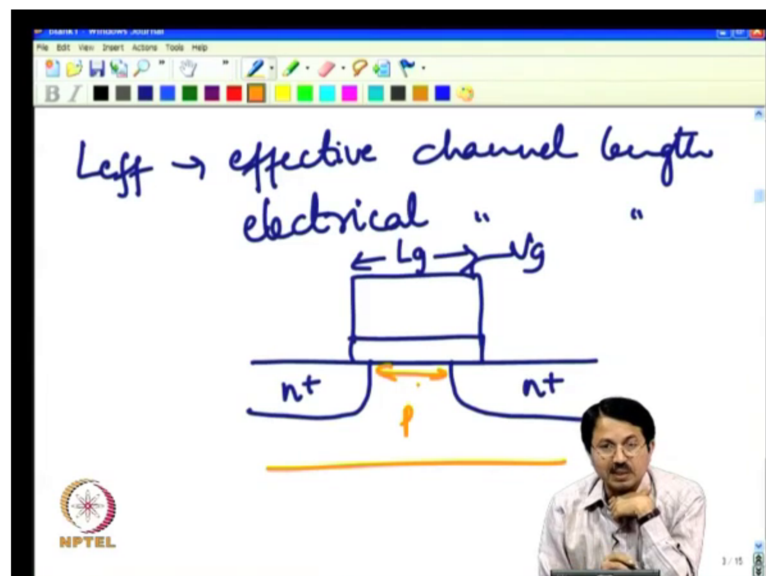

So, the next important thing that we need to find out is what is called l effective or effective channel length sometimes also defined as electrical channel length ok.

Now, first of all let us understand, you know why is it different from physical channel length. Now, if you look at the transistor, remember that you know have this gate and you know this is what we call gate length, which is l g. l g is different from l effective. You see and then what do you do; you do the un implantation and there is a diffusion and eventually your junctions will be formed n plus and n plus correct and what when we say l effective; what we are saying is the following I have made this transistor, with certain printed gate length, which you can always measure. If you put this transistor under a electron microscope, if it is an nano matric transistor and you can actually see how wide is the gate, physically you can look at it.

And then you have the junctions, but eventually, when you are doing the transistor action by applying the gate voltage, you are only varying; only the conductivity in this region you see. So, this is your respective transistor length, which is being modulated, only the conductivity of this region is being modulated, you cannot modulate the conductivity of this region, not this region because so, heavily doped this is the p region and this p region conductivity is being modulated by applying an appropriate voltage on the gate terminal. So, the question is how will you be able to measure, this in other words electrically the transistor looks as if it has this gate length, not this gate length, because I am not able to modulate this region anyway. So, you know this can be computed, only if you know what is the lateral diffusion and you know.

Fortunately, for us there is a very easy technique to compute that lateral diffusion, just by doing a electrical measurement. I do not have to do, you cannot do it by the way, using an optical or electron microscopy, because if you are doing electron microscopy as is like, this is also silicon, there are you know the same material, you know how will you distinguish the two materials, unless you do some, you know very rigorous post processing and try to see, you know how much is the diffusion, which is taking place laterally, it is a very difficult thing.

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L_{eff}: Choose trs, (transistors) W, different L

$$I_{ds} = \mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_t) V_{DS}$$

$$\frac{V_{DS}}{I_{DS}} = R_{ch} = \frac{L_{eff}}{\mu_n C_{ox} W (V_{GS} - V_t)}$$

So, what we do here is that in order to estimate this, we do the electrical measurement for l effective extraction, first of all we choose transistors with same w, but different transistors, multiple transistors that is not one transistor, different l values, when I say, l here this l is, what is there on my mask, which are used in photolithography process, you know a based on that mask curve printed some gate.

But, I do not know what is l effective, but what I will do is that I will choose this different length transistors and when we write this transistor equation as IDS is equal to mu and c ox by w by l you see in reality it is actually l effective, what is the channel length, electrical channel length of the transistor, which is being modulated and that will essentially determine, what is the current and it is, this l effective that we would like to compute and as I said, if you are in linear region, VGS minus V t times VDS, this is a linear region current.

So, what I you do is that, if I, before we go to the measurement, let us just do some algebraic adjustments. Here, let me compute this VDS over IDS, which we also called as r channel, channel resistance, what is it? It is essentially given by l effective from this equation, you know VDS divided by IDS is l effective divided by mu n c ox w VG minus V t correct. Now, we want to compute this l effective and what is this l effective, by the way l effective is l minus.

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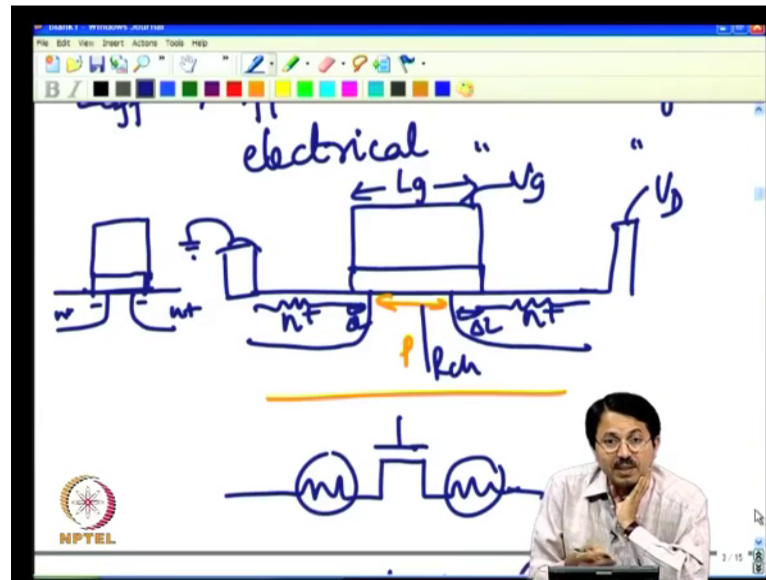

What we call 2 delta l; what is this delta l; this is delta l, there is a lateral diffusion from source side and the drain side, and these 2 lateral diffusions are exactly identical. They will not be any different, because it is all symmetric device anyway.

Fortunately, for us you see this delta l, does not depend on what is the actual printed length. In other words, if I have an another transistor, here which has not this l g value, but maybe a different l g value, even in this case, this delta l that I have here will be same as this delta l, because y is this delta l coming, we have an plantation and there is a lateral diffusion. Implantation is always at the edge of the gate, you see and hence the lateral diffusion, whether it is a 1 micron length channel or 10 micron length channel is always the same in that is, what is going to help us in getting the l effective value and that is why we are going to choose transistors of different length. So, we chose transistors of different length.

Length as defined in the mask and then on all these transistor, we do id versus VGS measurement, at linear region operation, meaning by very small VDS value and then we choose, when we do that for example, I will have curves like this IDS versus VGS for one transistor and then IDS versus VGS for a different values, different value transistor and so on and so forth.

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So, in all these cases, what I will do is that, I will choose a particular value of VGS in all these transistors and at that value of VGS, I find out what is my IDS and I also know what is my v ds and hence, I am calculating r channel, at you know for different transistors that I have, because I am choosing VGS minus VT.

I know V t, I know I am choosing VGS; I am doing this for the same VGS minus V t value on all transistor. So, I know this, I know this anyway and I do not know, l effective, I am trying to get l effective, but I am computing r channel. Now, what I am going to do is the following.

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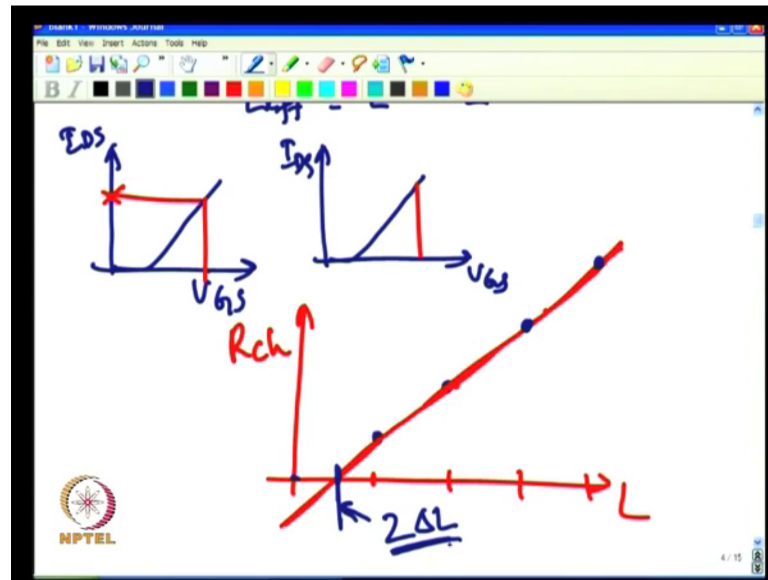

All I am going to do is that I am going to construct a plot of r channel as a function of l and what is this l by the way l is l on mask. I know l on mask was 1 micron, 2 micron, 4 micron. So, I have 1 micron, here let us say and for 1 micron I got some r channel value and for 2 micron transistor I got some value and so on and so forth, I have for multiple transistor measurement, I have got all these values and then what I know, I have got different values of these r channel.

Then I am going to sort of connect all these and make and extrapolation. So, this extrapolation is coming by actually measuring this resistance on different length transistors. So, what is this telling you, all this is telling you is that, at this value your r channel goes to 0 and what is our r channel equation, r channel equation is this, what is this by the way, l effective, l effective is l minus 2 delta l correct. So, if this is going to 0, then l should be equal to 2 delta l at that point correct. In other words, when l is equal to 2 delta l, l effective is 0 and hence, r channel is 0.

So, in other words by actually looking at the intercept of this straight line, where r channel is 0, I know that this should corresponds to 2 delta l value. So, in other words what I have been able to do is to really get that extent of lateral diffusion in all these transistor and all these transistor the lateral diffusion is the same then, then if I want to get l effective for 1 micron transistor, I am going to subtract 1 minus this 2 delta l value that is my l effective and l effective for this is again 2 minus this value and. So on and so

forth. So, that is how you compute l effective value by doing a electrical measurement and from electrical measurement, getting the channel resistance and from channel resistance to engine extrapolation for 0 channel resistance and hence, getting 2 delta l value.

This was quite you know in older generation technology, but in new generation technology, there is a problem with this technique and that problem is the following right and that is, I made an approximation, I may sort of I told you that I do this IDS VDS measurement and I do VDS over IDS and that gives me channel resistance. But in reality, it not only gives a channel resistance, but it gives this channel resistance in series with a parasitic resistance correct.

Because the way you have, we have discussed, this is a parasitic resistance here, there is a parasitic resistance here and eventually your drain, contact is coming, here this is where you are applying drain voltage and your source contact is coming here, this is where you apply source voltage when I do VDS divided by d s, I am measuring this whole resistance, this whole resistance is r channel plus r s d or r parasitic, any other external resistance outside this transistor. Other words, this transistor in reality is an ideal transistor, which is gate controlled in series, with these parasitic resistance correct.

So, these parasitic resistances will affect your analysis, because you are earlier mentioned VDS over IDS, only channel resistance, but it is not. So, VDS over IDS is r channel plus r parasitic and that is what you are measuring correct. So, then what will you do right; how will you extrapolate; you know this curve and get the l effective right. So, there is a very interesting technique.

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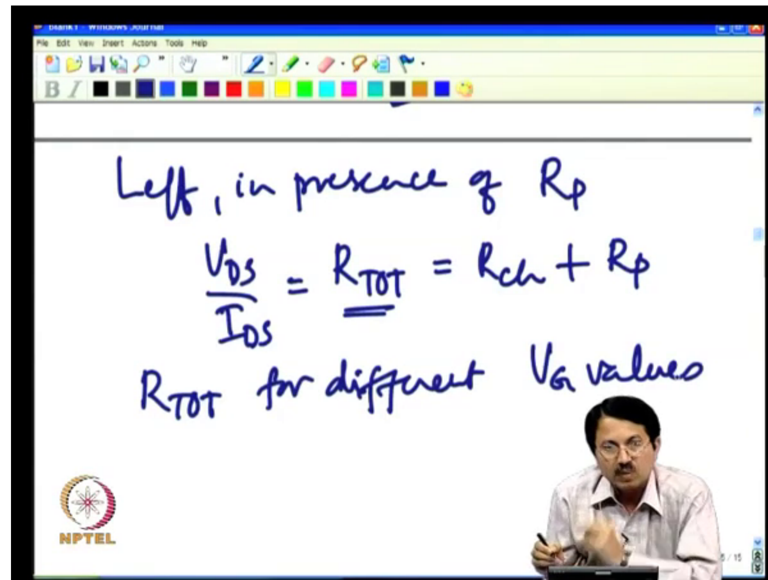

So, that it is now, a l effective measurement in presence of I will say r parasitic, what I mean by r parasitic is that VDS over IDS is really what is called r total which is r channel in series with r parasitic. When I am doing VDS over IDS r total essentially I am, you know measuring both r channel and r parasitic.

Now you see there is something interesting, one can do and that is r parasitic is fixed, given a transistor r parasitic is fixed, but r channel depends on gate voltage value. You see what has happened is that there is a new variable that has come in, if I have to get read of this new variable, I need another knob to play. So, what I do is the following, earlier I was extract constructing this graph for only.

One value of VG, but now, I will construct this graph for multiple values of VG the idea of doing is for multiple values of VG is that by doing. So, I am modulating r channel, but r parasitic is always the same and hence, I should be able to get r parasitic and hence, 2 delta l both will come out. So, the technique here is that do your r total measurement for different VG values, if you do that what you will get is something like this.

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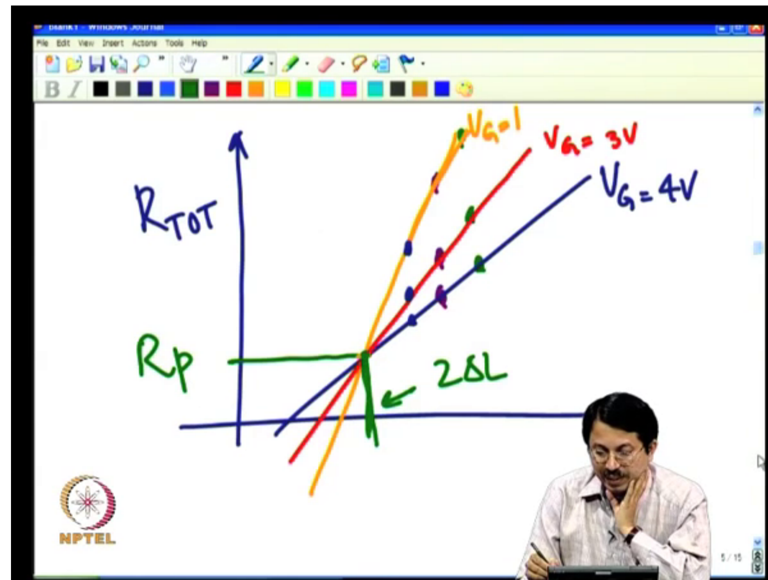

Again, I am plotting for different length transistor. Again I choose 4 or 5 different lengths transistor. Now, what I am plotting on the y axis is total measured resistance, I do it at one value of the gate voltage.

You get a curve, which looks like this. Let us say, this is for you, know VG equal to 4 volt, I do it for another value of gate voltage that probably will look like this and let us say, this is VG equal to 3 volt and you know, you do it for another value of the gate voltage, you will essentially get a curve, which would probably look something like this. Let us say this is VG equal to 1 volt very interestingly, all these curves will intersect at some point, here what are you doing, here really VG equal to 4 volt your r parasitic is constant, r channel has certain value when I decrease the VG value, r channel increased, because VG is decreasing and there are not as many electrons and I am modulating r channel.

But r parasitic stays as it is right that is why the resistance increases. Here, for a given channel length transistor. Remember, I am doing all these measurements for different values, of the channel lengths right and there is one transistor with this channel length, another transistor with the this channel length and I really constructed these transistors. And I am doing these measurements on multiple transistors. And from there I am extrapolating, but I am not going to look at this point, but I am going to look at this point, because this is the point of interest for me, what this is going to tell you is that the

fact, that all of them meet. Here, you know that is, what is your parasitic resistance, r parasitic resistance, parasitic resistance constant here at this value, and in fact, at this value your r channel is 0, that is why all of those are giving your constant resistance.

You see, that is all of them are really meeting at this point. If you look at this equation, when r channel is 0 r, total is r parasitic and r parasitic is same no matter, what is the length of your transistor, it is not going to change and hence, all of them start from this point. Beyond this, you see as you start, you know applying different gate voltages, for the same parasitic value of the resistance r channel, here is much lower for this transistor, at 4 volt compared to 3 volt. And hence, I get a, this curve at 4 volt, this curve at 3 volt, this curve at 1 vote and that is why all of them meet at this value and this is r parasitic and this is 2 delta l. Now, even though the transistor has lot of parasitic resistance, I can simultaneously.

Get the value of parasitic resistance as well as the lateral diffusion that has happened and once you get 2 delta l, for all these transistor, I go back and subtract this 2 delta l and get l effective right. So, this is a very interesting way of getting electrical channel length and this is important, because once you meet transistors in large number of channels, you know it is very difficult for every transistors length to be measured optically or using electron microscopy, but electrical measurements are very fast and nondestructive right. So, by doing this electrical measurement, you can actually do a lot of analysis on these transistors.

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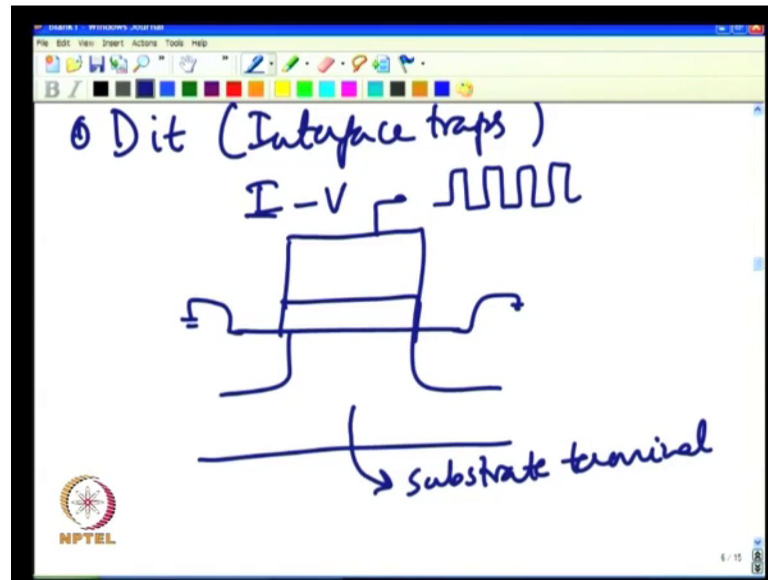

So, one last topic that, we will look at today, is to measure the Dit or interface traps from transistors.

That is using i v measurement, you know some kind of a current voltage characteristics measurement and in fact, you know I must tell you the way, this was discovered was really a serendipity I mean. In fact, you know people, who are doing measurement on transistors for some digital application, digital application what you do you, essentially apply a pulse or a square wave kind of a voltage, you know 0s and 1s is what is applied to the gate voltage right and you typically, expect that you know you apply some source voltage, you have applied for drain voltage, you have some current going from source to drain, but during such measurement, when you are applying ac waveform on the gate. There was some kind of a current that was measured at the substrate terminal.

And you know, this was at the beginning, you know very unusual, it is important that you know if you doing some experiments, if you get unusual resistance, sometimes it may be beneficial to really sort of, do more analysis on that unusual result, that may have some very interesting observation, hidden there and eventually it was discovered that the current, that comes at the substrate, which was unexpected, is really due to the interface traps and more specifically if the interface trap density was very high, the current was very high and if the interface trap density was very low the current was also very low. In

other words, the current was directly proportional to interface trap density. So, this turned out to be a very surprising and a very useful technique.

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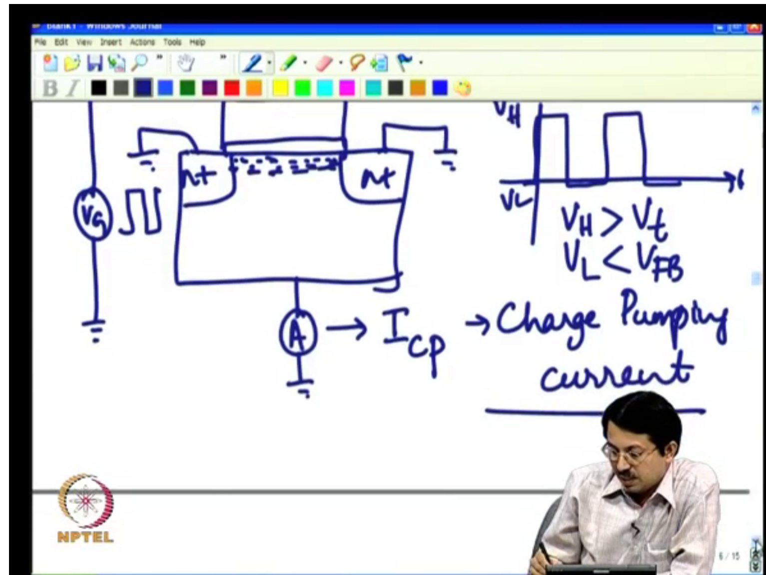

Now, let us look at, you know what is happening, really in terms of the experimentally setup, it is a very simple experimental setup. So, what you do is the following.

I have a transistor, you can ground the drain terminal, you ground the source terminal and you essentially apply in ac waveform square, waveform to the gate voltage and you connected dc ammeter to the subset terminal and you measure this current, which is also referred to as I cp and I cp stands for what is called charge pumping current. So, what happens here, there is a, there is a certain condition, here VG is being gram d c VG as a function of time.

This is done over time right, this vg essentially is going between v high and v low, there is a important conditions to do this charge pumping measurement and that is v high should be greater than V t and v low should be less than v f b, where v f b is the flat band voltage of the transistor and VT is the threshold voltage of the transistor. This is an important condition, let us say, we satisfy this condition, then what happens; let us do this analysis, if my gate voltage is at V h level, because V h is greater than V t the entire transistor will be inverted.

Correct. So, it will have large number of electrons.

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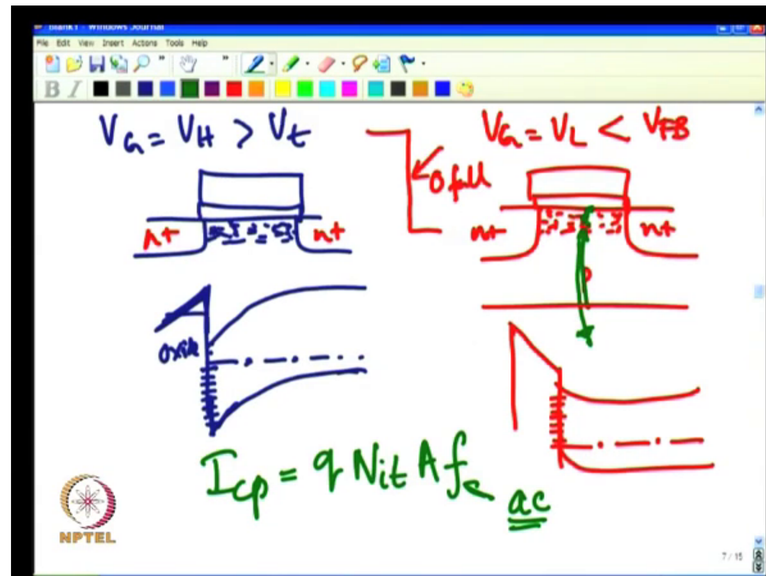

So, let us do that analysis, here for VG is equal to V h, which is greater than VT. What you have here is, large number of electrons, these are all electrons, we will also look at the band picture, in the minute why do not, we just do that here. So, if you have to do the band diagram, here what will happen for the band diagram, if this is your oxide you applied a positive voltage, the oxide and this is how the band diagram will look. Lot of electrons will be there for me, level will be very close to conduction band, most of the entropy traps are filled with electrons. Now let us look at the condition VG is equal to v l is less than V FB. Remember, V FB is a flat band voltage, if you are below flat band voltage then you are in accumulation condition correct. So, then what happens, if you look at the transistor, this is your n plus region, this is you, p region n plus p region. Here, you will have lot of holes coming in. Now, if you have to look at this band diagram, this band diagram will probably looks something like this accumulation condition,

But how did I go from high to low, I went from high to low with a pulse, which has let us say for the discussion for the time being 0 fault time, fault time is 0 from high to low. I have come down instantaneously, when I came down instantaneously, from high to low, what would happen, just think about it of course, hole will come and accumulate, because p is a majority carriers, lot of holes are available, they will come and just accumulate at the interface, but what happens, the interface trap remember when we were discussing about the interface traps, I have been saying that interface traps have

time constant, meaning the traps. Which are holding the charge, they cannot leave the charge instantaneously, that time constant, maybe from, for fast interface traps, it could be from micro second to millisecond. I am saying that, I am doing this transition at instantaneously, fall time is 0.

In other words, when I created this, these interface traps eventually would like to empty out, because the ferny level position is below the interface trap level, but it does not happen instantaneously, what happens, instantaneously is large accumulation of holes. Now, what happens? These traps, which has still filled with electron at time t equal to 0, that fall time they start coming out, electron start coming out slowly from the interface trap, because the steady state condition is that all the interface trap should become empty. So, when these electrons are coming out, here this series hole c of holes you know.

In other words we say there is a electron hole recombination, these electrons which come in here, they get combined with the hole and that will get replaced instantaneously, because it is a huge majority career p type that I have. So, all the electrons, that come out will effectively constitute, a current at the substrate terminal, because for each electron that is coming out, you need to provide a hole to recombine and that hole is essentially provided from the substrate terminal right. So, if you have large number of interface traps, there are large number of electrons trapped in and hence, they result in large number of electron hole recombination and hence, large number of current charge pumping current. So, this charge pumping current happens at this instance, as well as at the next instance, you know whenever I go from low to high and high to low right. In all these instance, the charge pumping current is like a spike right and what I do is then integration of this you know a averaged out that is why I have a dc ammeter here right.

I measure the total current, if your frequency is enough, you know that sort of averages out, over that frequency that you have. In other words, your charge pumping current it turns out is given by q times n i t times of course, the area of your transistor times frequency, this frequency is essentially your ac frequency that I have, if you have larger frequency, you have more current, because in a, in one second you have more such transitions and their in a lot more times, you have filled and empty electrons and holes in the traps all that average doubt and you have more current. So, now, n i t is total traps, because what I am doing from in virgin to accumulation is I am spanning the entire trap density.

From flat band 2 to 5 b condition in the band gap right. These entire traps in this region are either filled or empty and they are responding to this fast wearing trap. So, as a result of that if you go to compute i c p. You know what is your frequency of operation and you know what is your area and you know, you would be able to compute nit and from nit you should be able to compute Dit and in fact.

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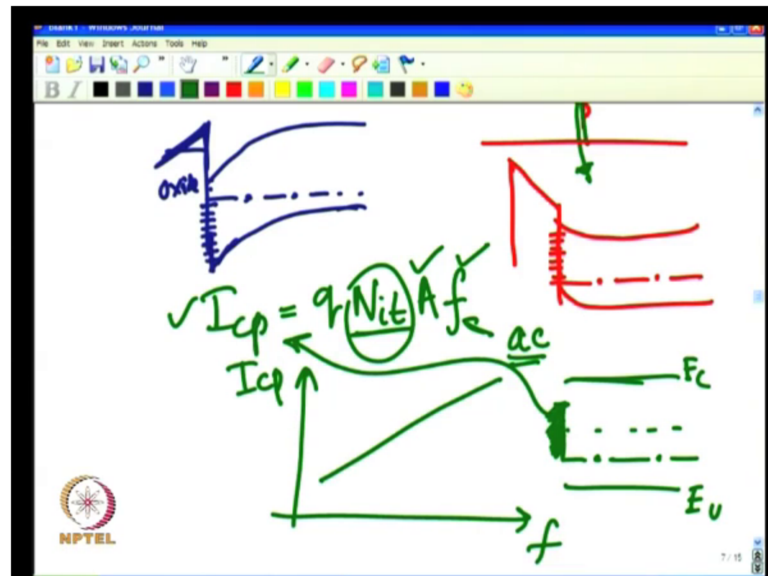

If you actually do this measurement at different frequencies, you will see that your I cp versus frequency will be linear and this is again a signature of the fact, that this current is coming due to filling and emptying of the traps, when I am going above threshold voltage and below flat band voltage right; if you do not do this above threshold and below flat band. You will not be able to get this kind of a current. So, this is a very sensitive, current sensitive technique, you know it. Sometimes even more sensitive than the capacitance measurement, techniques capacitance measurement techniques have some limitations.

Whereas, the charge pumping technique is a very sensitive technique and you know there is lot of literature available in terms of measurement, using charge pumping and their variants of charge pumping current, which can even give a distribution of interface traps, inside the band gap, because now what I am getting is a integrated value of interface traps between flat band to inversion condition right. What I mean by that is, you see, if it is silicon with certain band gap right and this is mid gap right, now flat condition is

formula well is here below 5 b, I mean 5 b below mid gap, when I reach inversion ferny level will be 5 b above mid gap.

So, this is the region that I am spanning all the interface traps, in this region are contributing to this current here that is the integral of the Dit over this region right. So, what I am told, you just now is that, there is variations of charge pumping current, which can even give you distribution of traps in energy, in this region, but that is final detail of charge pumping measurement. We will not really discuss about that, but suffice it to say that you know by doing this very simple technique, which is very accurate, you should be able to measure interface trap density, in transistor very accurately.

So, then let me just wrap up and summaries various parameter extractions that we looked at threshold voltage, as you know is a very important parameter. We can extract the value of threshold voltage using the so called peak g m extrapolation techniques or using constant current V t definition or using sort of sub threshold and linear transition, you know as we discussed.

Earlier, then mobility can be extracted by looking at trans conductance. Trans conductance is essentially change in drain current, for a given changing gate voltage. And hence, you extract mobility; l effective is a very important parameter, which is an electrical equivalent channel length of a transistor. And, in order to extract that you choose transistors of constant w, but varying length and do some simple iv measurement and be able to extract l effective. And finally, charge pumping is a very powerful technique to extract interface trap density.

So, let us stop at that.