Nanoelectronics: Devices and Materials
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Lecture - 14
MOS Parameter Extraction from C-V Characteristics

In the last lecture we were discussing about various non idealities in MOS capacitor system. We did talk about work function difference fixed oxide charge, and interface trap density, and how it impacts you know the capacitance voltage characteristics. You know today we will continue the discussion and look at some more non idealities. And after that we will look at parameter extraction from a capacitance voltage characteristic.

So, just to sort of recap what we have said earlier.

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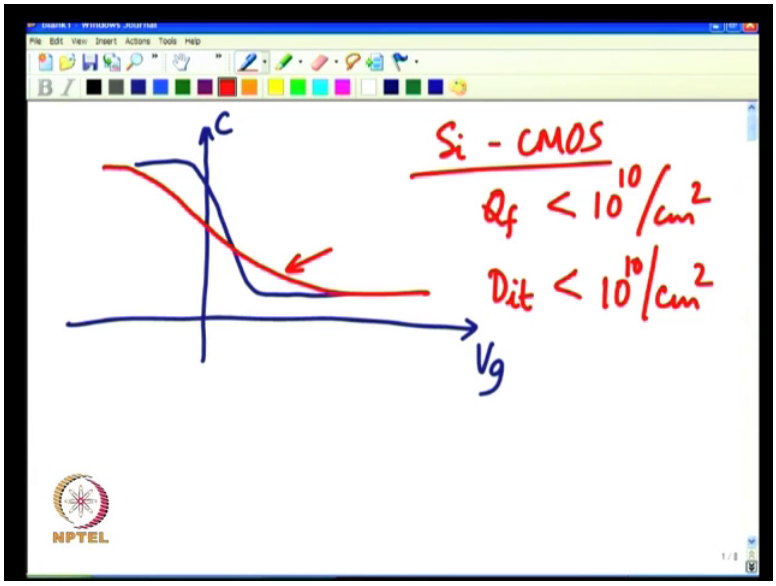

If you have a p type substrate then the capacitance versus voltage curve for an ideal situation will look like this and if it is only fixed oxide charge, this will essentially shift to the left because fixed oxide charge is invariably positive. And on the other hand if it is due to combination of both fixed oxide charge and interface trap not only will there be a shift, but also there will be a stretch out and that is what we said the C V could probably get stressed out something like this, right. And this could be in the presence of both fixed oxide charge and interface trap density, depending on how much is the interface trap density and how much is the fixed oxide charge.

Now, typically today if you are looking at the silicon CMOS technology, we have figured out ways to really minimize both fixed oxide charge and interface trap density, today routinely we get you know the fixed oxide charge in the range of less than you know 10 power 10 per centimeter square this is number, if you want to actually get the charge you multiply with q that gives you the charge. And similarly the d it that is interface trap density could also be of the order of 10 power 10 per centimeter square, you know this is the kind of technology that we have you know.

But in the olden days in the early days of silicon technology, in this used to be very high in the range of 10 power 11, 10 power 12 per centimeter square kind of numbers right, those were very high numbers, but we have come up with various process techniques to overcome all these issues. And one other thing that off course if you start looking at some other dielectric not silicon oxide or silicon if you are developing a new dielectric then of course, you could start with very high trap density, then you need to optimize the process to minimize those trap density.

Similarly, today we are talking of building transistor on different substrates like germanium or you know compound semiconductors, even there when you put an insulator on top of such a semiconductor your trap density may not be 10 power 10, you know your trap density is not surprisingly will be in the range of 10 power 11, 10 power 12 kind of numbers. But then you need to optimize it and bring it down to these numbers, if it has to compete with the kind of technology that silicon has today.

Now, in the context of fixed traps and interface traps there is one other kind of non idealities which is what is called slow interface traps.

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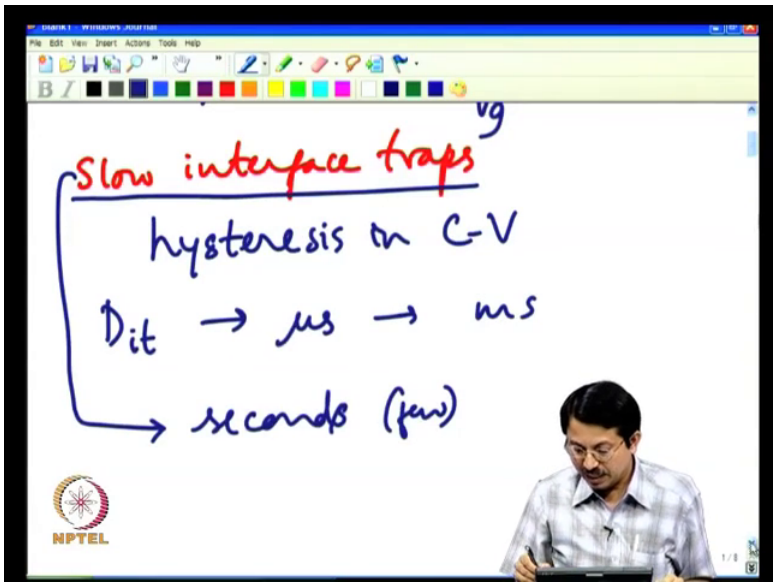

Now just quickly look at this, typically in silicon oxide system you will not see this slow interface traps. What it means is that you know it is not quite interface trap, but it is not also fixed charge it does vary but it varies slowly. Now what is the implication of that you know in slow interface traps could lead to what is known as hysteresis in CV characteristics.

Now, when I say slowly I need to sort of qualify that statement, when I talk of interface traps I did tell you that interface traps do respond to the slow varying. I mean the signal that is applied to the gate if it is slow varying, that is because they have certain time constants to interact with the channel charge so that they can exchange charge. Typically, the interface charge traps that we have, they have time constants you know anywhere from you know micro second to millisecond, you know may be a few tens of millisecond. And that is why we call them you know they are fairly fast, but if you have on the other hand if you talk of fixed charge it has time constant, which is sort of infinite meaning it does not really change. Once it is positive it just stays positive it does not get discharge and become neutral you see that is another extreme.

But if you are oxide that you have put in has you know some extra defects, they are may not be exactly at the interface may be little away from the interface. Hence, the time constant is little slower, then you know you may have what are called slow traps and

which may have the time constants in a few seconds, now what is the implication of this, right.

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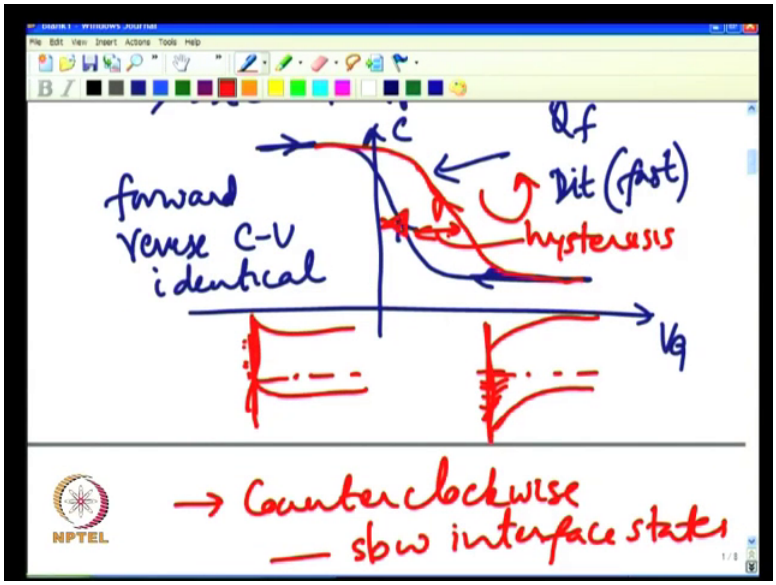

Typically whenever you do a cv characteristic right, that is capacitance versus voltage characteristics you can sweep the gate voltage either from negative voltage to positive voltage or from positive voltage to the negative voltage and you can do both in which it is called a bidirectional CV characteristics. I have set the voltage from negative to positive and come back from positive to negative.

So, ideally you know if you do this in the forward direction if your C V looks like this, in the reverse direction the CV will essentially overlap on top of it, this is what you will have ideally indeed this is what you will have in most of the silicon devices. Today you will never see any hysteresis that is forward and reverse CV are identical. Now this will happen if you have fixed charge even if you have interface state traps, you know they will not really fast interface traps that is they will not really give in rise to any hysteresis because you know they are responding. You know typically the CV measurement time frames are few seconds right, maybe you know you go back here from minus 5 volt to plus 5 volt.

Let us say you know that may take a few second and then you start coming back that is how your CV characteristic would look, now what happens with the slow interface traps is that they do not respond during the CV space, because that sweep is reasonably fast for

them, but once you are here you know you are essentially spending time. Once you reach this band bending, the band bending does not change in inversion it is more or less constant and similarly the band bending in accumulation is also more or less constant.

Now you know going up like this coming back like this will be a matter of a few seconds, during this time they would respond meaning only at this extreme and at the extreme they will respond, because they are relatively slow, they do not respond during the this CV free. So, what I mean by that again recall our discussion at this point our band bending will look something like this.

This is Fermi level accumulation condition at this time the band bending will look like this inversion condition remember and you know here ideally you know all these trap should be empty and all these traps should be filled correct because below this Fermi level that is what we are looking at. But what happens with respect to these so called slow traps. So, they may not be exactly at the interface, but they may be little bit away from this interface let us say somewhere here. And hence they take little longer time to respond, they also respond to the level of Fermi level position that you have.

So, what happens is that let us say out here you have all the traps empty and when you come here you fill all these traps right with the electrons and now when you are going back you have those extra charges in these traps and these extra charges stay put when you are doing this CV sweep right. So, because you have these extras traps extra charge in this case, when I have come from negative to positive I have this condition and when I am waiting here during this period and while I am coming back all these are now filled with electrons. Now you see when I am going back I have extra negative charge here.

And because there is an extra negative charge the CV will not trace the original CV, the CV will actually go back like this. Why go back like this because there is an extra negative charge, whenever there is an extra negative charge the curve shifts to the right, if there is a extra positive charge the curve shifts to the left. So, it goes back like this in other words forward sweep will be like this a reverse sweep will be like this. And hence there is what is called histolysis and whenever there are slow interface traps, the hysteresis which always counterclockwise.

Notice here while you are coming here the CV was like this and at this extreme you filled lot of electrons here and the charge is you know negative and hence it went in here

and here you have a lot of positive charge, the CV will come here so and so far. Whenever first of all if you see a hysteresis in CV characteristics that is indicative of the fact that there are so called slow interface traps which is also not good, just as fast interface traps are not good even slow interface traps are not good.

And if the hysteresis is counterclockwise, that is clearly a signature of the hysteresis is coming due to slow interface states and you know it turns out you could also have a hysteresis, which we rarely have unless you know today we take lot of care in making sure that, there are no impurities in terms of so called mobile ions such as sodium potassium so and so far, right.

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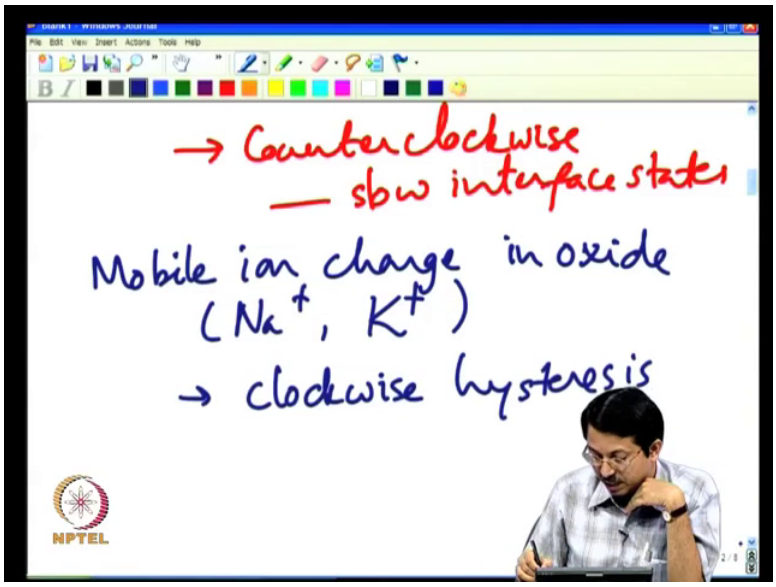

If you have mobile ions then you can also have a hysteresis which is called clockwise hysteresis, hysteresis will not be a counterclockwise hysteresis a hysteresis will be a clockwise hysteresis. So, clockwise hysteresis is not an indication of slow interface traps, where as if you have slow interface traps there is going to be hysteresis and that is always going to be counterclockwise as we discussed.

Now at this point it may be worthwhile to also discuss the non idealities of mobile ion charge, which as I said is very rare, but again if you mess up with your cleaning procedure and instead of taking quartz, where you take a Pyrex glass to clean your device silicon, pyres is a very good contaminant of sodium and potassium right. When we talk of mobile ion charge in oxide we are essentially talking of sodium potassium so

and so far. Which are you know metal impurities, you know positively charged metal impurities, if you have this then you will always have again a hysteresis and that will be a clockwise hysteresis; it also becomes clear why that is the case.

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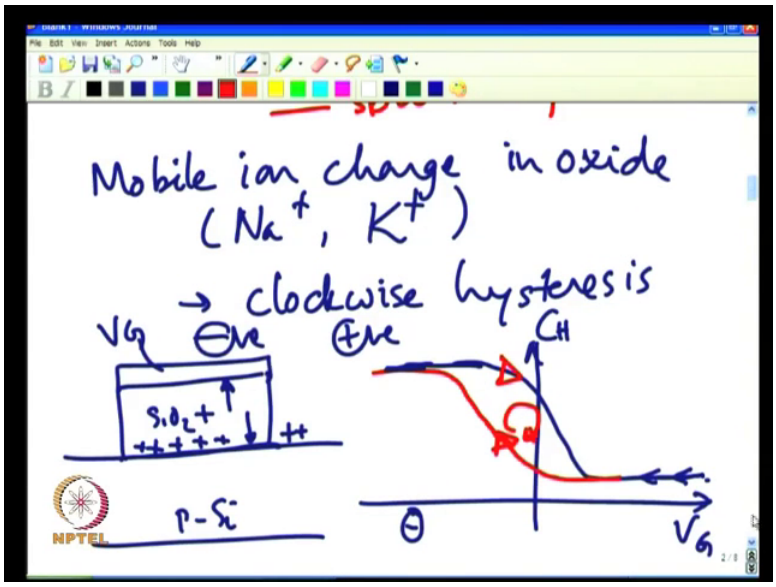

First of all when we say mobile ion charge what it means is that, I have this MOS capacitor there is an oxide here, this is our Si O 2. Now this oxide is contaminated with this mobile ion. So, these mobile ions can either move to this interface or move to this interface depending on your voltage on the gate electrode.

When I have negative gate electro voltage, all these charges will move away from the silicon interface to this interface remember, what we said last time the charges which are closest to the interface have the maximum effect on CV. In fact, if the charges are out here then absolutely no effect on CV characteristics.

On other hand if I have a positive voltage, then all these charges will be repelled because of the positive gate voltage and they will all move to this interface. But again this movement you see takes time it will not respond instantaneously and that time is also in the order of few seconds. So, now just imagine what will happen because of this right I have this gate voltage and this capacitance curve, let us say I started with negative gate voltage and negative gate voltage all these charges are here. So, there is no effect felt because of the charge and the CV will look very good like this.

Now, there is a positive gate voltage and because positive gate voltage will stay there for certain amount of time, all these charges by this time will drifts towards this and will accumulate here. So, when I am doing my reverse CV by this time all these charges would have come here. Now you have all these positive charge. So, whenever there is a positive charge the CV will go towards the left, remember that right we have discussed all this in the last class.

So, when I am doing the reverse CV, the reverse CV will go like this again I go here for some time all this charges will go back now to this electrode. So, when I am doing the forward CV see you will again come back here, because now it is does not feel this positive charge, all the positive charge are repelled all the way to the gate electrode and hence it is effect is not at all felt. So, when you have this mobile ion charge the hysteresis as you see is clockwise, this is what I meant clockwise hysteresis.

Whereas, here the hysteresis is counterclockwise, you know the hysteresis look like looks like this you know there is a counter clockwise sense for this hysteresis. So, as I said you know if you have really these mobile ion charges for whatever reason you may see a clockwise hysteresis and if you have these slow traps because you are doing different dielectric in silicon or new substrate, again you may have slow traps that will give you counter clockwise hysteresis.

Ideally we should not have any hysteresis you know forward and reverse should be exactly on top of each other, that would be the ideal condition. You could have fixed charge fast interface trap, but sow interface traps should not be present and that is where you would essentially need to optimize your process. And you know make sure that your slow interface traps are you know eliminated from the system that 2 more rather 3 more non idealities that I wanted to discuss.

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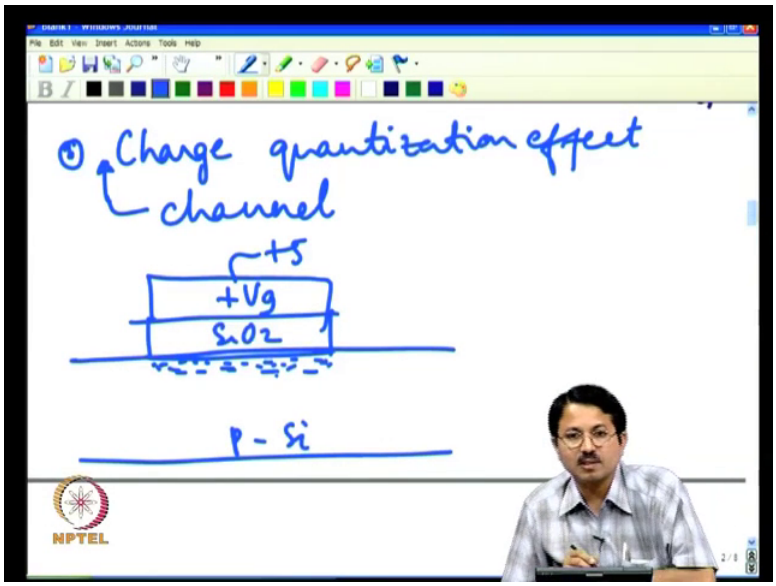

You know the next important thing is what is called this charge quantization effect and more precisely also referred to as channel charge quantization, the charge that you have and it is especially problematic when you are in inversion condition and let us just look at what it is right. So, this is p type silicon again let say I have positive gate voltage VG and this is Si O 2, when apply let us say plus 5 volt I have inverted this and you have lot of electrons here, this is what we call channel charge. Now if you look at in this direction, if you look at the band bending in that direction, ok.

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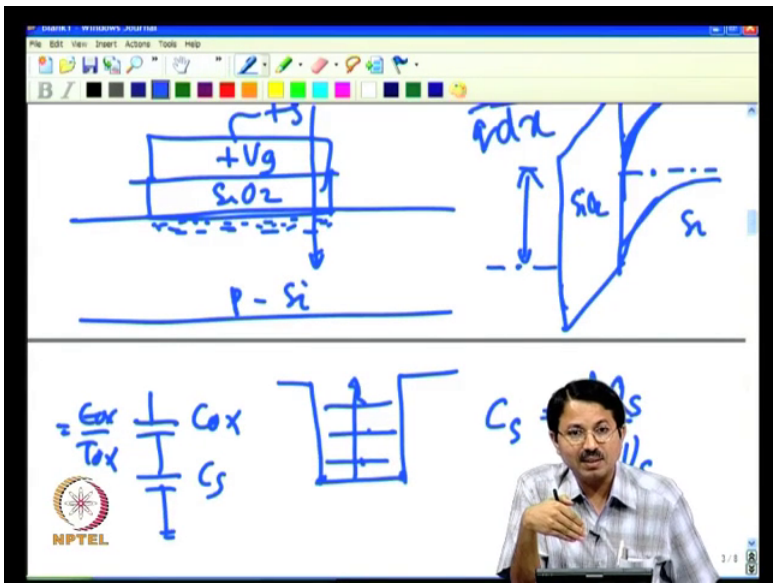

What you will essentially have is the following right, this is your oxide you applied a positive voltage to the oxide and let say this is your Fermi level here and there is a band bending which would look like this ok, silicon band has band and that is why it is p type here and it is n type here I have reached inversion condition. Now where are these electrons, all these electrons are supposed to be very close to this interface you see this is oxide as you know Si O 2 this is silicon and I have applied a positive gate voltage and hence that positive gate voltage corresponds to this distance that you have, you know separation of these 2 Fermi levels is essentially the applied voltage correct.

Now, what happens in modern day device all the nanometric device right, they have extremely thin oxide first of all remember and thin oxide has increase the electric fields right, electric field is essentially dependent on voltage divided by thickness of oxide. As you know we have not really followed constant electric field scaling theory. So, fields have been increased that is 1 aspect, oxide field has increased and oxide filed is related to silicon field also right and the silicon field not only depends on the oxide thickness, but also depends on the doping concentration. If you have a high doping concentration the depletion width is small and you are dropping at voltage whatever silicon voltage over a very narrow distance and that excess will beats this and hence the fields will be large in silicon and if fields are large remember we have discussed this electric field is gradient of band bending correct, we have a 1 over q d by dx correct.

That is this band bending that we have how fast is this band bending or the gradient of this band is directly proportional to electric field, if we have higher and higher electric field these bands bend more and more sharply something like this, very sharp band bending indicating that fields are very large. Now something interesting happens and that is the electrons which are here they almost looks like a particle in a box right, in other words you know what do I mean by particle in a box is that if we have a potential well and if you put electrons in a potential well, this electron cannot take any arbitrary energy right the energy of this electron will be quantized, ok.

There are only certain modes that are allowed because of a wave function of the electron should go to 0, at these points because there is a huge energy barrier electrons cannot really you know exists beyond this point based on the wave nature and that will quantize the energy electron can only take discrete energy it cannot take continuous energy. In other words what happens here this is almost like this not quite it is not like a rectangular

potential well, but it turn the less it looks like a potential well. And hence the energies of the electrons will be quantized and what it means is that the number of states available that goes down and hence the number of carriers will also go down, right.

Remember the total number of carriers is probability of the occupancy which is governed by the Fermi direct statistics, multiplied by the number of allowed energy states and what is happening because of this quantization earlier any energy allowed for the electrons. Now there are only fixed energy levels that electron can take and hence this is a phenomenon that is called inversion charge quantization or channel charge quantization.

Which reflects as if your threshold voltage of the transistor increases, effectively that is 1 aspect that is not the end of the story, there is also remember the semiconductor capacitance in inversion we say, dQ s by d psi s and of course, there was a negative sign here and we said in inversion the for a small change in potential, there is a large change in electron concentration. And hence when we add this equivalent combination of C ox in series with C silicon, we said C silicon is infinity or very large compared to Cox.

And hence, the net capacitance becomes Cox in inversion right, but now that is no longer the case for 2 reasons C ox itself has gone up because C ox is epsilon ox by T ox because T ox went down C ox went up right that is 1 part of the story and Cs will not be very large because the dq psi s by d psi s will not be large, because there are only finite allowed energy states, for a small change in the surface potential the electron charge will not change as rapidly as it would have earlier right and hence it degrades your inversion layer capacitance.

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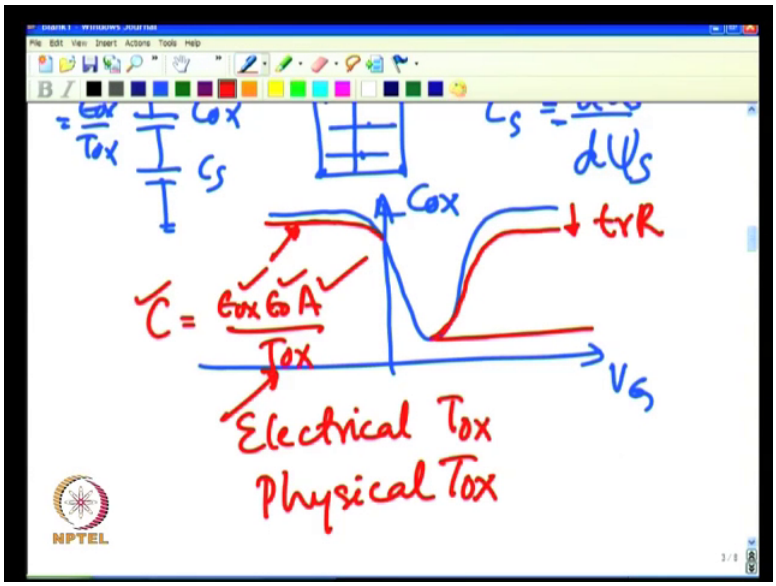

That is if you are doing a C V measurement on a transistor right this is very important in the context of MOS transistor, you are high frequency or low frequency both remember I said will give you a curve which looks like this, where in this maximum capacitance is Cox. Now in presence of channel quantization charge quantization your maximum capacitance in inversion will be degraded like this it will be less than Cox ok.

It will be less than Cox because Cox in series with C silicon is not infinity. Now it is finite capacitance and that will degrade the series combination and effective capacitance will go down. So, this is a very important manifestation that happens in most of the devices today, it could also happen in accumulation to some extent, but in accumulation the band bending is not as much as it would happen in inversion. And you know the effect in accumulation is not as severe as 1 would see in inversion, maybe in accumulation there is a very small effect may not be as big an effect as you would see in inversion. So, this is the CV curve in a transistor, anyway if you are doing a CV curve on a capacitor you know capacitor will anyway show up of like this.

But inversion capacitance will anyway be not at Cox, it will be much lower governed by the depletion bit maximum deletion bit, but accumulation capacitance may have some impact it may sort of degrade a little bit. So, this is 1 other important consideration that 1 has to people also modeled as effectively as if saying you know, your effective oxide thickness has increased and hence your capacitance will degrade and that is why when

we do the oxide thickness extraction using CV characteristic, we call this oxide thickness as an electrical oxide thickness not a physical oxide thickness your electrical oxide thickness extracted from CV curve may not be exactly equal to your physical oxide thickness and this could be 1 of the reason, why your electrical oxide thickness will be little different from physical oxide thickness.

What I mean by electrical oxide thickness is that I take this capacitance value and I say look this capacitance or accumulation capacitance is epsilon ox epsilon naught a by Tox and I know what is my a I know what is my epsilon ox and epsilon naught I have measured my C and I will calculate my Cox, this kind of oxide thickness calculation is what is called electrical Tox as opposed to physical Tox, invariably in today devices electrical oxide thickens could be anywhere from about 4 to 6 angstrom more than physical oxide thickness and 1 reason is this and the other reason what we call a poly silicon depletion effect ok.

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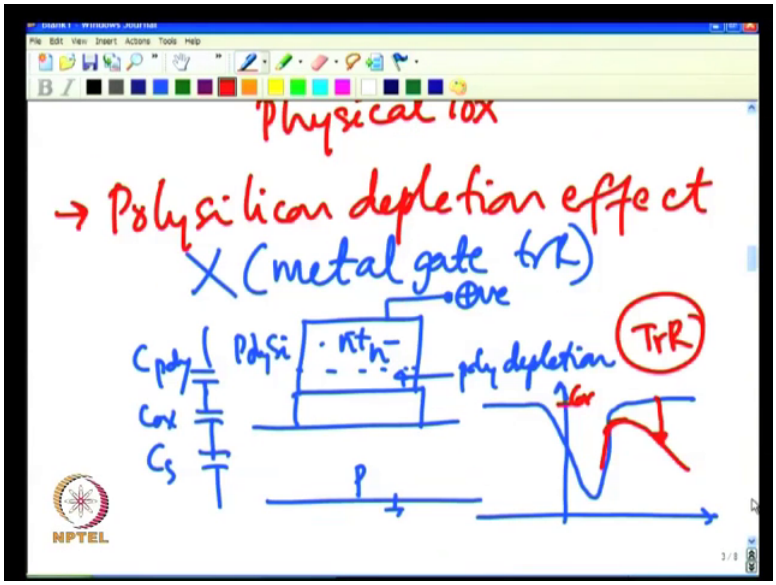

So, that is 1 other non ideality but this effect does not exist. If you have a metal gate capacitor or a metal gate transistor metal gate transistor this will not be there, this will be there only if your gate is poly silicon you know 45 nanometer and beyond mostly we are using metal gate transistor, that you know this is a mute point in that case and the only thing that you worry about is channel charge quantization which may affect your equivalent electrical oxide thickness because you have ultra thin oxides. Poly silicon

depletion is the case you know just for completeness let us also look at what it is, you know you have p silicon and this oxide and this is poly silicon is supposed to be doped with if it is a n MOS kind of a transistor, this will all be supposed to be n plus heavily doped n plus, but let us say for some reason.

It is not very heavily doped if it is not very heavily doped it is more like n minus, if it is like n minus and let say I have applied positive voltage what will happen, if I apply positive voltage it is as if I am applying a reverse biased to this pn junction, this is at ground potential and this is a positive and that will create a depletion region here correct like a reverse bias p n junction, you have a depletion width you know as you increase reverse bias your depletion width starts increasing.

And because of that this poly depletion under positive voltage not under negative voltage under positive voltage it adds a new capacitance in series, earlier my model was only oxide capacitance in series with silicon capacitance, but now I have what is called as C poly capacitance ideally that poly was supposed to be a metal like you know electrode, but it is no longer because it will contribute add a capacitance here. And hence again the total capacitance will degrade because of that because as soon as you start putting capacitance is in series your total capacitance starts coming down.

So, even under poly silicon depletion what you will see is again let us just look at a transistor structure, this is accumulation in inversion ideally you should have had something like this correct, but as I start applying positive voltage higher and higher positive voltage more and more depletion effect. So very interestingly your curve starts looking like this it will never reach C ox it will start degrading and I when I start again this measurement is done on a transistor not on a capacitor, if it is done on a capacitor anyway the minimum capacitance in inversion is C minimum, You know that we will not worry about it right now.

But in a transistor structure the capacitance in inversion should have been oxide capacitance correct, but no longer the case because when I start putting positive here there is a poly depletion, this depletion effect increases larger the depletion lower the capacitance and hence the series capacitance starts degrading, because this capacitance is pulling everything down. So, this is also not desirable. In fact, one of the reason why we moved away from poly silicon gate to metal gate was precisely this.

I told you a couple of reason 1 is the resistivity, when I have this long finger poly finger you know that contributes Rc delay and hence I wanted to sort of that resistance is also because you are not able to dope it very well. In addition to that you also have this kind of a poly depletion and you are on current of the transistor will suffer very dramatically because of that because remember your on current of a transistor is directly proportional to your oxide capacitance in inversion for a transistor. If your oxide capacitance in inversion degrades like this in poly depletion or degrades like this in channel quantization that will degrade your on current of a transistor and that is why we say your threshold voltage has now increased because you are on current has decreased accordingly.

So, this is one very important non ideality that you know we want to keep in mind and again as I said in a metal gate transistor you know this is not an issue right. So, the 1 last you know a non ideality that I want to talk about is during the measurement, this is all related to the device structure, but during the measurement you may have what is called a series resistance effect or a parallel resistance or parallel conductance effect ok.

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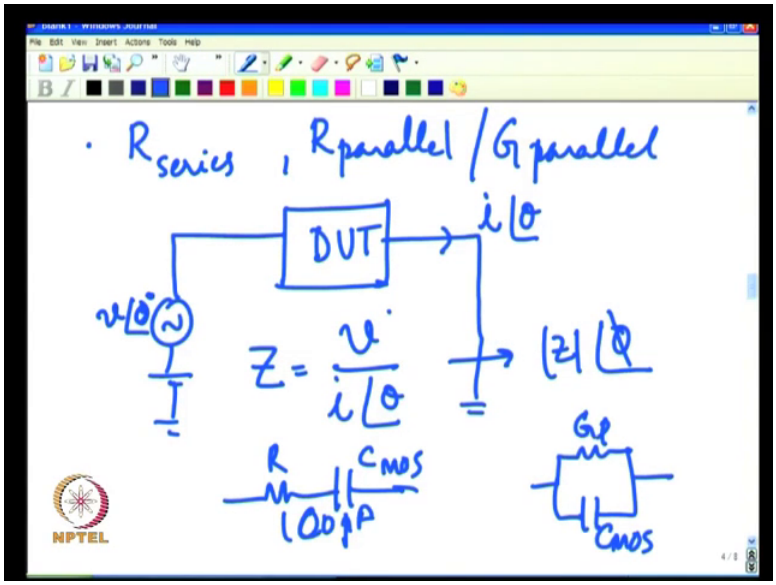

And sometimes we you know rather than calling it r parallel, we call it g parallel. Now what is it how do you do the CV measurement let us just take high frequency CV measurement right, it is very simple as I have mentioned anyway you have a dc bias let us not worry about dc bias right now. I apply some ac voltage which has some magnitude

and an angle theta let say this is my reference and I make this theta as 0 degree I am just representing it in a phasor form and I have my device under test which we call DUT and what you do is measure this current and it is angle right theta it is a phasor right, all you are doing is that you have this device under test you are applying some input excitation you are looking at what current is coming out. And then you say look my Z is essentially V divided by I theta correct and all that equipment is doing is measuring this current phasor that is coming out and at output and it knows what voltage phasor it has applied and taking the impedance as v divided by I theta.

This is the impedance that you get which is essentially mod z and angle five. Let us say it has certain angle and it has certain magnitude now if it is an ideal capacitance no issue right, you know because the angle will be ninety degree and you know whatever magnitude you have you know it is capacitance, you know it is 1 over j omega C is it is impendence right, you know the magnitude and you equipment has some routines it will spit out a capacitance value for you. But as a user you need to tell the equipment whether the device under test.

Looks like a series RC combination because of non idealities this is your MOS capacitor that you are trying to measure device that you have built or it looks like you know G parallel and see whatever MOS capacitance that you have that you have built, meaning that it has to resolve this z into either this form or into this form z is same, but when it is resolved into this form you get a different number for resistance and different number for capacitance. When you take the same z and resolve into this you get a different value of resistance and different value of capacitance. As I said if there was no non ideality then you get 0 resistances here and the exact same value of capacitance the capacitance here if it is.

Let us say 100 Pico farad, if you get 0 resistances if you resolve it like this you get infinite conductance here, it is like an open circuit this branch is open if it is an ideal capacitance and you get the same hundred Pico farad here right. This is only if there are no other external non idealities external or internal now you see when you are doing this, there may be a series resistance because you have not probed it properly if you are not very careful, there could be this cable that you are connecting two equipment and that may also have some resistance.

And you know the metal that you have used may not be very good that may also contribute some series resistance. All these are sources of series resistance. What are the sources of parallel conductance; if you have ultrathin gate oxide then the gate oxide will also leak because of the direct tunneling current that we talked about.

If you have a thick gate oxide there is absolutely no conduct no leakage through that, but if you have an ultra thin gate oxide as I said let us say 1 nanometer gate oxide. And you have built this MOS capacitor, there is always a leakage here this is a dc path correct and this essentially showing that dc path.

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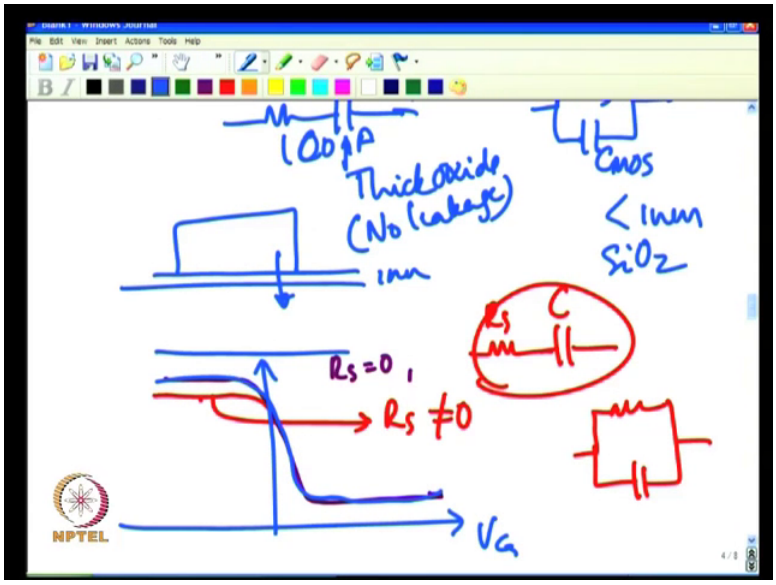

So, as a user for example, if you have made sure that there are no series resistance invariably the rule of thumb is that, if you are dealing with the MOS capacitor which has reasonably thick insulator. Which means let us say 10 20 nanometer and you have actually verified by doing an iv measurement, that there are absolutely no leakage. Then you never use this model because there is no leakage path anyway, there is no leakage path meaning this model is true.

So, at no point in time it allows dc leakage current here whereas, this model allows you a dc leakage current to be modeled correct. That is what we are saying the device under test has to be modeled properly. So, thick oxide use a series model always because no leakage and you verify you can always verify you can do a very simple iv measurement on this MOS structure and make sure that there is no leakage current or even if there is a

current let say Pico ampere or 10 Pico ampere you have a terahertz, I mean tera ohms kind of a you know resistance which has almost like an open circuit.

So, you do not worry about this, but there could be some series resistance you model it like that then you get the right value. On the other hand, if you are dealing with let say less than 1 nanometer kind of Si O 2 or an high k dielectric which is very crappy, you are developing high k process ideally high k process if you have a 5 to 10 nanometer it should have 0 direct leakage current, but for some reason you know you really have large leakage which you can always verify by doing a simple dc iv measurement.

Then you better use this model, because there is always a dc conduction path and what it means is that the current that you are measuring has a dc component also, you tell the equipment that this is a more realistic model to use not this model right. If you do not follow this then you will actually get an incorrect result for your capacitance. In fact, you know I will leave this as an exercise you can actually do it yourself that if you were to do this kind of an equivalence you see that when r is not 0 and this is not infinity your capacitances in these 2 cases will not be equal right.

For the same z you will get 2 different capacitance value and that is when you have to decide what is the value to choose and that depends on what additional information that you have on your device, and you need to be careful about you know that non ideality. And more specifically you know if I may sort of elaborate it very quickly, if you have let us say series resistance only. Let us say this is my ideal C V curve hf C V curve which I should have got right when your R s is equal to 0 and accordingly you r parallel is infinity. But if R s is non zero then if you are doing the C V measurement, what will happen is that in the low capacitance value range the effect will be not as great, but when the capacitance is very large you know you will actually see a degradation of the capacitance.

That is if in reality now this is R s non zero, but you have told the equipment that R s non 0 meaning this is how the model should have been this is your ideal actual capacitance that you wanted to get, but by mistake you have told the equipment that use this model that either is effectively it looks like this and there is a parallel resistance and my d u T is low this extract this value from z if we extract this value your capacitance will be less

than what it should have been, but if you use the right model then you know you will get back the same capacitance right.

In fact, when you do the measurement right of course if R s is 0 then the ideal then there is no issue, but non 0 R s or conductance whenever you ask the equipment to do a series model and parallel model, you see that the 2 C V s we will be entirely different right and you make sure that you do the right model representation for the device and you get the right capacitance right. So, that is important message that I wanted to convey.

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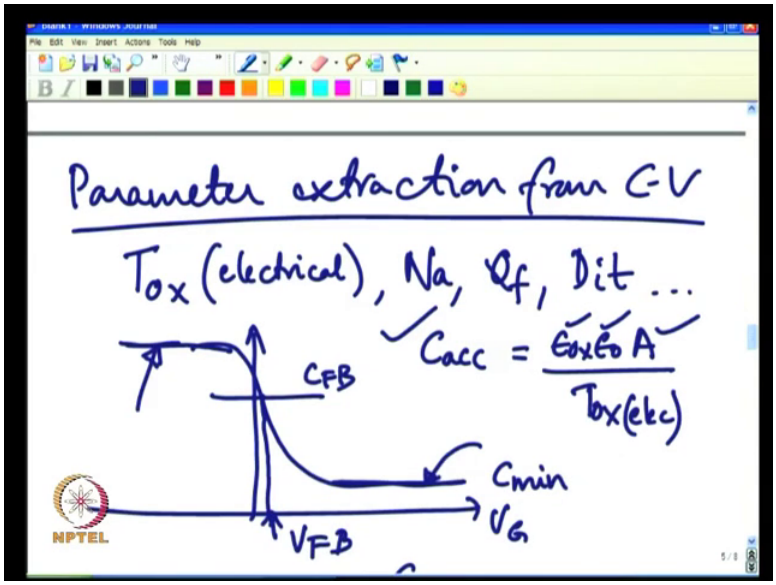

So, let us look at now this issue of you know parameter extraction, extraction from C V what I mean by parameter extraction is I want to extract what is my oxide thickens, I let me call it electrical oxide thickness, what is my substrate doping, what is my fixed oxide charge what is my D it and so on and so forth right.

These are the most important parameters that you want to. A very simple thing that you do is that you make a MOS capacitor, you do a high frequency C V and you should make sure that you get a true high frequency C V, the frequency should be reasonably large. So, that you know you get a capacitance which looks like this and make sure that I mean if there is hysteresis of course, that is due to interface traps you know that hysteresis will only tell you how much is a slow interface traps now fine.

So, what you do first is that you look at this value accumulation capacitance and you say that this accumulation capacitance is essentially due to oxide capacitance. And you say that you know this is epsilon naught you know the area of the capacitance that you have built and T ox electrical T ox electrical extracted in accumulation region right. So, you know this you know this. And hence you could extract your oxide thickness. Once you have the oxide thickens right then you can go back to this minimum capacitance C minimum, remember that C minimum is essentially determined by the doping concentration.

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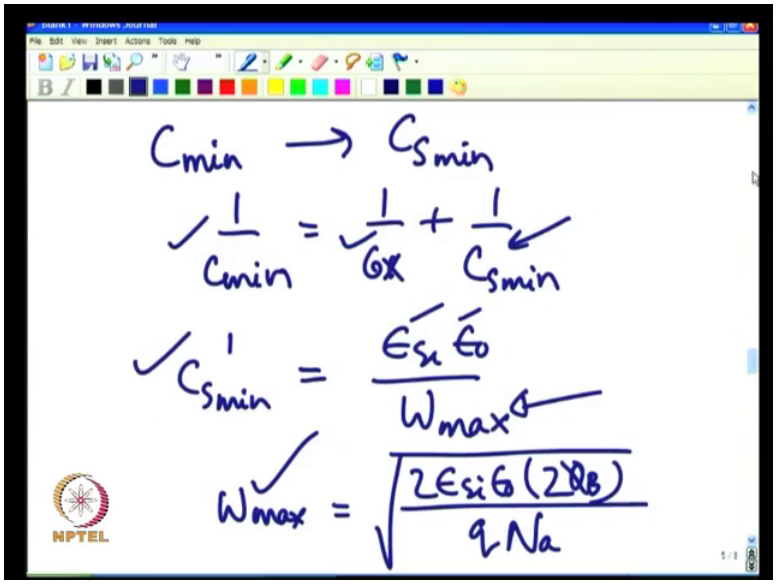

It is has a strong influence I mean doping concentration has a strong influence on minimum capacitance right. So, first of all what you have to do is that from this measured C minimum you need to get what is the silicon C minimum, because this measured C minimum is really silicon C minimum in series with oxide capacitance you see. In other words whenever doing the measurement, what you measure is really always oxide capacitance in series with silicon capacitance correct.

So, you need to first get the silicon capacitance from this, you know this already you know this already because this is oxide capacitance you can always get the minimum silicon capacitance. Now you also know the area once you get minimum silicon capacitance you remember always we deal with per unit area capacitances when we do calculations right. So, you know divide it by area and you get the per unit area

capacitance right which let me call C s min prime which is essentially this divided by area, and that is essentially epsilon silicon epsilon naught divided by w max, where w max is a maximum depletion width correct.

Now, you know this and this is known anyway and you can extract what is maximum depletion width. Once you know the maximum depletion width you can find out doping concentration value, because as you may recall the maximum depletion width essentially is given by right.

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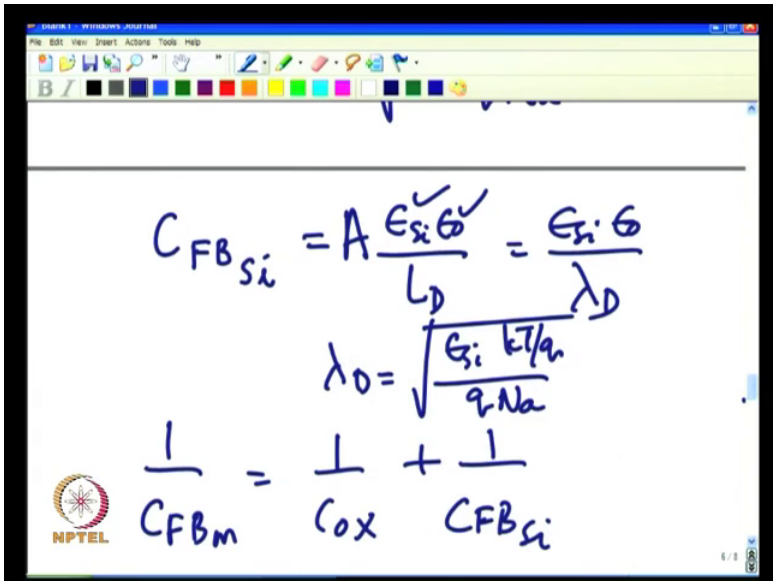

When you reach a band bending of 2 phi B that is when I reach inversion correct divided by q N a where N a is the doping concentration that I want to find out; however, phi B is also dependent on doping concentration because phi B is k T over q l n a over n i, but you can solve this equation iteratively and because you know this you can extract N a value right. And hence, you find out what is N a value and this we are doing assuming that the doping concentration is uniform. If it is not uniform doping concentration then also there is a way to extract doping concentration as a function of depth by looking at the C V characteristics right. So, you know the textbox will.

Certainly discuss that you know this is little more involved, but one can easily do that. But for most of the calculation a uniform doping concentration is a reasonably good estimate right especially when one is doing process development anyway, one starts with a you know standard silicon wafer which has anyway uniform doping concentration you

do not do any implantation or diffusion which will alter the doping concentration as a function of depth. So, uniform doping concentration is a reasonably good a estimate, as soon as you get this doping concentration I can extract what is flat band capacitance. First of all flat band capacitance in silicon, because flat band capacitance in silicon as you know is epsilon silicon, epsilon naught by debye length lambda L D or sometime this is also referred to as lambda D debye length. And remember I told you what debye length is in the last lecture that is essentially related to your doping concentration.

So, once you know N a this is thermal voltage instead of band bending psi s, psi s is 0 anyway we have thermal voltage here and N a is what is already evaluated and I can find out this and everything else is known anyway you multiply this with area, you get flat band capacitance of silicon. Then you can ask the question if this is the flat band capacitance of silicon, because it is coming in series with oxide capacitance what would be the measured flat band capacitance and that is simply C F B measured is 1 over I mean C ox in series with silicon flat band capacitance correct.

And that will give you what is the flat band capacitance that would be measured flat band capacitance. What it means is that in this C V curve now I am locating a very unique point which is a flat band capacitance point. And this in this point on the C V curve gives you flat band voltage and that is how you obtain a flat band voltage.

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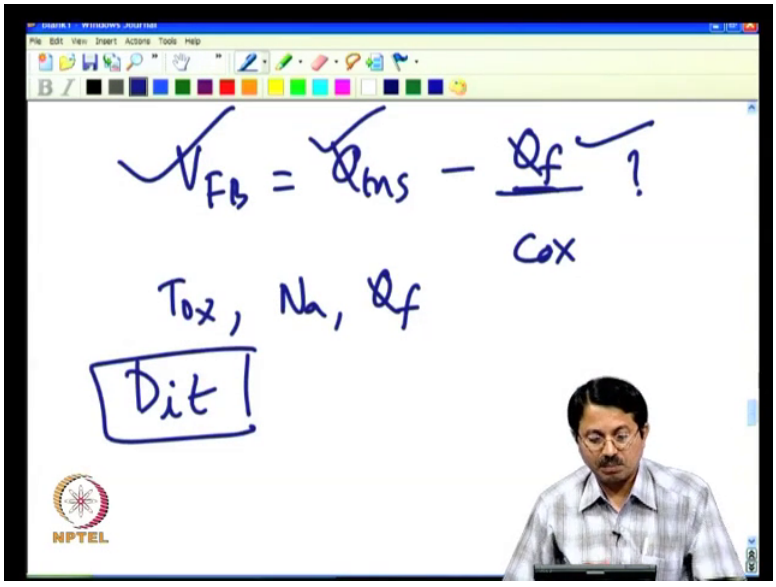

Once you know the flat band voltage you know the flat band voltage as you know is phi m s minus Qf by C ox correct. Phi m s presumably you know because you know phi s because you have obtained doping concentration in silicon is easy to find out phi s now phi m preassembly you know what metal you have put on the gate and you can take the metal work function as phi m phi m s is known V FB is known already from the graph and I can calculate what is Qf correct.

So, Qf can be easily computed using this. So, now, I have done T ox, I have done N a, I have done Qf the next important thing is to measure D it you know which is one of the most important thing especially if you want to get a very good quality MOS capacitor. So, how do we get this Dit? There are multiple ways 1 can get this Dit.

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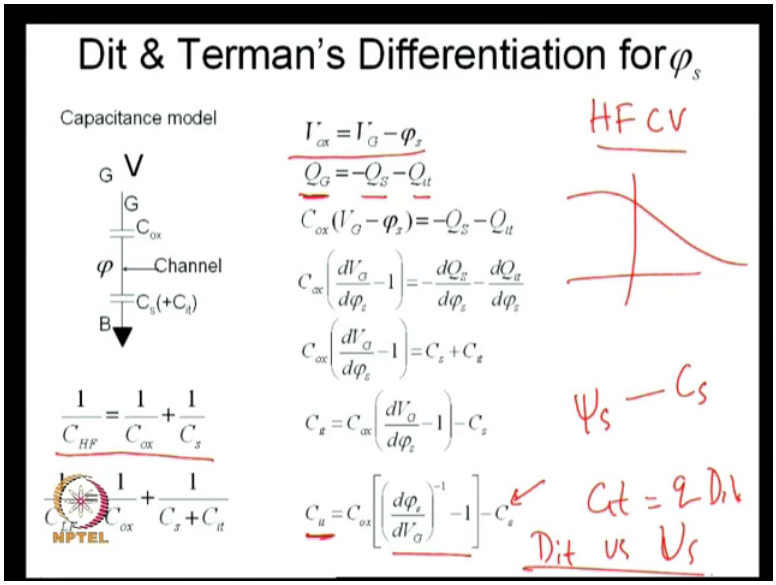

So, let us look at you know different ways of getting Dit, the first thing that you can do is that you can look at only high frequency C V, from high frequency C V you can get Dit you do not need to do low frequency C V. Remember our model that we have apply gate voltage.

On the gate terminal this is oxide capacitance this is my channel and that is the psi s surface potential this is the surface potential which is changing depending on the applied gate bias, and your silicon capacitance plus interface trap capacitance. At high frequency it is 1 over C ox plus 1 over C s because when I am doing a high frequency measurement Cit does not respond, although the stretch out is there the value of the capacitance will

not increase this is what we have discussed in the last lecture. On other and in the low frequency you know it is C s plus Cit which comes in series with C ox. So, in a high frequency C V measurement just looking at this I do not have the Dit information; however, remember the stretch out of the high frequency characteristic gives me Dit information. So, what I need to find out is.

What is that stretch out. So, how you do that? So, let us look at this right you know your oxide voltage can be written as V g minus psi s right and that is what it is VG V ox is equal to V g minus psi s psi s is the silicon potential. Now there are 2 elements in series total voltage is V g, subtract the silicon potential you get the oxide potential also Q g the charge that is put at any gate bias remember this stretch out that we are talking about at any gate bias when I go from one gate bias to the next gate bias, I give enough time and hence there is a stretch out. So, the gate charged that is what is now Qs and Qit combined. Qs is the silicon charge which is essentially coming due to the impurities enhanced impurities and electrons and Qit is the interface strap charge and now I hence I can write.

V ox is C ox times Q G is essentially C ox times V g minus phi s and this essentially is Qs and Qit and what I am doing here is that you differentiate this equation with respect to psi s and if you do that C ox dVG over d psi s minus 1, because d psi s by d psi s is 1 minus d Q psi s by d phi s and d Qit by d psi s and what is this? This is cs plus C i t. So, C ox is dVG by d phi s minus 1 equal to C s plus Cit. And hence C it is C ox times dVG over d psi s minus 1 minus C s. This we can rewrite it as because V g is an independent variable I am controlling V g from the external world and psi s is the dependent variable.

Psi s is responding to the change in gate voltage and hence I am rewriting dVG by d psi s as d psi s by dVG inverse right that is all I have done here it is the same thing rewritten here. So, Cit is C ox times this quantity and C s. Now you see I have a means to figure out Dit if I do high frequency measurement, from high frequency measurement at every psi s each psi s uniquely define C s.

Remember that because psi s is the band bending as soon as the fix the band bending there is a particular value of C s that is it, because that band bending will fix Qs in silicon and that Qs will correspond to certain C s value. So, at any psi s, I know C s and if I i

have already computed C ox because C ox is measured anyway that is known to me if you can find out what is d psi s by the d V g.

At every value of psi s then I can put that value here and C s value here and get Cit if I get Cit remember Cit is q Dit and hence I get Dit value at that psi s, and hence I can generate Dit versus psi s plot at different band bending I can get Dit. In other words I am getting interface traps in the band gap very nicely. So, how do you do that from the measured information? So, what you do is the following right I need to get this how do you get this and to get this.

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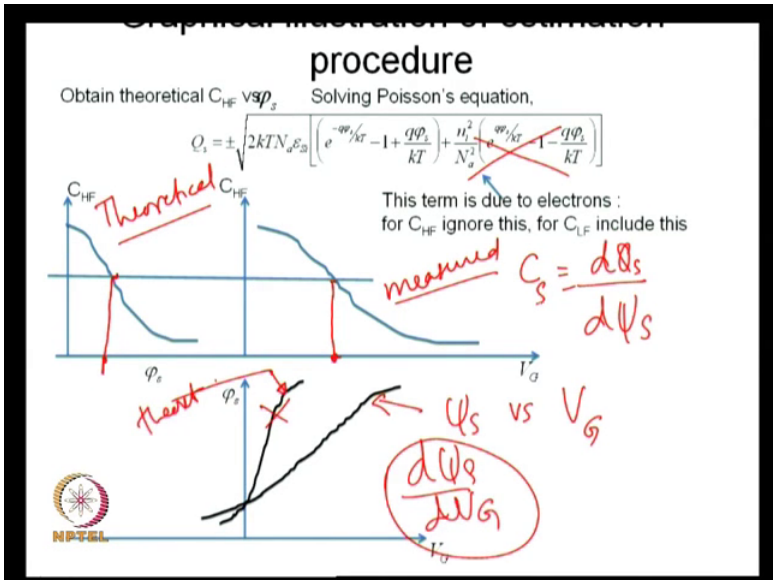

We essentially first we note that as I mentioned for any band bending psi s, I can estimate what should be C s because there is a very unique mapping between psi s and C s.

And that is essentially based on solution of poisons equation if you solved poisons equation you get Qs which is semiconductor charge as plus minus plus minus indicating that when it is in accumulation it is positive charge, when it is in depletion and inversion it is negative charge. Accordingly psi s is positive or negative in accumulation it is negative in inversion it is positive. So, this expression here this corresponds to all your charge corresponding to whole charge, this you know whole charge and also the depletion charge and this expression corresponds to your minority carrier charge which is electron charge.

I have already found out N a you see, and I know you know all other constants epsilon silicon everything now for different values of psi s, I can generate Qs right I have given a doping concentration I have a very unique relation between Qs and psi s. Once you know the Qs and psi s you can very easily get capacitance because capacitance remember is d Q psi s is silicon capacitance by d psi s.

So, all you need to do is that you generate psi s versus Qs which is here and you differentiate this you know you can write a very simple program to do that, it could be even a excel program to do that you put in several psi s value generate Qs you do dQs by d psi s and you have a capacitance. Except if you want to get high frequency capacitance you ignore this term, because this term is due to minority carriers. We say that under high frequency minority carriers do not respond and hence I ignore this term I only retain this term and I generate C HF versus psi s.

In other words for different values of psi s, psi s is going from 0 which flat band going towards 2 phi B which is going towards inversion, I generate all the values of capacitances. So, this is theoretical right from theory I have been able to generate this, but this value of capacitance uniquely corresponds you know this is my measured C HF versus V g I have measured it, but this psi s uniquely corresponds the same band bending because only when you have that band bending you will get this capacitance because it is C ox in series with C silicon and hence for every capacitance value you have a unique value of psi s and this unique value of psi s maps to a unique value of V g, this is your measured curve.

So, for every value of psi s again you know you can either do it graphically, but you do not want to do it manually again a very simple program can be written to do that, every value of psi s will have a unique value of V g. And in other words what you have generated is really psi s versus V g, this psi s versus VG would be theoretical. I do not really need to worry about theoretical psi s versus VG and I can also generate psi s versus V g theoretically forget about this curve. All I am trying to tell you is that by comparing this with the measured C V, I have this psi s versus V G curve and because I have psi s versus V G curve, I can get d psi s by dVG very easily at any value of psi s I put a value of psi s, I find out what is d psi s by dVG and I also find out what is C psi C s because it is very uniquely defined for that value of psi s, as soon as I know both these quantities I know C s I put that value here I know.

D psi s by dVG I put that value here I have any way measured oxide thickness oxide capacitance I know what is Cit once you know Cit you know Dit. In other words what you have generated for every value of psi s, you have generated Dit versus psi s plot and this Dit versus psi s plot gives you the interface trap density in the band gap of silicon and this is what is called the sometimes this was first proposed by a person called Thurman and in fact, it is also called Thurmans differentiation technique used this differentiation process of psi s versus VG d psi s versus dVG is used in estimating interface trap density.

So, this is one way of doing. So, just by having high frequency C V capacitance you can do this measurement, especially when your trap density is very large this measurement is fairly accurate, but if you are trap density is very very low like 10 power 10, then this kind of a differentiation process leads to some errors, then this process will not be very accurate. But for most of the process development when you are doing a new high k dielectric you know you are trap density is reasonably large. And you can very easily just do a C V measurement just high frequency C V and you can obtain the interface trap density as well using the C V measurement.

There are 2 other ways of doing see interface trap measurement which we will discuss in the next lecture, those 2 measurements will work only if you have a ideal I mean not ideal a good low frequency measurement done along with the high frequency measurement and that we will discuss in the next lecture. So, just to sort of rap up you know there are multiple non idealities in a C V system which we discussed ranging from fixed charge interface charge slow traps right. And we need to deal with these non idealities, and also there are ways to extract the various parameters from the C V measurements as we discussed today. So, you know now if you have both high frequency and low frequency measurement, you know then what 1 could do is that you know as I mentioned here, I will go to this equation remember this.

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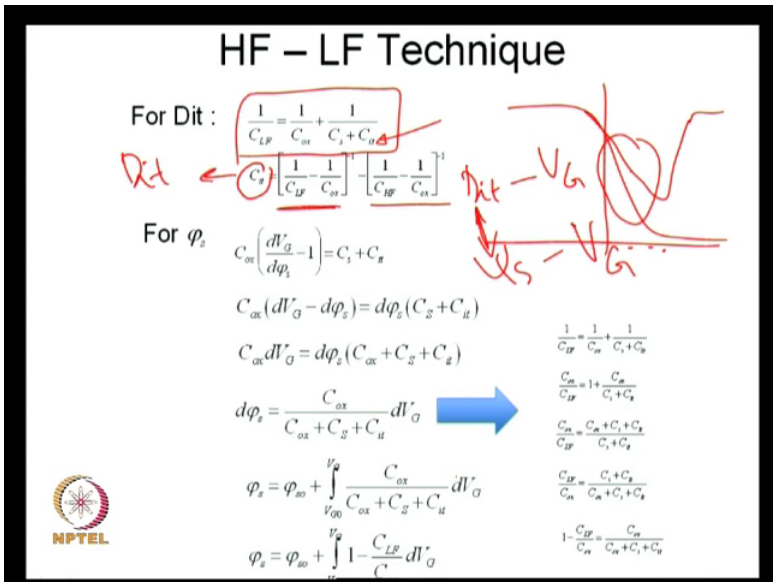

Then you know from this equation I should be able to get the interface trap density here. So, you know how does one that one do that right you know assuming that you have just the low frequency capacitance do not worry about this equation you know we will postpone the discussion on this equation for a minute, ok.

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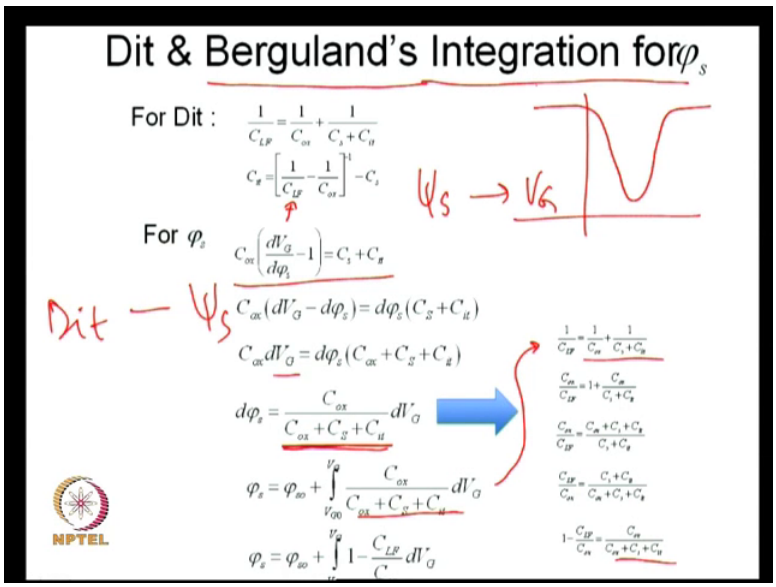

Maybe I was looking at the wrong slide maybe let us just focus on this right I have measured low frequency C V measurement. Remember that in the depletion region the low frequency capacitance region responded to interface states right. If you are high

frequency was lower your low frequency was higher it would be much higher, because the slow varying signal traps can easily respond to that and that is why I have this model C s plus Cit. And now Cit can be written as one over C LF minus 1 over C ox minus Cs you have measured this low frequency capacitance and all you need to do now is that at different psi s you need to find out C s and also need to find out a relationship between psi s and V g earlier we found that.

Psi s versus VG relationship through that differentiation technique, but here we will not do that differentiation we will actually use an integration technique of a low frequency curve as opposed to differentiation technique of psi s VG derived out of a high frequency curve now we are not looking at high frequency at all, we are only looking at a low frequency curve. So, what do we do right and this is a generic expression that we have C ox times dVG by d psi s minus 1 is C s plus Cit which is what we derived earlier when we were discussing the C V measurement. Now you know a one can sort of rewrite this equation a little bit you know just some algebraic manipulation right you know you sort of you know take this phi s on this side and you know you have d C ox dVG as d phi s times this and in other words d psi s is equal to C ox divided by this times dVG .

Now what I can do now is that this part right first of the all if I can express this part as a measured low frequency capacitance and then I can integrate this whole thing phi s psi s would be psi s 0 plus integration from VG naught to VG of C ox divided by C ox plus C s plus C it dVG right I mean I am just sort of integrating it for example, at VG naught is equal to V FB right your flat band voltage is 0 right. So, that is an initial condition for example, and you know from that you can actually go to different gate voltages and you do this integration and you can get different values of psi s as a function of VG what I am going to do now is that I am going to rewrite this right I based on you know this.

Capacitance equation 1 over C LF is 1 over C ox plus 1 over C s plus Cit, and I am multiplying this equation on both side by C ox again doing some algebraic manipulation here and I am simplifying that equation and what I get is C ox divided by C ox plus C s plus Cit is same as 1 minus C LF by C ox I have this is something interesting right C LF is what is measured externally C ox can always be obtained because it is you know looking at the accumulation value of capacitance you can find out what is C ox right in other words this term inside the integral can be replaced by 1 minus C LF measured divided by C ox . So, now, all you need to do is that put different values of psi s at these

different values of psi s you precisely know you know what is the value of V g and accordingly you also know what is the value of Cit.

So, at different values of V g you know what is the value of a LF capacitance that you have measured and hence you would be able to find out Dit as a function of psi s again you are mapping Dit to psi s, 2 major differences 1 first difference is that the way I computed Dit is from low frequency capacitance and this is what I used to compute Dit that is one major difference compared to previous technique. In previous technique only high frequency was used. The second difference also is that to compute psi s versus V g relationship earlier I did it using high frequency curve, but now I am doing it with the low frequency curve. So, both these thing are done using a low frequency capacitance voltage characteristic right.

That is the major departure here and hence you know again this was first postulated by Berguland and this is use using an integration process to compute psi s versus VG relationship and hence the name Dit computation using a Bergulands integration to get that psi s versus VG relationship. One last technique if you have both high and low frequency at your disposal then what you can do is that you can use what is called a h f l f technique right meaning that I have measured high frequency capacitance which looks like this, I have measured a low frequency capacitance which looks like this in this region which is where your band bending is going from flat band to inversion that is the region of interest for us from 0 to 2 5 b.

Psi s is going from 0 to 2 5 b, in this region your low frequency capacitance is higher compared to high frequency capacitance. You can look at this difference and you can get Cit as you know something like this you make use of low frequency capacitance and this C s that I had in the previous equation that can be computed using high frequency capacitance 1 over C HF minus 1 over C ox inverse. So, the Cit or in other words Dit is now computed based on 2 actually measured values, low frequency value and high frequency value right and this is how I get Dit as a function of VG at different values of VG I get Dit, but I really need to map it to different values of surface potential.

And in order to get that you still needs psi s versus Vg. So, that you can if you get psi s versus V g then because you know this, you can map this Dit versus C s and for that you know you can essentially use the same Bergulands integration that we talked about

earlier right you can use that and you would be able to get psi s versus V g relationship from the low frequency curve. You do it from the low frequency rather than high frequency because the integration process will not give rise to too much of noise whenever you trying to do differentiation from the measured curve, you can end up with large noise in the differentiation process and this is what is called a h f l f technique right.

So, one can extract this interface trap density either solely by high frequency curve or solely by low frequency curve or a combined high and low frequency curve right. So, depending on what you have at your disposal you can do 1 or all of this. And this also happens to be one very important you know a parameter extraction process.

So, then let us stop here. That sort of completes all the discussion on MOS capacitance characterization. And in the next lecture we will you know discuss about current voltage characterization on a transistor.