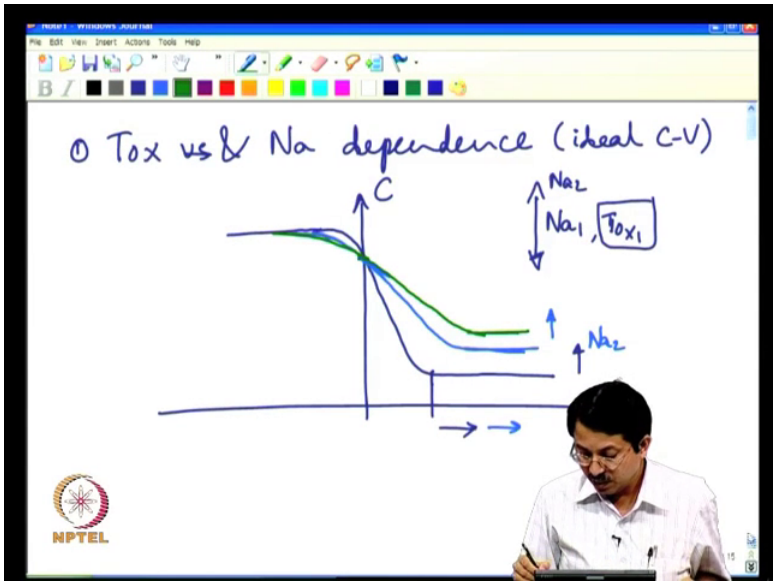
Nanoelectronics: Devices and Materials
Prof. Navakanta Bhat
Centre for Nano Science and Engineering
Indian Institute of Science, Bangalore

Lecture - 13
Effect of Non idealities on C-V

So, today we will look at several non idealities in capacitance voltage characteristics, but before we do that I just wanted to discuss two important points based on the ideal C-V characterization that we discussed in the last lecture. The first one is just to sort of understand how does C-V curve depend on oxide thickness and substrate doping. We already looked at various other factors such as measurement frequency dependence, temperature dependence and light dependence during the measurement and so on and so forth. All these are external characteristics but the device itself can have different oxide thicknesses and different doping concentration.

So, let us just look at the T ox versus I am sorry T ox and N a dependence of ideal C-V and we are still discussing on ideal C-V.

(Refer Slide Time: 01:11)



So, let us just consider high frequency capacitance. It would be similar for low frequency as well and you know, as you recall from our last discussion, if you look at C versus v g for a p type substrate capacitor you know it would look something like this. It has a flat band voltage which is 0 and the capacitance voltage curve will essentially look like this

and this is where you reach a strong inversion and after that you have a flat characteristics. Let us say this is the case for a particular doping concentration of N a 1 and a particular oxide thickness of T ox 1.

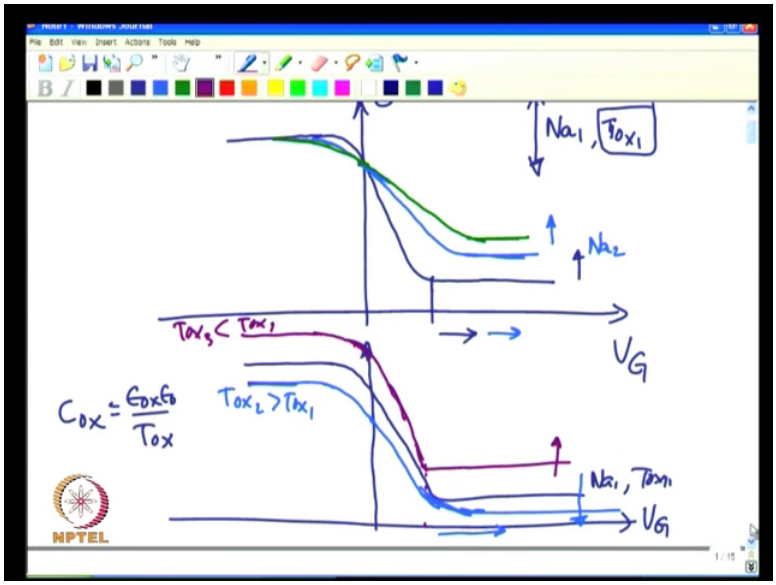
First, let us consider a situation where T ox 1 is kept constant, this is not well changed, but this N a 1 is varied, then let us ask the question you know what would happen to the C-V characteristics. Again, let us for the time being consideration ideal capacitance. Somehow, I made this capacitor so that v f b is 0. So, the v f b point essentially is out here for all these cases. Now, if you let us say increase the substrate doping, what you would expect because of that is your threshold voltage should increase. As we have discussed in very early lectures of this course, threshold voltage has a very strong dependence on substrate doping concentration. If your threshold voltage corresponding to N a 1 is out here.

Your threshold voltage corresponding to let us say N a 2 which is higher than N a 1, will certainly move to the right because it will have a higher threshold voltage. Right, that is one aspect. In addition to that the other thing that would happen as you can well imagine, when you, you know reach inversion right, the inversion capacitance eventually the minimum so called minimum capacitance that we are talking about, you see depends on what is your maximum depletion width and of course, that maximum depletion width will set them in minimum semiconductor capacitance that will come in series with the oxide capacitance. And you know eventually, you get the equivalent series combination of these two capacitance, but the deciding factor is really the depletion width maximum depletion width. As you could now well imagine, as you also increase a substrate doping concentration due to the fact that the depletion width has an inverse square root relation with substrate doping concentration.

The depletion width will decrease and hence you would expect the capacitance to increase. So, what it means is that the minimum capacitance should also go up as you start increasing N a 1 right. So, as a result of that you know your curve may look something like this. If we say that this is a pig out point here, the maximum capacitance will not change necessarily because maximum capacitance is essentially governed by the oxide thickness. We are saying that we are keeping oxide thickness constant, we are not changing oxide thickness, but the v t will shift minimum capacitance will also shift. So, your C-V curve will probably look something like this. This is, N a is increasing, N a 2.

Now, if you increase N a further, you know this will increase further and this will also increase further threshold voltage will increase further right, and you know eventually you start seeing the curves which would probably look something like this right. So, notice that two things happen with varying N a v t increases and minimum capacitance also increases. Right, both happens sort of simultaneously.

(Refer Slide Time: 05:22)



Now if you were to consider the other situation wherein, you keep N a constant, right and let us sketch those characteristics as well. Let us again say that we start with some C-V characteristics for certain value of you know, N a 1 and T ox 1. Now, I start varying T ox. Let us say I start increasing T ox.

So now, let us see what happens if you increase T oxyou would expect because your C ox has relation epsilon ox, epsilon naught, over T ox right? Your oxide capacitance will start decreasing as you start increasing the oxide thickness and that will certainly have an impact on the maximum capacitance that we will have, because maximum capacitance is slowly governed by oxide capacitance and oxide capacitance starts varying as you vary T ox. Now let us ask the question, what will happened to the minimum capacitance. Substrate doping does not change, as a result of that, the maximum depletion width in inversion does not change in silicon and hence, the silicon minimum capacitance does not change. But what we measure externally is silicon minimum capacitance in series with oxide capacitance, because oxide capacitance is decreasing although silicon

minimum capacitance does not change the equivalent series capacitance will decrease right because C ox is also changing, right.

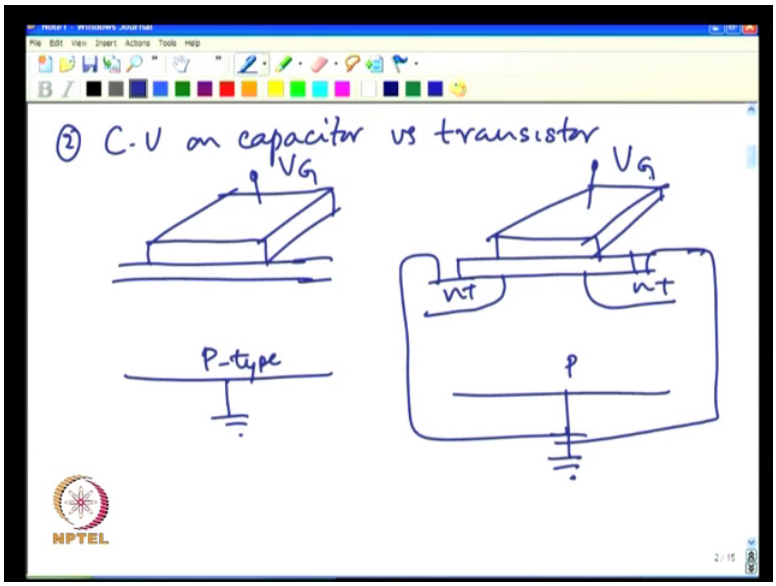
So, what you would then expect is that, if you start increasing the oxide thickness this; obviously, will come down. Let me just illustrate here and accordingly out here as well because all the N a is not changing silicon capacitance is not changing external oxide capacitance has decreased and as a result of that, your total capacitance will also go down. And, when you are started increasing your oxide thickness, your threshold voltage also increases.

So, what you might actually see is a curve which would look something like this, right. It starts moving in this direction and it starts moving down and the reason why it happened here is that, for threshold condition again as you remember, just as threshold voltage increases with increasing substrate doping concentration, threshold voltage also increases with the increasing oxide thickness.

So, this threshold minimum capacitance point shifted to the right and also the minimum capacitance value came down. On the other hand, let us say this is for T ox 2 which is greater than T ox 1. Now, if I choose another T ox which is less than this, then your min capacitance here will increase because now I have chosen T ox 3 which is less than T ox 1 you see, this will increase and because oxide thickness decreased, your v t will also decrease now and hence, it will probably look much more steeper and your minimum capacitance will increase now, because our your oxide capacitance which is coming outside in series with the silicon capacitance has gone up now.

So, your C-V may looks something like this. It will have a saturation at lower values of VG because your v t has come down. At the same time, your minimum capacitance increase because your oxide capacitance increase, right. So, you know your total capacitance sort of goes up and down because your oxide capacitance is changing. As a result, of that the capacitance in the entire C-V range will go up and down as oppose to this case, where only substrate doping was changing. So, these are some very important differences that you may want to keep in mind. In fact, in the next lecture, we will also discuss once you do a C-V measurement, how can you start extracting various parameters, but this is something that you know will be useful to remember when we have that discussion.

(Refer Slide Time: 09:47)

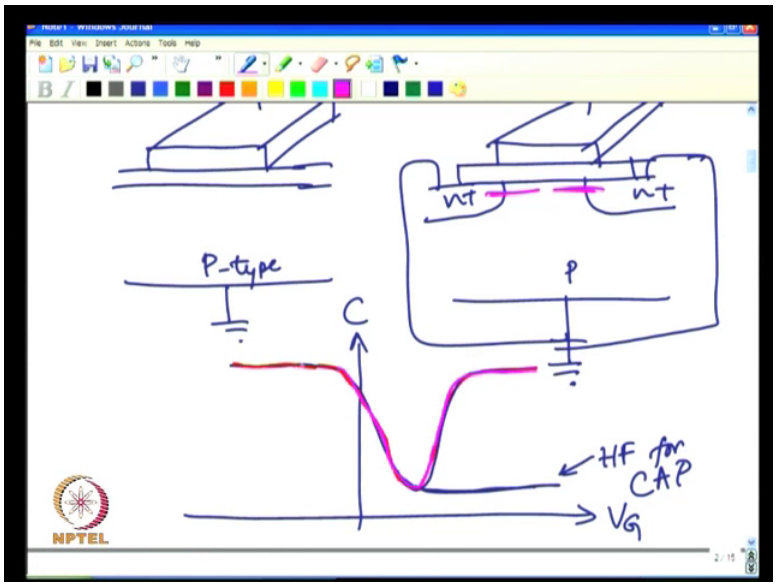


Now, one other point that I wanted to discuss a C-V on. You have been talking about MOS capacitor, but we also built transistors using these, right.

So, is there any difference in C-V of a capacitor device and a transistor device? In other words, the question that I am asking here is that, you have P type substrate let us say, you have oxide and you have essentially built an electrode here which is your gate. Now, this is essentially a 2 terminal capacitance device and you have another device where in, you know everything looks same. You know you have this similar gate area and all that, but in addition, you have also made junctions here, n plus n plus and there are contacts to the junctions as well and let us say, we have connected all these together. Whereas here, this is the low point and this is V G. So, both have the same area.

So, you would have expect the capacitances should be similar because the capacitance is essentially governed by what is happening here; however, there is one very important difference that you have to keep in mind and that is their behavior and high frequency characteristics.

(Refer Slide Time: 11:09)



Let us say this is C, the low frequency capacitance if you do l f C-V measurement on this structure as well as this structure, you know, you get a curve which will be exactly identical, right. Let us say if this is the curve for capacitor then your transistor curve will essentially overlap on top of each other. This is what you expect because anyway the area is same. So, your capacitor that is formed is you know is identical really, but your high frequency capacitance in a case of this device, as you know will essentially look like this right.

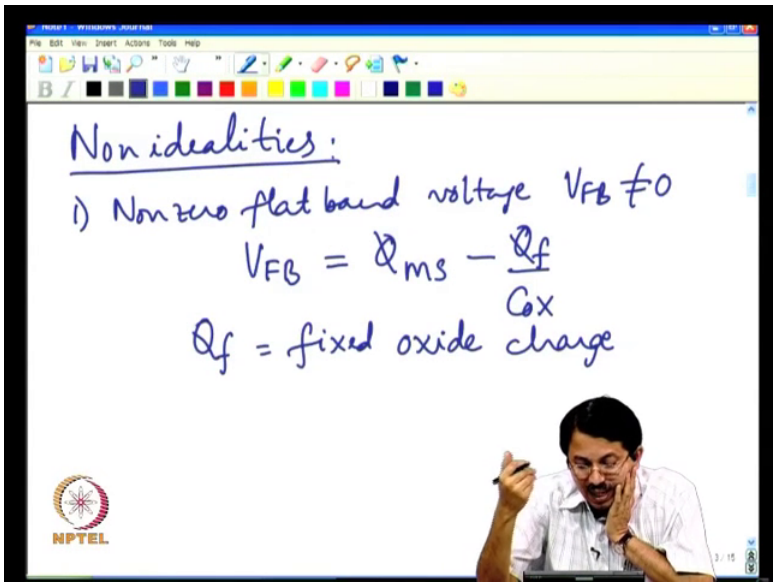
In inversion you have the minimum capacitance under high frequency. This is your H F C-V for capacitor structure. On the other hand, if you were to do this on a transistor, you see the transistor will give a capacitance voltage characteristic which will look exactly like a low frequency C-V. In other words, if you are doing this C-V measurement on a transistor structure with the connections as shown here, whether you do the C-V at high frequency, low frequency does not matter they always are identical, exactly identical and all look like a low frequency C-V. Only in a capacitor structure in inversion, your capacitance is quite different from the low frequency capacitance and if you think about this, this is obvious and it is no surprise at all, because as we discussed in the last class the very fact why we got a capacitance which is lower is because the electrons were not responding in a capacitance structure.

But you see now, you have given huge reservoir of electrons here, right this is a n plus, there lot of electrons which are available right next to that capacitor. So, you do not have to generate these electrons in a depletion region. So, these electrons will come back and forth instantaneously in this structure because of the fact that just as the majority carrier holes are available in this capacitance and hence, you do not see any difference in accumulation region.

Now, in inversion region also, although you do not have electrons as majority carriers here, but there are two junctions which are sitting right next to it which have electrons as majority carriers. So, you do not need to generate electrons anywhere else in this is device. These electrons can come back and forth instantaneously and hence there is no dearth of availability of electrons. Electrons respond instantaneously and hence, your semiconductor capacitance is very large it is no longer the depletion capacitance because you do not need the depletion edge to respond,

The inversion charge right here is responding instantaneously as opposed to the depletion edge responding, you see and hence, you do not see any difference here. This is another important point that you need. To that is why we make these junctions right. So, that you know, instantaneously we can turn on and turn off this transistor. Otherwise, you would not turn on the transistor at you know, Terahertz frequency, if you have to wait for these electrons to generate because of the generation that is happening, right because we have this source so called source junction, but here both are source junction because both are at ground potential, but in the transistor action, one of them is at positive potential that cannot source because you are draining the electrons there, but the source can instantaneously supply electrons into it, right and that is how we can fix the transistor at very high frequency.

(Refer Slide Time: 14:57)

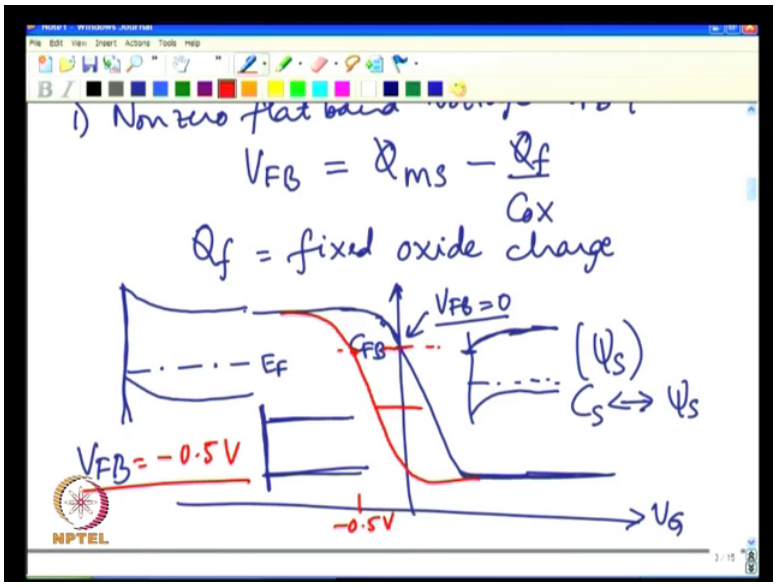


You know now let us look at.

First thing that we will look at is non zero flat band voltage. So, V FB not equal to 0. What are the contributors for V FB essentially as you may recall, V FB is the work function difference between the metal and silicon right because in ideal capacitance, we said I chosen a fictitious metal. Metal which has a same work function as silicon, but that will never be the case. Your capacitors made on p type silicon are likely to be for n channel transistor and they will have their work function on the gate side which is closer to the conduction band of the silicon.

It will be like n plus on the gate and hence, there is a Phi m s and in addition to that you can also have what is called fixed oxide charge Q f here refers to fixed oxide charge. Meaning, oxide is also not perfectly ideal. Ideal oxide will not have any charge inside it. But a non ideal oxide can have some non zero charge inside it and that would also impact your capacitance voltage curve, ok.

(Refer Slide Time: 16:36)



So, now let us look at the impact. So, let us say this is my ideal C-V curve, which has V FB is equal to 0. One important thing that you want to recognize here, the capacitance value at any gate voltage is uniquely determined by the surface potential in silicon.

In other words, when you have the accumulation condition if you recall, if I am looking that the p type substrate and if this is my oxide interface and this is my p type substrate what will happen. I have accumulation region which is, if this is E F bands are bent up like this you see, correct. That is, I have more holes here and that is what is called accumulation region and at this condition, I have flat band. What is flat band? You know if this is my oxide interface, again my bands are perfectly flat that is, Psi S is equal to 0 and as I am going in this direction now, I start seeing some depletion, ok.

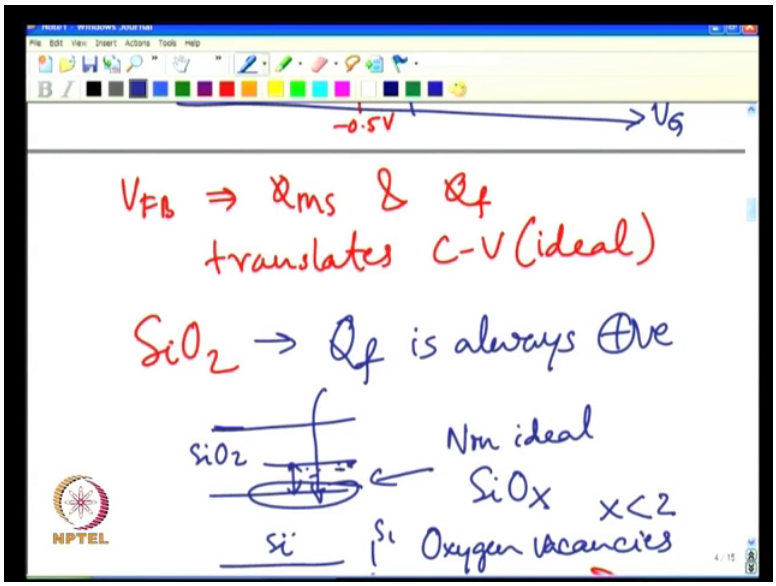
This bands will start bending like this right, again this is surface potential has changed. Surface potential 0, surface potential negative, surface potential positive, going down is what we treat as positive surface potential and eventually, when you reach inversion these bands have bent so much that you have band bending is 2 Phi b and you have reached inversion condition. In other words, the capacitance value is uniquely determined by Psi S, right. There is a very specific one to one correspondence between the silicon capacitance and this Psi S, the band bending. The value of Psi S, as long as, you have the same Psi S, you will get same capacitance, that is, the message. Because

you see, it is only the silicon capacitance that is variable oxide capacitance is not variable.

So, in other words now, when I have a non zero V FB, all that it would do is that, in order to get a flat band condition, under which, I should get this capacitance. By the way, this capacitance is called C FB. Once you fix your device, oxide thickness and doping concentration C FB will never change. So, if you have a different Phi m s non zero Phi m s, it will give non zero V FB and similarly, if you have a fixed charge, it will give non zero V FB, all it will do is that, it will translate this C-V curve along the gate voltage axis.

In other words, if my V FB let us say, is minus 0.5 Volt, what it means is that, in order to get C FB value, I need to go to minus 0.5 Volt. This is where you know I will get this capacitance value and after that, as I start applying more gate voltage you know it will go towards this and hence, capacitance will start increasing and I start applying a positive voltages beyond minus 0.5, band will start bending like this, capacitance will start decreasing like this. So, in other words what you will have is really this. So, there is this translation ok.

(Refer Slide Time: 20:24)



So, V FB due to Phi m s and Q f you know, translates C-V curve. Translates the ideal C-V curve that is, you know, whatever you got based on your ideal C-V characteristic, it just you know translates either to the left or to the right depending on whether your V FB

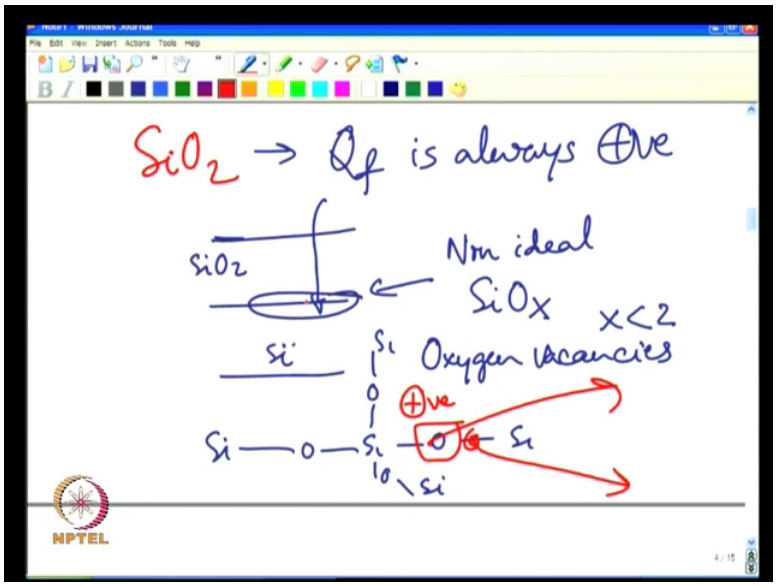
is negative or V FB is positive. In fact, as we will see in the next class. In fact, this is the information that we use to find out what is the fixed charge in the oxide when you actually measure a device because once you measure a device, I can generate a ideal C-V.

We will talk about it in the next class and then I can compare an ideal C-V with the experimentally measured C-V and looking at the difference I can generate all these non idealities in a capacitance voltage, I mean the MOS capacitor. Now this fixed by the way, Phi m s is very obvious, you have different work function. This fixed oxide charge is you know, essentially attributed in case of silicon oxide. At least Q f is always positive and essentially what is attributed is that, if you have this silicon oxide, you have to grow this silicon oxide on top of silicon. When you are growing the silicon oxide you are transitioning from silicon to maybe silicon oxide as I start growing thicker and thicker oxide.

But in this transition region, this transition region is really non ideal in other words, you really have something like S i O x. You see, when x is equal to 0 you have silicon. When x is equal to 2 you have S i O 2, but here you have really S i O x no its not perfect silicon not perfect silicon oxide something in between right. So, this is really non ideal thing. So, what it proposed really is that, you really have in this, this was supposed to be silicon oxide with an abrupt transition, but really in this region you have oxygen vacancy that is why your oxygen is no longer 2 it is less than 2, where your x is less than 2. X is less than 2 because you have oxygen vacancies.

Okay what I mean by that is that.

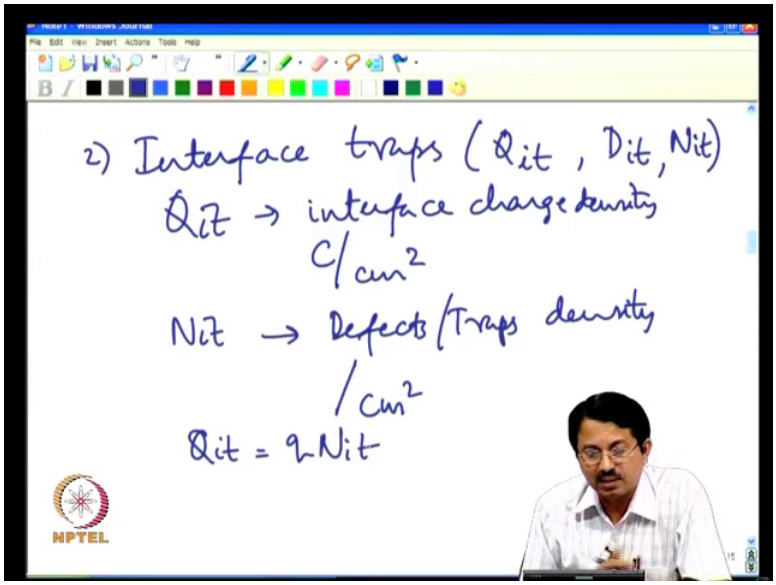
(Refer Slide Time: 23:06)



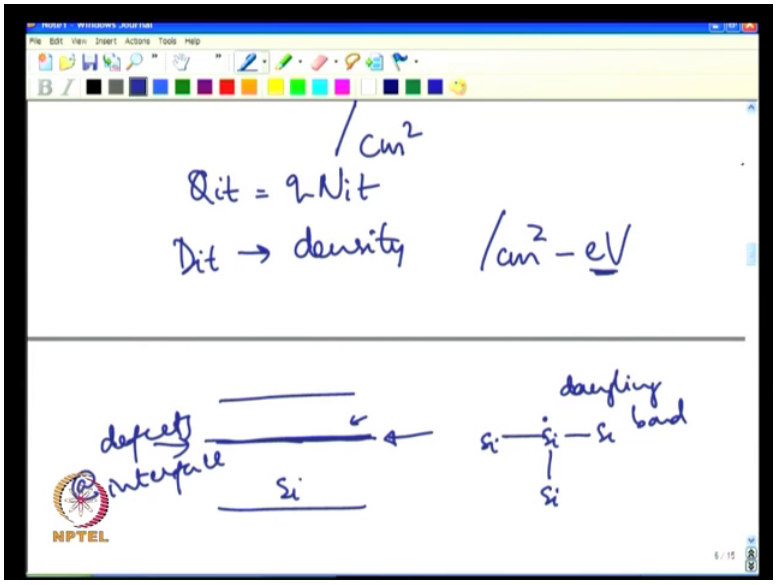
If you were to look at you know, the silicon oxide matrix, the silicon oxide matrix will essentially look like this ideally. You see silicon has valance of 4 and all that is satisfied oxygen has valance of 2 and that is also satisfied. But let us suppose that this oxygen is not there this is missing, then this is what is called a defect site and this defect site, ideally should have one electron from silicon and one electron from this silicon, but it tends to lose one of the electron right, because it cannot hold that electron there and hence, this defect size becomes positively charged. So, that is a very plausible very simple model that is given.

And in fact, this has also been you know validated by doing lot of structural characterization of silicon oxide right. So, invariably whenever you grow silicon oxide, on silicon, you have this transition region and this transition region has lot of oxygen deficiency and that oxygen deficiency results in a missing oxygen atom and a defect site which becomes positively charged right. So, invariably whenever you are doing a MOS capacitance characterization on S i O 2, you will invariably see that, you know because there is a positive charge this C-V will always tend to shift left. This is obvious right, if you have positive charge, you know your inversion voltage also decreases right and that is also obvious right. You have positive charge, this positive charge can attract electrons, right in other words, you need to inversion need reach inversion much earlier correct.

So, if you have a negative charge it will be the opposite. It will shift to the right. (Refer Slide Time: 25:10)



So, Q f is something very important that you need to consider right. So, this is essentially one of the non ideality. The next non ideality which is also very important is what is called interface traps. Itis denoted as Qit which stands for interface trapped charged or Dit or Nit there are different ways of. So, Qit essentially means interface charge. In other words, I am essentially saying Coulomb per centimeter square so much charge is available, Nit means defects or traps density. This is charge density that is why it is per centimeter square. Here it is number per centimeter square. So, many 10 power 12 traps per centimeter square. So, there is no charge here. You multiply Nit with q you get Qit. So, that is Qit is q times Nit. You are converting it into charge. (Refer Slide Time: 26:38)



And Dit is something is again a density, but its density trap density not just defined in terms of areal density, it is density in terms of area as well as per unit energy. It becomes clear in a minute what will mean by that.

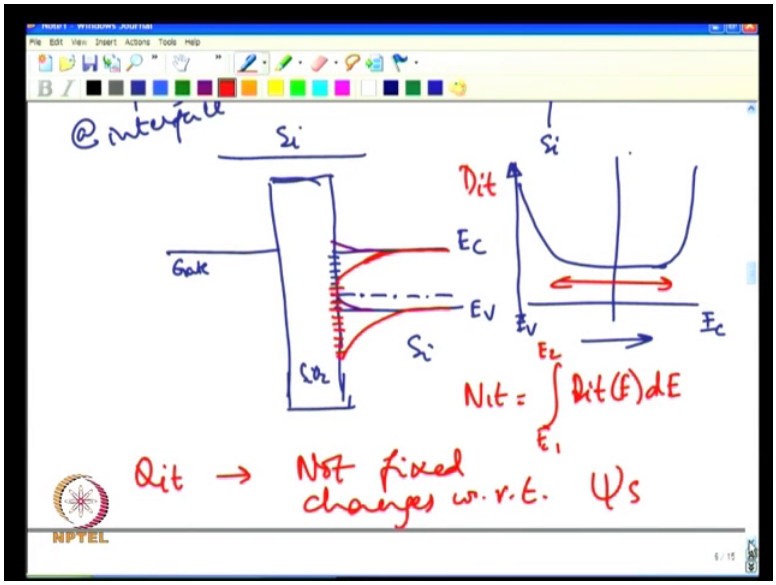
In other words, the unit of this is per centimeter square e V and this e V is essentially what I meant. It really tells you per unit value of energy in the band gap what is the density. So, first of all what are these interface traps, as the name suggest, when you have silicon and oxide exactly at this interface, the fixed oxide charge is little away from the interface whereas, interface trap charge that we are talking about is exactly at this location and hence, the name interface charge, going from silicon into silicon oxide exactly at this interface. Now again, if you see, at this interface you have lot of non idealities right, you have some silicon atoms which is sitting here.

Right the silicon was happily sitting here bonding with four neighboring atoms, but here you do not have a silicon here right. So, here you have what is called a silicon dangling bond right at the interface and similarly, you know you may have oxygen here and you know that oxygen bond length with silicon may not be perfect as it should have been in silicon oxide.

So, all these are defects again and these defects are exactly at interface and this is very important. And hence because they are exactly at interface their charge state changes. That is, the major distinction between the fixed charge that we discussed. Fixed charge is little bit away from the interface; not exactly at the interface right, this region which is a

transition region. This is where the fixed charge is and this being away from the interface it does not interact with the silicon underneath and its changed charge state does not change and hence the name fixed charge. Whereas, the interface charge, its charge state changes, it can either you know get an electron or release an electron, it can be positive charge, neutral or negative charge depending on the nature of the defect.

(Refer Slide Time: 29:32)



Now, these defects is what is going to impact your C-V characteristics and hence, the behavior of the MOS capacitor and transistor very significantly. Now this is in terms of position, let us look in terms of energetic. Now, this is my silicon which just consider flat band condition.

And this is my oxide right which has huge band gap as we have been discussing and you have some gate metal you know it could be anything. Some let us say n plus poly silicon now this is silicon and this is S i O 2 and this is gate. Silicon here is perfect band gap e G. there no allowed energy states here, oxide again no allowed energy state in between large band gap. But this transition region is non ideal and it has large number of allowed energy states. This is a energy picture of the same phenomenon. In terms of the physical defects, the physical defects are exactly at the interface; those physical defects in turn translate energetically either traps closer to the valence band, traps closer to the conduction band and traps somewhere anywhere in the middle of the band gap and experimentally you know, it has been seen that if you were to really go from conducts

valence band edge to the conduction band edge in terms of energy. In terms of your trap density you know you get a distribution which looks something like this. At the middle of the energy which is what is important as far as transistor capacitor operation is concerned.

This is the region when we are applying a gate bias. This is the region where in, we are moving the Fermi level. We are moving the Fermi level from you know accumulation towards the inversion region, because you do not go very close to valance band anyway, we do not go very close to conduction band anyway and now, this here distribution is what is called Dit because this is given as a function of energy value and per unit area value.

Per unit area at a given energy what is the trap density that is what we call Dit interface trap density in terms of number per centimeter square E v. So, from Dit if you want to get Nit, you integrate this over energy range right.

In other words, you know you get Nit as integral from E 1 to E 2 right. Dit which is of course, a function of the E d E will give you Nit. Now, you see you can sort of make correspondence with all these right. So, Dit has a unit of per centimeter square E v because your integrating over d E. You know E v gets cancelled in terms of dimensional consistency and you get the trapped density which is number per centimeter square.

So, this is what I meant in Dit. You know, this is density which is not only areal density, but also energetic. Now, what is the impact on the C-V right, what happens when you are doing C-V right, when I have flat band condition, if it is a p type semiconductor as you know, the flat band condition, the Fermi level looks like this. Bands are perfectly flat and in fact, if it is inversion accumulation condition then you know these bands will actually bend like this correct. I am just keeping Fermi level as constant I am not disturbing that and just changing the bands to sort of see what happen what is happening. Now you see when you have the Fermi level here; again based on the Fermi direct statistics you can say that everything above the Fermi level is empty.

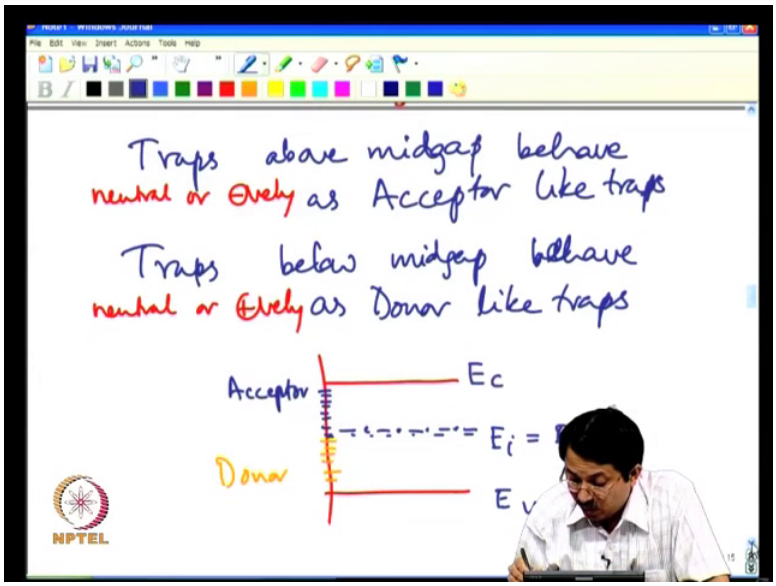
There is no carriers there, no electrons there. Everything below the Fermi level is filled with electrons and that is how we define Fermi level in the easiest manifestation of the Fermi level depletion. What happen in inversion? If I go into inversion the bands as you know we will bend down wards, you see, correct as you know the Fermi level comes

closer to the conduction band that is why it is end like now because its inverted now and here in accumulation it (Refer Time: 34:37) is very close to valance band it was very heavily repeat like right. So, now, the bands here the traps that we are looking at these are the interface traps you see. Now, what happens when I sweep the gate voltage from accumulation to inversion? The location of the Fermi level with respect to band edges is changing at the surface or the bands are bending with respect to Fermi level you know, one and the same.

So, in other words what has happened here you see, in accumulation, most of the traps were empty and inversion most of the traps are filled. So, when I am sweeping the gate voltage from one extreme to the other extreme, the charge state is changing and hence, it is not fixed charge it is a variable charge. The variable charge the exact quantity depends on the exact value of gate voltage because exact value of gate voltage intern depends on intern dictates what is your band bending and that, in turn dictates how many traps are empty, how many traps are filled right. So, now, you know the conclusion based on this discussion is that the Qit is not fixed. In other words, changes with respect to Psi s.

Psi s is changing, as a result of that you know you will also have this variation. Now the next question to ask is that now we have understood at least the charge should be change. Now is it going to be positive charge, negative charge, now how is the charge going to change. Now that depends on the nature of the interface traps and based on all the experimental studies again and lot of theoretical studies as well, a fairly good model for interface state traps has been you know involved and that essentially states that if you have traps in silicon you know distributed from the conduction band all the way to valence band edge right. The model says that the traps you know above mid gap behave as acceptor like traps.

(Refer Slide Time: 36:53)



We will see what it means by that and the traps below mid gap right behave as donor like traps. Now the donor and acceptor like essentially sort of used here you know the actual donor if you if you are talking of phosphorus as a donor you know donor is very close to conduction band correct. It donates an electron so obviously, these traps are not good donors right because they behave as donor like, but they are below the mid gap they cannot really donate if there any electrons they can catch the electron, but they cannot really give out electrons you see

Similarly, acceptor an ideal acceptor boron you know its energy level should be very close to valance band only then it acts as a very good acceptor it donates holes, but here these so called acceptor like traps are above mid gap. So, their certainly not going to donate you any holes, these traps are not going to give you any extra free carriers, but they actually instead take out the free carriers. Now when they trap these carriers the question is whether they will have positive charge and neutral or neutral and negative charge because you can only change between 2 states right. You can go from neutral to positive or you can go from neutral to negative you cannot go from negative to positive unless it captures multiple carriers that does not happen. In other words, let us consider arsenic atom.

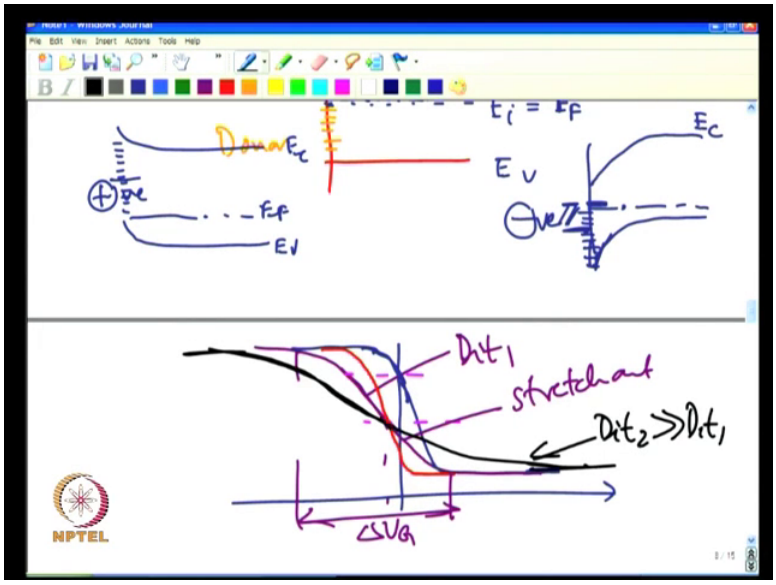
Arsenic atom can either be neutral or when it donates an electrons it becomes positive, but it cannot become negative right because even it has all the electrons filled it does not

have any tendency to get an extra electron over there you see. So, arsenic atom in silicon either be positively charged or neutral similarly, a boron atom in silicon can either be neutral or negatively charged correct, but it cannot be positively charged. So, the meaning of this is only that if it is a acceptor like trap it can either be neutral or it can be negatively charged. If it is donor like it can be either neutral or positively charged. So, that is how these states behave.

More particularly if you have an acceptor like a state, if it is filled with electron you know then that will have negative charge on the other hand, if you have donor like state if it is filled with electron it will be neutral. A donor like state which is empty of electron will be positively charged right. So, again acceptor like state which is filled with electron will be neutral. So, in other words, what you essentially have if we again look at this band picture. I mention, let us consider this is E i then this is E c E v and we just said that all these above mid gap this is mid gap above mid gap are acceptor like and all these you know below mid gap or donor like.

In other words, when my Fermi level is exactly at mid gap, if Fermi level is exactly at mid gap what does it mean all these donor like states are filled with electron. They have not donated electrons. These traps and hence, they will all be neutral and all these acceptor like impurities are empty of electrons they are not filled with electrons. If acceptor like states are empty of electrons, again they are neutral. In other words, when you have the mid gap condition, when the surface potential in silicon corresponds to the mid gap condition then interface traps do not correspond do not give any extra charge. So, that one point which will act as a pig out point will be exactly same with Qit is equal to 0 or meaning Dit is equal to 0 or Dit non zero that will be the same point.

When this starts coming down you see, when this starts coming down these acceptors states continue to be neutral because there anyway empty the continue to be empty, but some of these donor states are now getting uncovered. They will leave out an electron. Now, lot of donor more particularly when this you know, comes all the down that is, what happens in an accumulation condition. In an accumulation condition bands are bending at the surface Fermi level is very close to valence band meaning most of the traps are empty. So, anyway acceptor traps which were anyway empty is not going to give charge, but all these donor like charges will now give positive charge. (Refer Slide Time: 42:58)



So, more particularly now, when you have a accumulation condition.

This is your accumulation condition correct this is Fermi level this is E v this is E c you see all these traps are empty. Most of the traps are empty and these acceptors do not give any charge, but you have net positive charge here. Opposite thing happens in inversion in inversion the bands will start bending down the donor like traps all filled down in inversion anyway whenever they are filled. They do not give you any charge, but acceptor like traps as soon as they start getting filled they start giving you a negative charge. So, in other words, if you see here this is how you will have your correct. So, now, most of the traps are filled, because now the E c c has come very close to Fermi level. So, most of the traps below Fermi level are all filled.

Donor like traps has not going to give anything extra to me mid gap is somewhere here, but these traps which are acceptor like traps you see, they are all filled with electron they give negative charge. So, when I am going towards inversion I get. So, as I go closer and closer to the inversion I am filling more and more negative charge and the charge magnitude is increasing towards more and more negative at mid gap 0. As I start going towards accumulation the charge magnitude will again start becoming more and more negative. As we discussed here, because more and more donor states are getting un covered. So, with this, what is going to result in a phenomenon called stretch out of a C-V curve, what it means is the following right. So, now again let us look at the capacitance voltage curve.

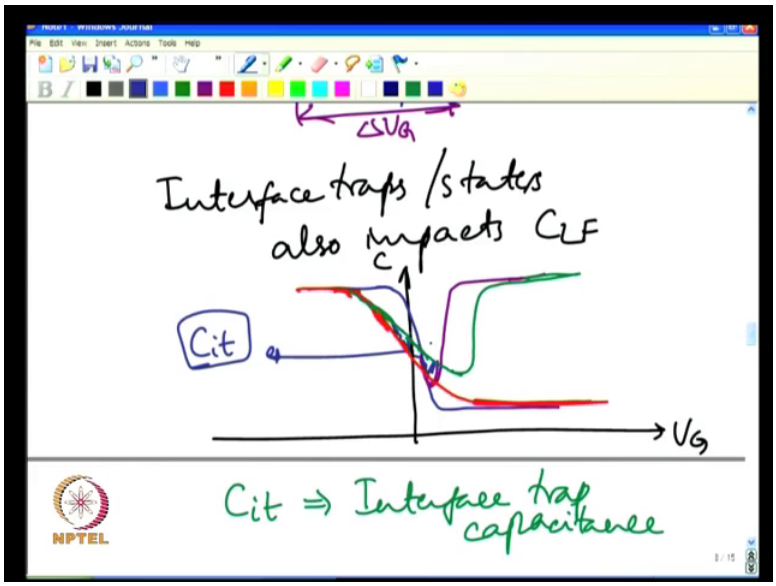
Let us say this is my ideal C-V with V FB is 0, if V FB is non zero this will probably shift have a parallel shift. Now in case of interface states right what will happen. So, somewhere here this is V FB, this is all flat band right, somewhere here I have a mid gap condition you see. This is flat band, this is deep accumulation, this is deep inversion and somewhere here I have a mid gap condition. At mid gap condition there are no extra charges because of interface states. So, which means you know your capacitance value will be exactly here for this gate voltage, but now as I start going towards this direction I start getting more and more positive charge, positive charge will tend to shift the capacitance to the left remember, but it is not fixed positive charge.

The positive charge starts increasing as I start going away and away. So, in another words this curve starts looking like this you see this shift. That shift is due to positive charge and because the positive charge is increasing, this shift is also increasing it is not a parallel shift you see, similarly in this direction I start having negative charge. Negative charge will tend to shift the C-V to the right and again more and more negative charge starts coming up and hence, the C-V comes out like this. So, another words, you see this is what we call stretch out C-V, it is as if you have taken that C-V and you have stretched it out you see. So, that it takes much larger voltage span to go from accumulation to inversion condition as compared to a much shorter voltage span to go from accumulation to inversion.

So, now, if you have higher and higher trap density that is interface trap density, your stretch out will be more and more. If let us say this is for Dit 1 and now you have a Dit 2 which is even higher than this then the stretch out is even much more. You will probably get a stretch out which look like this you know. This could be Dit 2 which is much greater than Dit 1. Again at this point you may not have any charge you know, as I will start going to the left, more and more positive charge continues to increase and in this direction more and more negative charge continues to increase as I think is right this is essentially the stretch out phenomenon ok.

This is as far as high frequency capacitance is concerned, now there is something interesting and that is this.

(Refer Slide Time: 48:11)



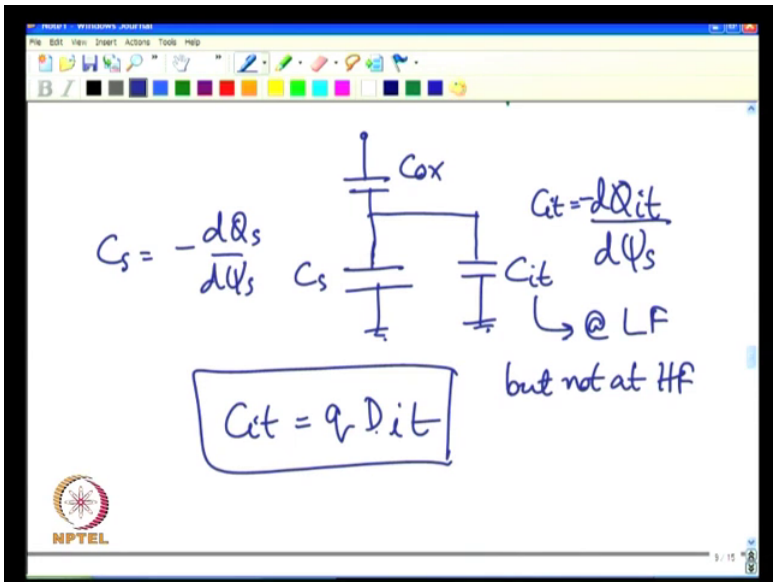
Interface traps, a traps or states you know we use it interchangeably also impacts CLF low frequency capacitance. Now, that is a little bit interesting thing to look at if I have this c versus VG. Let us say that you know I actually do the measurement instead of being very sharp ideal C-V , a high frequency C-V you know let us say this is high frequency and accordingly the low frequency will probably like this correct.

And now, because of the interface state density let us say that the C-V curve actually looks something like this. Now based on this discussion I mean we have not discussed what else will happen to low frequency C-V, the minimum that you would expect is that because high frequency looks like this the low frequency at least should come up like this and go up here. Even the low frequency should be stretched out just as high frequency gets stretched out, but very interestingly that is not the only effect for low frequency there is another effect for low frequency curve and that is, in the region between flat band to inversion that is, in a depletion region you low frequency capacitance you know your low frequency capacitance will be higher than little higher than the high frequency capacitance.

And of course, eventually, it will go up like this and indeed low frequency is also stretched out just as high frequencies also starched out, but earlier in the presence of ideal condition, meaning no Dit then low and high frequency, not only is superimposed on each other at accumulation, but also throughout depletion and then they started

departed. But here even in depletion, the low frequency capacitance is higher than high frequency capacitance and this is essentially because the low frequency capacitance value is also increase because of trap capacitance. In fact, we modeled this as Cit which stands for interface trapped capacitance.

(Refer Slide Time: 51:03)



In other words, more specifically remember the equivalent model that we had, I had C ox. I had C silicon here correct this is my equivalent and now I have something called Cit now what is this Cit? Just as C s is defined as you know how do you define as C s minus d Q s by Psi s correct. Whenever I try to change the surface potential there is a corresponding change in semiconductor charge that constitutes a semiconductor capacitance. Precisely on the same definition ass I am trying to change the surface potential traps are also changing the charge.

States there is certain charge in the traps, which we call Qit and this Qit is changing correct is precisely what we discussed I am trying to change the surface potential and that changes the charge in the traps, and hence we defined this term called Cit which is minus d Q I t by d Psi s that is when I go from one surface potential certain band bending in silicon to a second surface potential that is d Psi s, I not only will generate some charge and silicon, but I will also change the charge in traps correct. So, there is a change in voltage and there is corresponding change in charge. So, that is capacitance for you

right and that is now a trap capacitance or C it and this is a total charge that when I put a gate charge.

Accordingly this is the total charge that is responding in silicon partly at the interface and partly in the rest of the silicon and that is why we say that these 2 are in parallel. Now as you would imagine if this is a case then your semiconductor capacitance would be increasing you see, if I try to measure the capacitance C ox in series with C s in parallel with something else, you would expect to capacitance to change because of C it and that is precisely what happens in this region for low frequency, but not at high frequency very interestingly why is that? Again exactly what we discussed at high frequency I am changing the signal very fast and hence, these charges which are trapped in these defects they need some time to you know empty or full.

I am not giving enough time for these 2 empty and fill, because my measurement frequency is so fast and hence when I am doing high frequency measurement, I do not get that extra capacitance; when I am doing low frequency measurement my frequency is also low that I am giving enough time to fill these traps empty these traps as a result of that this C it will come in only at low frequency and hence this is what you see. So, C it at L F, but not at H F right make sense right and hence at any given point here at this point you do not see that difference anyway because all your capacitance is dictated by C ox and again here.

You know this is you know as expected this is dictated by the maximum depletion with minimum capacitance and again this is governed by you know whatever you have in terms of the oxide capacitance, but here where there were supposed to be exactly identical on top of each other you see this difference, and this difference you know whatever you have in this depletion region is due to C it and that is what you see. So, this is a very interesting impact on low frequency in addition to the stretch out now why did the stretch out happen again you must understand this. When I went from this gate bias to this gate bias, remember exactly what the discussion we had in high frequency, I am giving enough time for that to settle down. So, when I go from this point to this point I have given enough time to fill and empty these traps that is why there is a stretch out.

Because in order to generate that many charges in silicon to get that band bending first I need to take care of the traps started charges. So, that is why the C-V is getting stretched

out I need to put in more charge on the great because there is more charge that needs to be generated in silicon, not only for that you know the usual depletion charge, but also the trap charge and because I am doing slow step, the stretch out is responding to the slow variations slow ram that I have, but at any gate voltage my measurements frequencies too fast or too slow. So, for that measurement frequency only when it is low frequency I have higher capacitance at high frequency I do not see that capacitance you know due to interface traps because frequency is too fast ok.

So, let us just recap then what we discussed; we looked at the ideal C-V re looked at it and studied the impact on impact of oxide thickness and doping concentration, and recognize the fact that transistor structure if you do capacitance voltage measurement, no matter whether you do a measurement at high or low frequency you always get a curve its looks like a low frequency curve, because of the fact that you have this is a wire of electrons. And then subsequently we started looking at the non idealities and the V FB non zero V FB comes because of work function difference or the fixed oxide charge, if the fixed oxide charge is positive the C-V will always shift to the left if the fixed oxide charge is negative not in silicon oxide, but in some dielectrics it could be then the C-V could shift to the right.

Ok, but this is always a parallel translation no stretch out compared to ideal capacitance voltage characteristic. On the other hand when we talk of interface states these are exactly at the silicon silicon oxide transition and hence they communicate with the channel charge depending on holes electrons whatever is there you know they can easily go back and forth and hence you have a varying charge and Dit is defined as a function of what is the density in the band gap and because this is distributed in the band gap discharged state varies depending on the location of the Fermi level. And given that if we go with this model that above mid gap is acceptor and below mid gap is donor like you know then C-V will essentially stretch out with the ping out point being out here right C-V will always stretch out in place of interface traps ok.

Where is the pivert points depends, where is the charge neutral condition. Here we have said charge neutral condition is at mid gap and then finally, low frequency capacitance also gets impacted because of Dit and that is simply because there is also a trap capacitance. In fact, C it is given as q Dit this is how we define this definition will translate to this definition they are equivalent definitions. We will stop here and in the

next class we will continue discussion on other non idealities and the actual measurement and extraction of parameters.