Nanoelectronics: Devices and Materials
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Lecture - 12
Ideal MOS C-V Characteristics

Today we will look at the capacitance voltage characteristics of MOS capacitors. First we will consider an ideal MOS capacitor.

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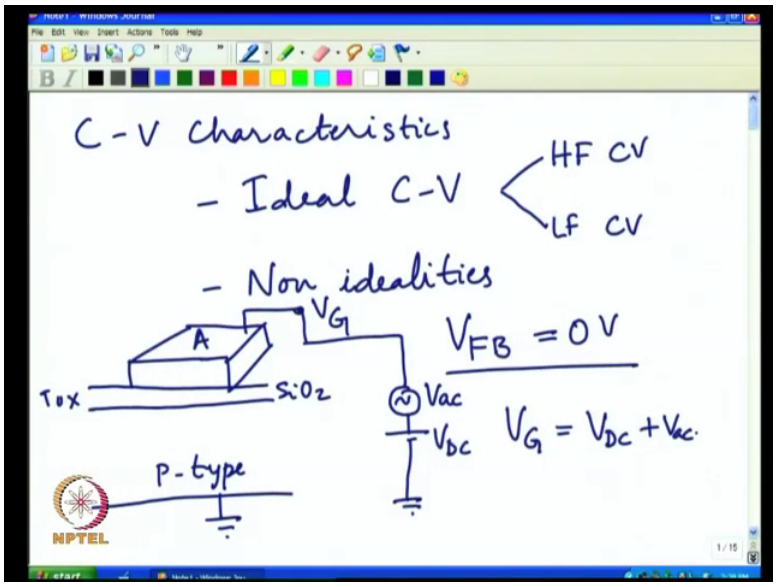

And hence we will first consider ideal C V characteristics and then we will consider a whole range of non idealities that one may encounter in capacitance voltage characteristic of MOS capacitors. So, in ideal CV characteristic, we will look at 2 kinds of capacitance voltage curves one; what we call high frequency CV and then low frequency CV. So, the device that we are considering here is as usual P type substrate silicon with a gate oxide Si O 2 of certain thickness T ox and a gate electrode of certain area. So, this is where you are applying your gate voltage and you know the substrate is at ground potential right this is a simple structure that we are considering and we are also making an assumption when I say ideal CV all it means is that I am making an assumption this capacitor has a flat band voltage of 0 volt which essentially means that.

I have a fictitious gate electrode whose work function is exactly aligned with the work function of silicon; silicon being P type material you know its work function will be the

electron affinity which is the distance between vacuum to the conduction band, then half the band gap of silicon because Fermi level in P type silicon is below the mid gap and whatever that bulk potentialized right. That is your work function on silicon I have chosen a metal which has exactly identical work function.

Let us assume that and hence and also oxide is also ideal and hence V F B is 0 that is what I mean by ideal MOS capacitor CV characteristics. So, when I am measuring this C V characteristic essentially what I am really interested in is you see Iam actually interested in variation of the capacitance with applied gate voltage in other words if you have to think of a measurement setup.

What you really have is something like this; this gate electrode is being excited by a DC voltage V DC plus an ac voltage and hence your V G is equal to V D C plus V a c. Now when we say high frequency and low frequency capacitance all it means is that the capacitance is an ac quantity the frequency of measurement here you see it can be very low or it can be very high now what is low and what is high we will see in a few minutes little later right. So, what we are doing here.

Then in order to do this kind of a measurement is that we will apply different DC gate voltages and at each DC gate voltage we will apply a very small signal ac. So, in other words if you were to look at your gate voltage.

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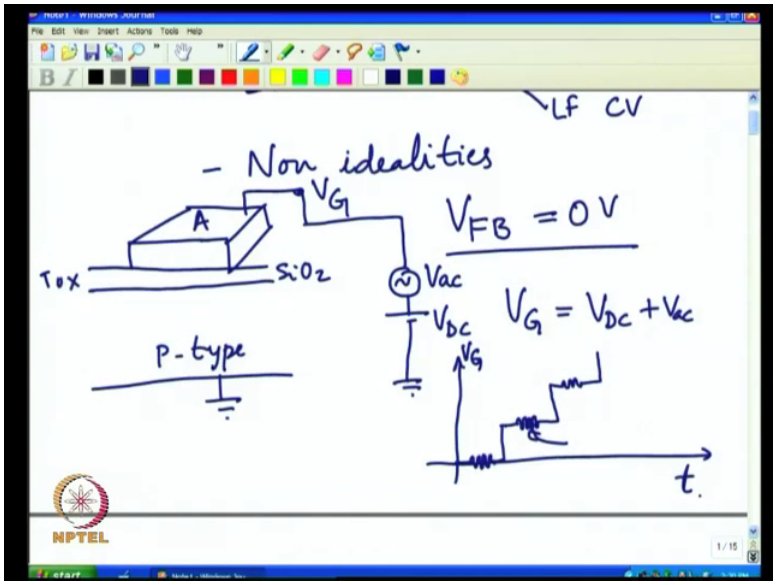

V G as a function of time what you will see is that let us say I start from 0 and go towards positive right, I mean we will typically start from negative and go towards positive right just for the illustration. So, at 0 it there is this is the DC voltage and I have a very small ac. And I do the measurement of the capacitance take a next step and apply any again an ac and do the capacitance measurement and go to the next step and so on and so forth you see. And hence at different DC values which is different gate voltage value on this MOS capacitor I am measuring the capacitance. So, this frequency of the measurement can be either low or high and that in turn gives you 2 different capacitance voltage curve which is HF and LF CV characteristics. Now let us start from the very basic that if I have a V G applied.

On the structure as we have seen in one of the earlier lectures what you will essentially have.

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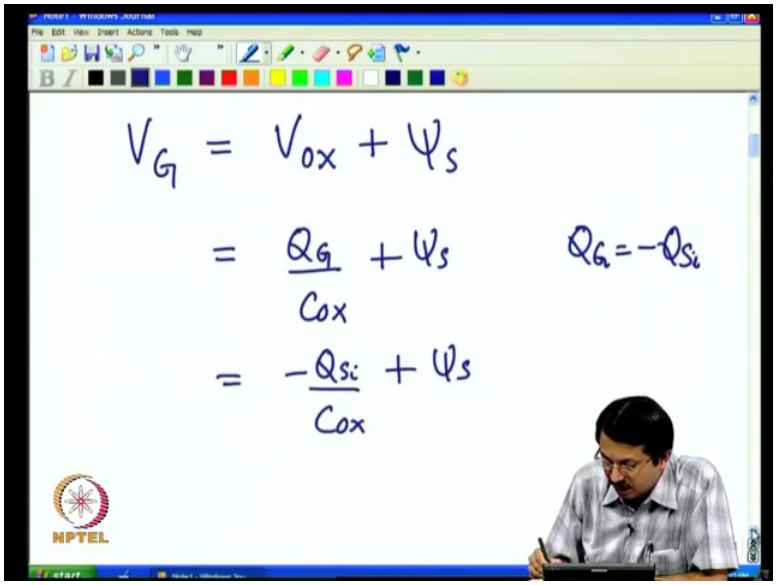

In this structure, it is can be treated as oxide in series with silicon right. So, the applied gate voltage has to drop across these 2 element part of that will drop across the oxide that is what we call V ox and the rest of the gateway applied gate voltage will drop across the silicon which is what we call psi s or the band bending that we have in silicon when we have flat band conditions psi s is equal to 0. Then whether you are applying positive gate voltage or negative gate voltage the band will either bend down or bend up accordingly your psi s will be coming become non zero becomes positive or negative, right.

So, this can be further written as what is V ox you see V ox can be written simply as QG divided by C ox plus psi s. Now remember that this is a capacitor whenever I put a charge QG on the gate that charge will be balanced perfectly by an equivalent charge in the semiconductor. So, we can also write QG is equal to minus Qs where Qs is the charge in silicon, because it is a capacitance right positive charge is balanced by the negative charge and this negative charge is in the silicon for positive applied gate voltage. Similarly if you apply negative gate voltage you have negative charge on the gate that will have to be balanced by an equal and opposite charge in the silicon it is know sometimes you see in the books this notation either as Qs or as Q silicon one and the same right. So, I can now re write this as minus Q silicon divided by C ox plus psi s.

So, let me just do a very simple mathematical operation on this equation; what I am going to do is that differentiate this equation with respect to Qs. So, that is dVG.

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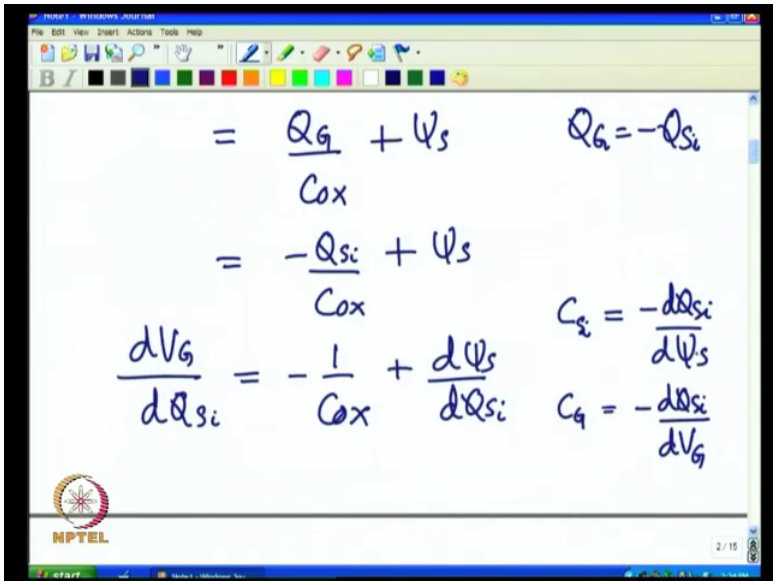

Over dQs right is differentiate this right hand side with respect to Qs you know because Qs is again Q silicon right I mean I am using them interchangeably. So, this is Q silicon by C ox. So, differentiate this is what you get you essentially get minus 1 over C ox first term correct because differential of Q silicon with respect to Q silicon is one right and plus d psi s by d Q silicon, now this is interesting now what. So, what we are defining now see this C ox is a insulative capacitance. Now these 2 quantities are really the total gate capacitance and the total silicon capacitance.

In other words what we are saying here is that we defined C silicon as minus dQ silicon by d psi s and similarly we define the total gate capacitance which is being measured in the external world as minus dQ silicon by dVG, right. So, why I am defining this as minus in reality the capacitances are being defined as plus d Q G by d psi s that is silicon capacitance my excitation was gate I am looking at how the gate charge is changing with respect to change in gate voltage because Q G is equal to minus Q psi I am making that substitution here directly right.

So, what this is telling you really is that when you know you are changing the gate voltage there is a corresponding change in the gate charge and that delta Q G divided by delta V G is my total capacitance that is on the left hand side and that consists of these 2 quantities. In other words you know if you now make use of these definitions; what you have really got is 1 over C minus 1 over C G, because of this negative sign.

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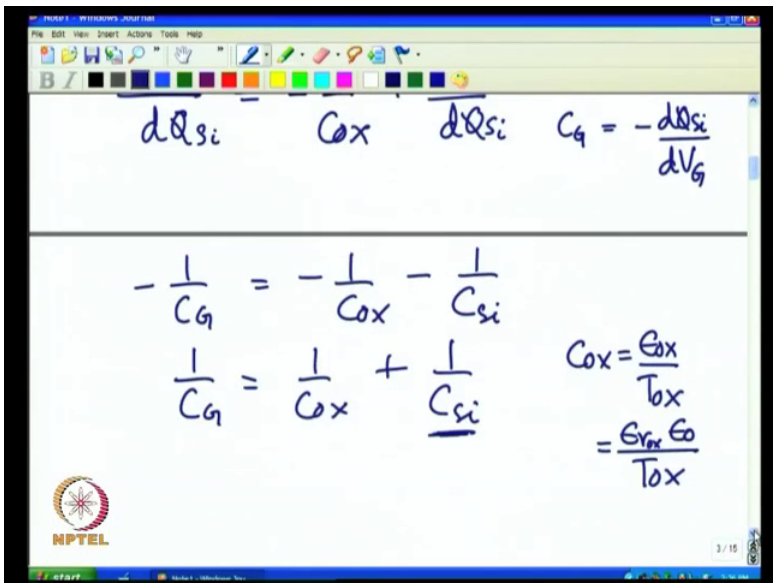

That I have is minus 1 over C ox minus 1 over C silicon in other words all this has told you is that you know cg is equal to one over C ox plus 1 over C silicon. So, what this is telling you is that the total gate capacitance that you would measure in the process at different gates steps by applying that small signal ac is going to be modeled as a series combination of 2 capacitances one is C ox which is a insulator capacitance we can define C ox as epsilon ox by T ox.

We are now presently dealing with per unit area capacitance eventually you are really interested in total capacitance when you do the measurement just multiply with that area that you have in the device, then you get a total capacitance right. If you are using per unit area on the left hand side you be consistent and use per unit area on the right hand side. So, I am just defining all these values in my equation as per unit area capacitance to just keep it simple.

So, area is a scaling factor for me now this is really you know when I say epsilon ox this is a permittivity of the oxide in other words this really is epsilon r of oxide which is relative permittivity of the oxide terms epsilon naught divided by T ox. So, what is this telling you epsilon naught is constant epsilon r ox is constant T ox once you make a device is constant and hence oxide capacitance does not change this is a fixed quantity.

However, C silicon which is defined as d Q silicon by d psi s is not constant for unit change in surface potential how much is the change in charge varies depending on whether the capacitance is inversion region whether it is in depletion region or whether it is in accumulation region.

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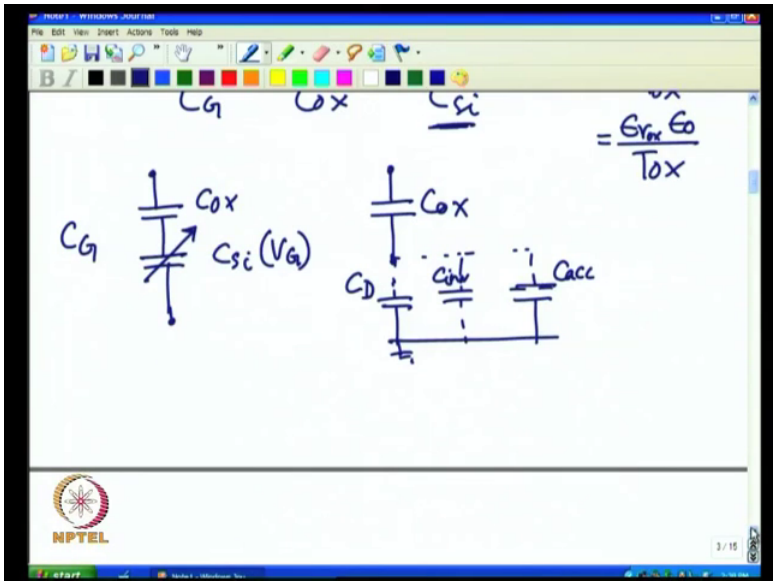

So, hence what we essentially say is that you know this is a variable capacitance and my equivalent model now is C ox in series with C silicon.

And this is a voltage dependent capacitance and the total capacitance that you see is C G you are applying V G here and this is at the ground potential this C s i is a function of V G right and as I said you know you can sort of say that this is silicon depending on the region of operation you know it is different as I mentioned this can also be shown as something like this one of this branch is active that is why I have drawn this as a dotted line depending on if it is in depletion region we call this a depletion capacitance. And if it is in inversion region that capacitance will be different if it is accumulation region that capacitance will also be different.

and this of course, remains constant and more specifically right it turns out if you recall our discussion earlier that we had in depletion the charge in semiconductor is essentially depletion charge you see because all mobile charge electron and hole charge can be neglected, right. In other words the change in charge is essentially be governed by how the depletion charge changes.

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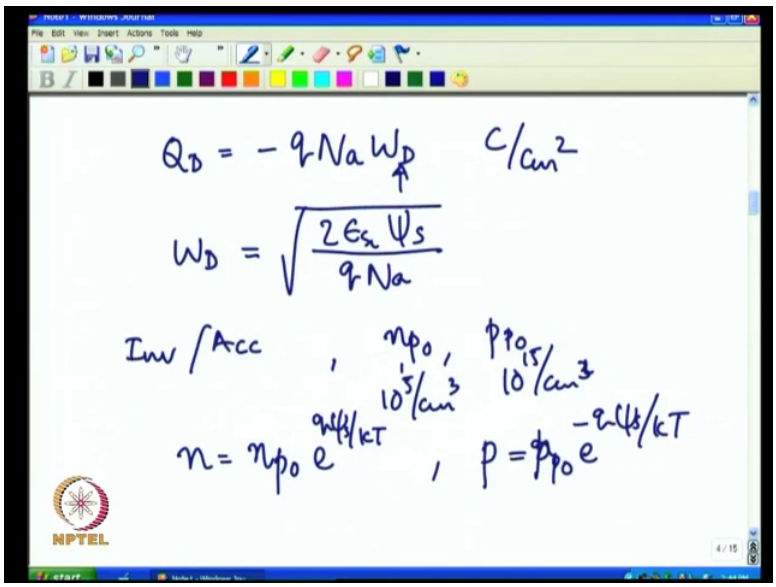

So, what is the depletion charge in particular if you look at this CD? The CD is really I will call it as you know CD will come from the depletion charge and this depletion charge is essentially right you have P type semiconductor and hence acceptor impurities which form this depletion layer that is number per centimeter cube. And hence, you multiply with the charge and multiply with the depletion width. And hence, you get coulomb per centimeter square correct, because this is number per centimeter cube

coulomb per centimeter cube I multiply with centimeter. And hence I get coulomb per centimeter square right dimensionally consistence.

So, as I said I am using all quantities as per centimeter square and it is negative because acceptor charges negative. Now, what is WD, I also had mentioned that you can make a depletion approximation right and then it becomes a one sided junction right in we have discussed this in the earlier class. In other words for an one sided junction your WD is essentially given as 2 epsilon silicon times psi s which is psi s is a voltage.

Across the depletion region you see right because psi s is a voltage across silicon and y is the voltage across silicon present because as a depletion region and hence psi s is effectively voltage across the depletion region by q Na right. So, you know now you substitute this here and you get Q d as a function of psi s right and you differentiate that you get depletion capacitance notice that Q d is only a square root function of psi s in depletion region this needs to be contrasted little later for the condition inversion and accumulation. And we will indeed see that the charge in inversion an accumulation will be an exponential function of psi s not a square root function of psi x.

So, in other words what I am telling you is that in inversion or in accumulation. The charge is not coming because of the acceptor impurities the charge is more the acceptor impurity charge if any in inversion region is more than compos I mean sort of overshadowed by the large number of inversion electrons and in accumulation region anyway there is no acceptor charge, because I am now no depletion region anyway. So, in both cases we sort of ignore the depletion charge right and the charge is either due to excess electrons or due to excess holes what do you mean the excess my initial concentration of the charge right electron and hole charge is n P naught and P; P naught which essentially means that this is a P type semiconductor as I have already told you the P type semiconductor to begin with they have a doping concentration of 10 power 15.

Let us say Na is 10 power 15 per centimeter cube it means that the equilibrium thermal equilibrium hole concentration which we call P; P naught hole concentration in P type material at 0 meaning thermal equilibrium is 10 power 15 whereas, n P naught electrons are minority carriers and electron concentration in P type material under thermal equilibrium will be n i square by Na which will be about 10 power 5 or so.

So your if you look here your pp naught will be 10 power 15 per cm cube and your np naught will be 10 for 5 per cm cube correct and as you know when I am going in accumulation the hole concentration continuously increased from 10 power 15 further up. And when I am going towards inversion this 10 power 5 would have gone up to 10 power 15 and beyond that is why I am ignoring the Na completely. So, when I am only looking at the free career charge as you know the carrier concentration here right will essentially be given by the surface potential right.

In other words, you are n carrier concentration will be given as np naught e to the Q psi s by k T when psi s is equal to 0 flat band condition this exponent term is 0 anyway and n is equal to n P naught and similarly your P is pp naught e to the minus Q psi s by k T again once equilibrium psi s is equal to 0 V F B is 0 is what we have assumed P is equal to pp naught and these numbers. So, once we start applying voltages what is accumulation? Accumulation is when the bands are bending up its becoming more and more P type you started with certain condition P type doping concentration right the Fermi level is already below the mid gap, but at the surface it becomes more and more B type the band start approaching at the surface become come closer to Fermi level right and based on our conventions bands bending up if psi s is negative.

When bands bend down psi s is positive. So, in other words when i am in accumulation this can be completely ignored because psi s is negative if anything this is going down, whereas here psi s is negative P starts increasing how does P increase with respect to psi s exponential function; similarly when I am bending the bands down wards to convert this P region into n region.

Once I reach inversion subsequent to that there is further band bending you see and psi s is now positive as you know that is why n is increasing and what is the functional relationship of n intern your inversion charges inversion charge is what related to n inversion charge is a exponential function of these 2; what does it mean a very small change in psi s results in a very large change in Q s is it not that is what we mean by exponential function as oppose to a square root function that we had in depletion. In other words we say that the silicon capacitance is almost infinite it is not quite infinite right all we are saying is that silicon capacitance is very large compared to the insulator capacitance that we have.

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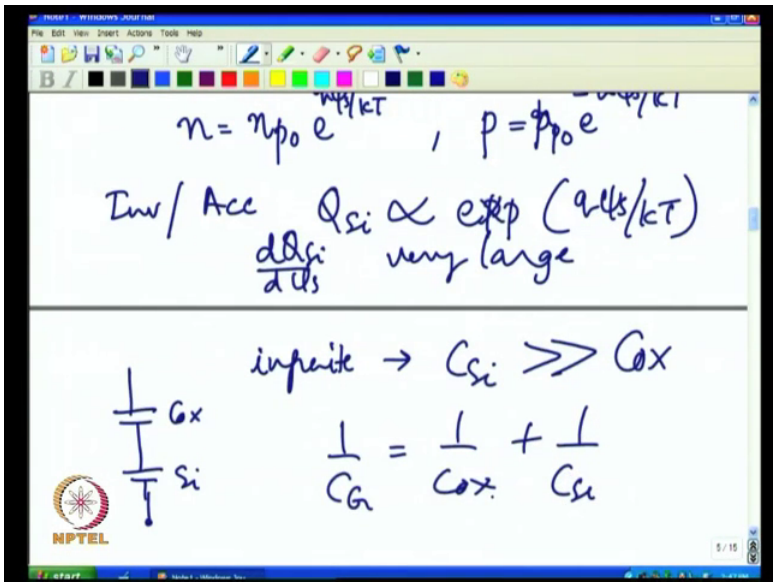

So, in inversion and accumulation condition because Q silicon where is exponentially with Psi s you are d Q silicon by d psi s you see this is differentiation of this; this is an exponential function is very large very large meaning sometimes in text book you see that its treated as infinite you know its treats an infinite all; that means, is that C silicon is significantly large compared to C ox that is the meaning right compared to C ox my C silicon is huge and hence I say infinite.

So, that you know when you have a series combination of 2 capacitors you have C ox in series with C silicon what happens to the equivalent capacitance. Remember the parallel combination that we had one over cg is one over C ox plus; once I mean this is essentially given by this when C silicon goes to infinity your total capacitance is simply oxide capacitance, right.

So, what this is telling you is that in inversion and in accumulation if the semiconductor charge is an exponential function of the surface potential psi s then silicon capacitance is. So, large that equivalent capacitance goes to C ox.

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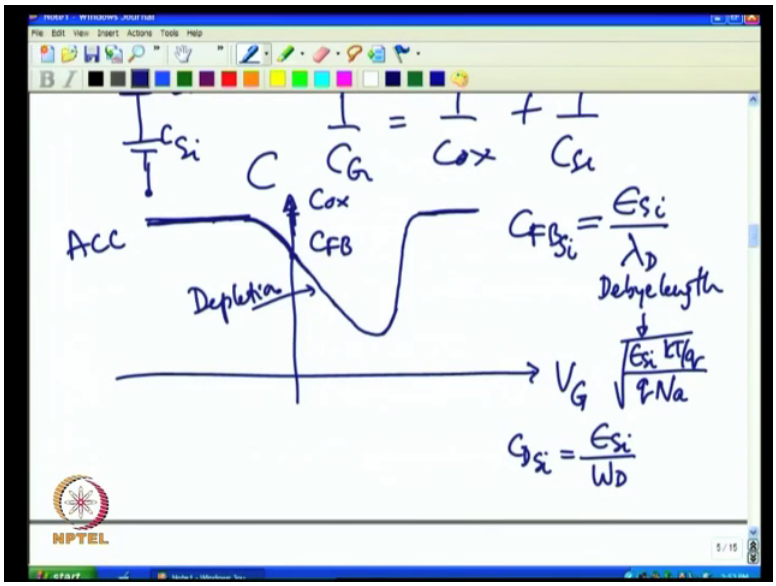

So, all it means is that if I now where to look at the capacitance voltage curve this is telling me this is a P type V F B is 0 flat band condition at 0 gate voltage and that will have some capacitance. In fact, it turns out we call it C F B flat band capacitance we will come to the definition of flat band capacitance in a minute for negative gate voltages on a P type substrate we are accumulating more and more hole right negative gate.

Voltage can attract more holes to the surface right meaning accumulation condition in accumulation condition C silicon is so large, right. And hence my capacitance should be constant right when I go to large negative voltage and what is this value this value is C ox that is the maximum capacitance I can have measured capacitance I can have in a you know MOS capacitor. And of course, when I start approaching this, it is not quite that accumulated right I mean this little bit accumulation, but not quite exponential function.

If you see when x is very low exponential function can be approximated as a linear function right e power x is x when x is very small, you see and hence when I have just started bending bands up or down up that is a started going towards accumulation right and still the change in charge is not very huge compared to change in surface potential. And hence I cannot make this assumption right and hence there is a finite capacitance which comes in series with oxide capacitance that will pull down the total capacitance and that is why the total capacitance starts coming down. Tnd this capacitance C F B is essentially defined as epsilon silicon by what is called lambda d and lambda d is called

Debye length and Debye length is intern defined as you know epsilon silicon k T over Q which is thermal voltage rather than psi s we have thermal voltage here because psi s 0 at flat band remember that we are trying to define a capacitance at flat band condition divided by Q n a.

So, this is essentially your flat band capacitance and flat band Debye length is also sort of referred to as the screening capability of semiconductor meaning if your plan electric field what is the distance over which that electric field can be screen if you have a large doping concentration it can be screen electric it is like a metal you know metal can screen the electric field you know electric field cannot penetrate inside the metal you see. So, high doping concentration results in low Debye length and low doping concentration results in large Debye length and accordingly flat band capacitance is epsilon silicon by a lambda d of course, this is flat band capacitance in silicon that again is in series this C ox and again you compute the equivalent capacitance. So, let me define this as C s B silicon understand. So, what it means is that when I have a flat band condition.

This is a silicon capacitance now this silicon capacitance as usual you see as i have shown here in this picture this is C silicon is in series with C ox. So, anytime once you know the silicon capacitance you should put that in series with C ox and compute the equivalent capacitance, because that is what you measure in the external world. So, this is defined with respect to silicon only you put this in series with C ox compute this you get a capacitance equivalent value which is lower than C ox right, because this is not infinite. This is finite beyond this I am going in depletion region in depletion region what is happening the charge is not of course, changing as fast as it was in accumulation and even in flat band condition the charge changes only as a square root function of psi s. So, which means this silicon capacitance continues to go down.

In depletion region further and farther and hence you would. Obviously, expect this to continue to go down. So, this is what we call a depletion region right and this is really accumulation region. So, in depletion region what is your capacitance against silicon capacitance as we have already seen C depletion in silicon is epsilon silicon divided by WD where WD is the depletion width this will be even lower than CFB silicon put that in series with C ox you compute the total capacitance and that is what is plotting here and eventually you reach inversion. Let us say this is my inversion voltage somewhere

here what am I expecting in inversion in inversion charge should again increase exponentially, right.

And hence I would expect this capacitance again to go to C ox this is C ox. So, and somewhere here you make this transition. So, what this is telling you is that I have started in depletion; depletion capacitance continues to decrease as you continue to you know have increased depletion width, but eventually depletion width get sprint when I reach inversion. And then the inversion capacitance is little more than depletion capacitance and that is why this starts going up, right.

So, you essentially you know reach the inversion condition somewhere out here. And when you really are in deep inversion very heavy inversion you again have gone back to your maximum capacitance and what is that maximum capacitance you have C ox as an maximum capacitance I mean this is what you would expect.

And now very interestingly this happens only if only if the measurement frequency here is low frequency we will come to that why that is the case what is low if it is a silicon capacitance that you are looking at a very high quality silicon capacitance in order to get this kind of behavior your frequency should be less than hertz, it could be 0.1 hertz or something like that depending on how good is the quality of silicon. So, this is really really low frequency let me just sketch that again to avoid the clutter.

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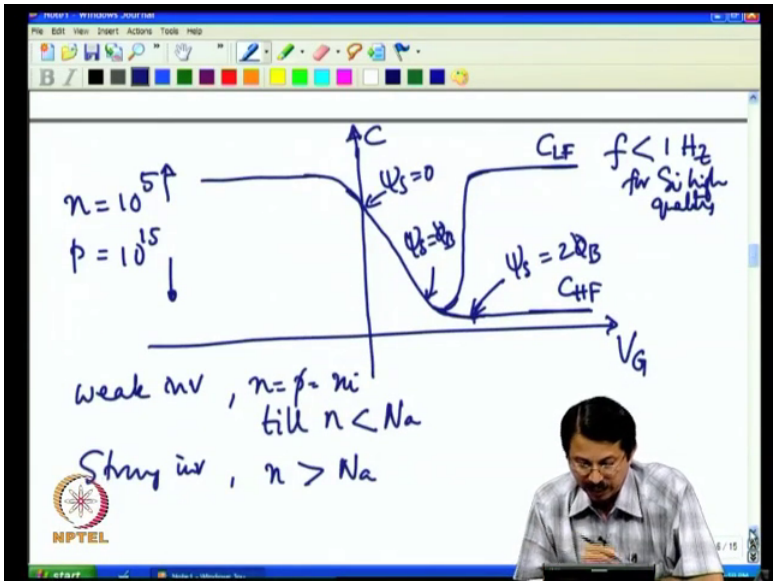

So, what I am telling you right now is that you have this V G and you have this curve here. So, here C what you get here is only under which we call CLF only under low frequency and the frequency could be less than a hertz very very low frequency for a very good silicon high quality silicon high quality silicon; what I mean by high quality silicon it has no defects and it is a very pure silicon crystal no defects in that kind of silicon you really have to go to very low frequency. If we do this measurement at 100 kilo hertz, 10 kilo hertz, these are called high frequencies; what happens is that I do not see this, instead I see a curve which looks like this and this is what we call high frequency series in other words as I go deeper and deeper inversion.

Typically you know somewhere here we say we have reached weak inversion weak inversion meaning the surface are become n like it used to be P like earlier, because the bands are bend so much electron concentration is more than hole concentration when the electron concentration becomes equal to hole concentration that is what we call a weak inversion and strong inversion is when I am sorry, electron concentration and hole concentration become equal to each other what is that intrinsic concentration right and that is weak inversion. Remember my electron concentration to begin with was 10 power 5 whole concentration to begin with was 10 power 15.

As you know this starts increasing this starts decreasing somewhere in between them it what is that that is intrinsic condition beyond that my electrons are more than holes. So, that is the point which is called weak inversion from that point onwards until my electron concentration goes to 10 power 15 which is now is equal to the hole concentration that i began with and that is what is called strong inversion. So, the weak inversion is when n is equal to P is equal to n i till n is less than Na; Na is your acceptor impurity concentration your strong inversion n is greater than Na that is your strong inversion. So, when I reach strong inversion that is when I reach maximum depletion width that is what is called WD max that happens when my band bending is 2 times 5 B right 5 B is the initial bulk potential that I had to begin with, ok.

So, here this is really the strong inversion point this point here where capacitance reaches a minimum and continues to stay constant this is where your psi s is equal to 2 5 B 5 B is your initial potential the bands are bends. So, much that P region has been completely converted into an n region at the surface and somewhere here you know you will also reach a condition where psi s is equal to 5 B you see here psi s is equal to 0 that is why

we call it a flat band condition no band bending psi s is 0 here bands are bend such that the Fermi level and intrinsic level are coinciding at the surface and that is the weak inversion from here to here i have a weak inversion condition from here onwards i have a strong inversion condition .

So, why is it that? I get a different capacitance at high frequency let us think about it I mentioned that when I am computing silicon capacitance.

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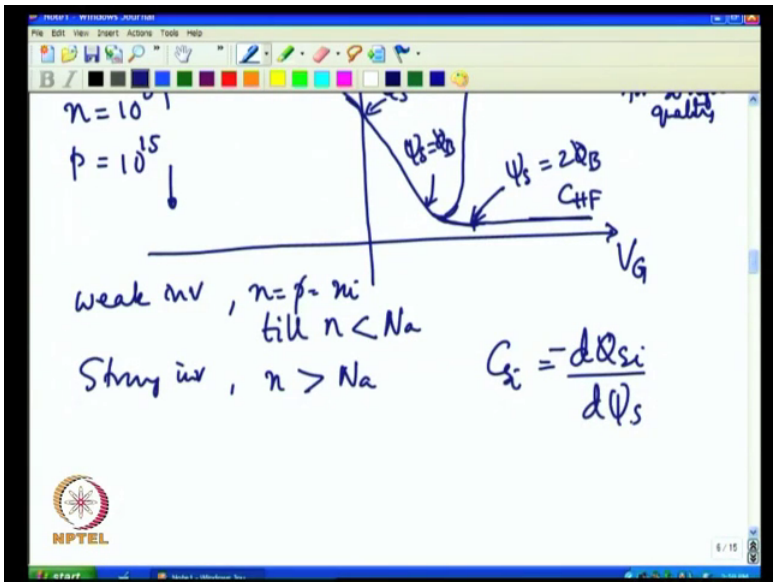

Silicon capacitance is d Q silicon divided by d psi s of course, this is a negative sign this is how I defines this when I change the surface potential a little bit what is the charge that is coming here and I did mention that in inversion the charge is dominated by the electrons majority I mean the.

Now they have become majority because they are more than Na and hence they change exponentially with respect to 5 s and hence capacitance is very large, because I made that assumption capacitance is very large the series combination went to C ox. But now we have to ask the question what are the prerequisite for the capacitance to be very large the prerequisite is that you need to have enough electrons; electrons remember or minority carriers. So, what am I doing?

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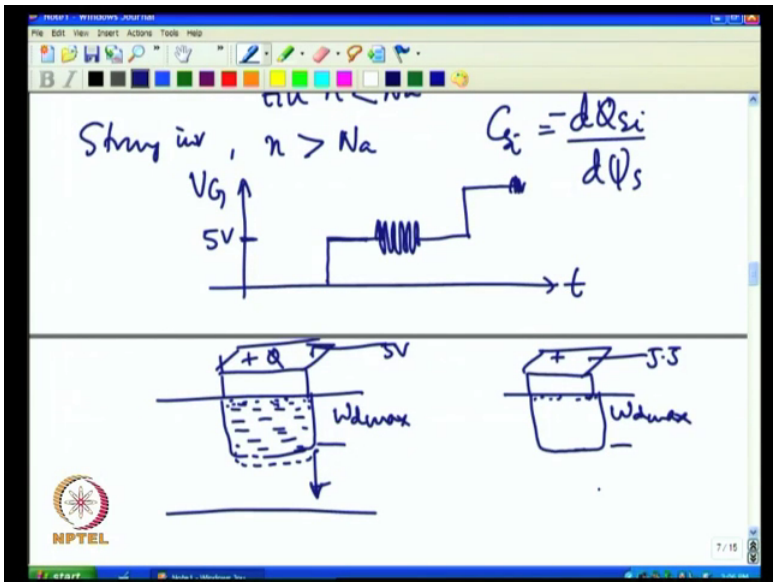

I am just to sort of remind you the wave voltage waveforms that I had earlier, I have at any point a DC and I have a wig ling ac wave from here. So, whenever I go from previous step to next step I always reach first steady state condition I reach a steady state condition only under steady state condition right.

If you have produced where are these minority carriers coming form you see minority carriers are not available there holes are already available in silicon because its P type dope. So, minority carriers have to be generated in silicon it is a electron hole pair generation that should happen in silicon if you have generated electron hole pairs then electrons go towards the surface, because the field is favorable for electrons to go to the surface and holes are of course, collected in the bulk of the silicon.

So, when I wiggle this gate voltage at high frequency you see there is a generation time just as there is some re combination time given any silicon material there is certain time it takes to generate carriers and again that generation time depends on how good is a silicon if your silicon is not at all defective the generation time can be in seconds it takes a few seconds to generate these carriers unless you generate these carriers what have I done I have plat a DC voltage remember this let us say this voltage here corresponds to 5 volt and this point is 5 volt, I am at 5 volt, I have generated a steady state electron concentration which is required for inversion, but now instantaneously I am changing the gate voltage little bit higher.

But in that could be of the order of micro second or millisecond if the generation time is one second or 10 seconds in microsecond you can generate those carriers electrons are not generated and hence whenever I am changing the gate charge the charge that is responding in silicon will not be minority carriers at the interface. In other words remember what has happened now this is the MOS capacitor that we have with certain area right and I have produced an inversion electrons here.

by applying 5 volt this 5 volt has put in some plus some Q charge here and that plus Q charge is more or less balanced by these electrons here you see. Now if I need extra electrons, they need to be generated only when there is a charge compensation happens by these electrons the silicon capacitance is very large, but when I change this charge what is the meaning of more positive voltage instantaneously. I have dump more positive charge on the gate capacitance charge balance has to happen the charge is not coming from the electrons because electrons are not there.

So, what happens; what happens is very simple what you really have in inversion condition is large number of electrons and large number of acceptor may not be as large there are acceptor impurities. So, if this instantaneous positive charge at very high frequency has to be balanced by an equal negative charge that can happen only by uncovering more acceptor impurities at the edge of the depletion region.

So, meaning that the holes here which are out here holes go away and extend is depletion region a little more and positive charge is balanced by this extra negative charge. So, the extra negative charge is not coming due to electrons the extra negative charge is coming due to the edge of the depletion region responding. So, edge of the depletion region starts moving up and down because electrons are not able to respond instantaneously because there is a generation time and electrons have to get generated in depletion region only then more electrons will come here.

If I take the next step because I am waiting for a long time again I reach for the next measurement let us say; it is a 5.5 volt when I have a 5.5 volt steady state. Again, I have a situation where in the depletion width looks exactly same as this depletion width there is no change in the depletion width because I have waited long enough. So, all that has happened when I went from DC 5 volt to you know DC 5.5 volt I have dumped at extra positive charge, but I gave enough time and hence large number of electrons got

generated here. And I have reached again a new steady state where in the depletion width is still same and now I apply small signal. So, what happens this small signal; I cannot generate electrons. So, edge of the depletion region moves back and forth right because the WD max has reached here and WD max has reached here in inversion the capacitance does not change and also the capacitance does not go to C ox because electrons are not responding.

It is only the edge of the depletion region the holes are uncovering and covering the charge and hence you get a capacitance which is a capacitance constant capacitance first of all a constant value which is not the same as the oxide capacitance value which is much lower than the oxide capacitance value and what is this value this value is essentially you know your C ox again.

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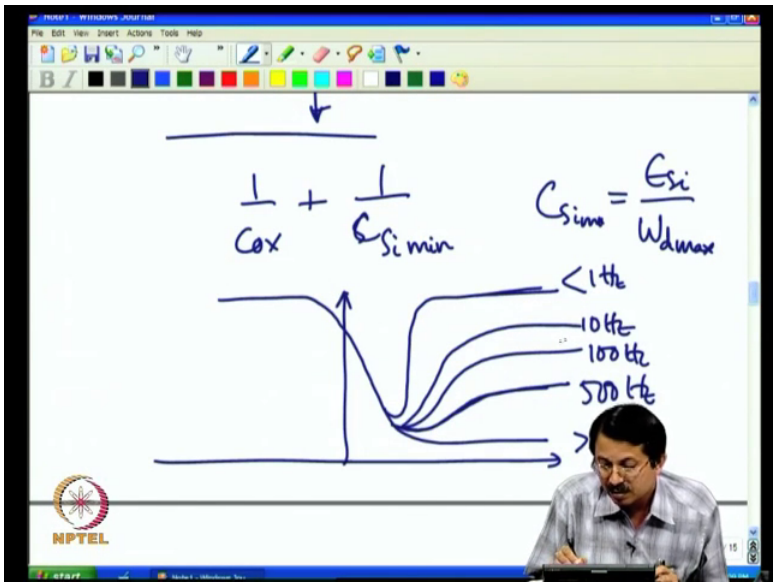

In series with C silicon minimum when we reach C silicon minimum when depletion width reaches maximum in other words C silicon minimum is epsilon silicon divided by WD maximum. So, whenever I am in a steady state inversion I always reach a maximum depletion width correct and hence the maximum depletion width remember is dependent on doping concentration, right. So, if you have different doping concentration you are see minimum will vary and then put that C minimum again in series with C ox and then you get your equivalent total measured capacitance right. So, then the key here is that if I do measurement at any frequency which is ok.

Let me get this here at frequency such as you know 10 kilo hertz even one kilo hertz could be reasonably high, but there could be a transition here you know less than one hertz is really low. So, that I am at the other extreme I am generating enough carrier enough electrons are generated. So, you are charging change in charge on the gate is balanced by electron charge which is changing and at are other extreme electrons are not at all responding because it is very very small compared to generation time.

But when the generation lifetime and yours frequency of probing are comparable you will have a transition region right. In fact, you may see curves which would maybe let me just sketch it again. So, that you know there is no confusion here as I mentioned this is really high frequency. And this is really low frequency and lay as I said, you know this could be less than one hertz and this could be let us say a greater than 1 kilohertz for example. If the generation time is of the order of second for example, then as I go to let us say 500 hertz.

You know your CV may look like this why you have some electrons responding not as many as you would have desired it right, when you go to 100 hertz you know you may get something like this. You know 10 hertz maybe something like this and eventually when they dropping frequencies and hence the inverse of frequency is that time span that you are giving is much you know larger than the generation time then obviously you are in this region, because now you know just to contrast this here again what is low frequency.

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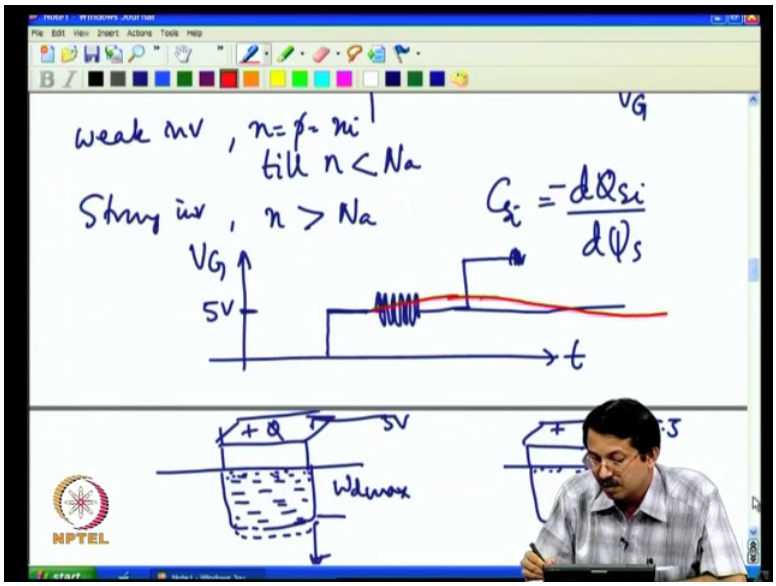

The low frequency is that it is varying. So, slowly you know I am still at the same step you see I have not change the step, because I have still not completed my measurement my frequency is very very low. And since going from this voltage to this voltage typically the ac signal is of the order of 20 millivolt; you know 30 millivolt of that time at that range because this re this voltage is changing.

So, slowly I am giving enough time at any given voltage for these electrons to respond right and hence you know you are at this extreme. So, this is very important point that you know often times I see students miss out completely why there is a change and how the transition happens right and why is it that at high frequency I continue to get the same minimum value why not different value, because in steady state remember I go to a new value of voltage I am stabilizing everything.

And hence, I am operating at the WD max I have saturated that depletion that is not changing, and because of that change in frequency only the edge of the depletion region is responding and hence the capacitance flat comes out. However, often times you may have also seen you will also see this in some text books.

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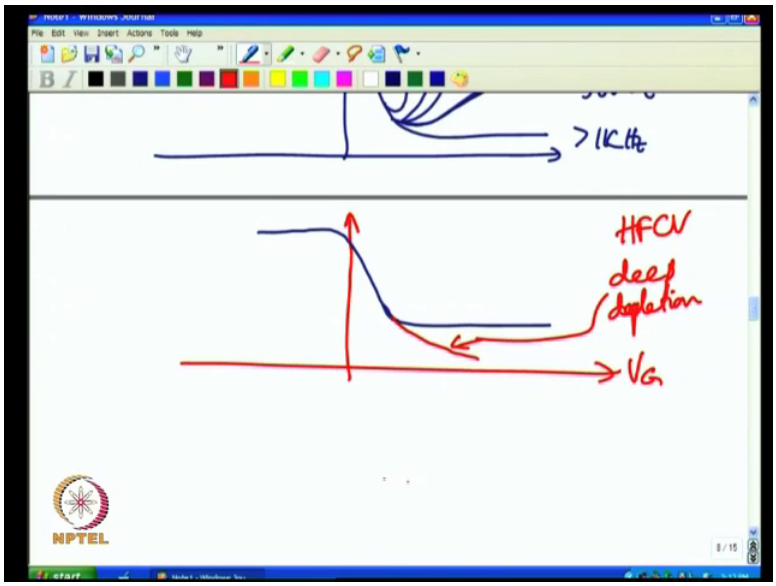

Right that if you are doing this CV measurement if you are not doing this steady state meaning.

If you do not give enough time then what could happen is that you see your high frequency should look like this it should you expect this to reach a minimum value and that minimum value is exactly gone by this WD max this WD max is exactly governed by a band bending of 2 5 B 2 5 B is the band bending. So, that you have generated enough carriers right, but if you are doing a very fast ramp right the remember there is a ac and there is a DC change with the step this step or ramp whatever you want to call.

If you do the step and instantaneously apply the voltage right meaning your effective ramp rate is too fast to reach a new steady state then what you could see is that you see some times that you are capacitance goes into what is called deep depletion. And this is called deep depletion at high frequency, I should have got the flat capacitance. Once I reach inversion, but what is happening is that when I go from 5 volt to 5.5 volt a picture that I showed you, I am not waiting enough time for 5.5 volt. So, what has happened because of that when I was trying to do the measurement of the capacitance?

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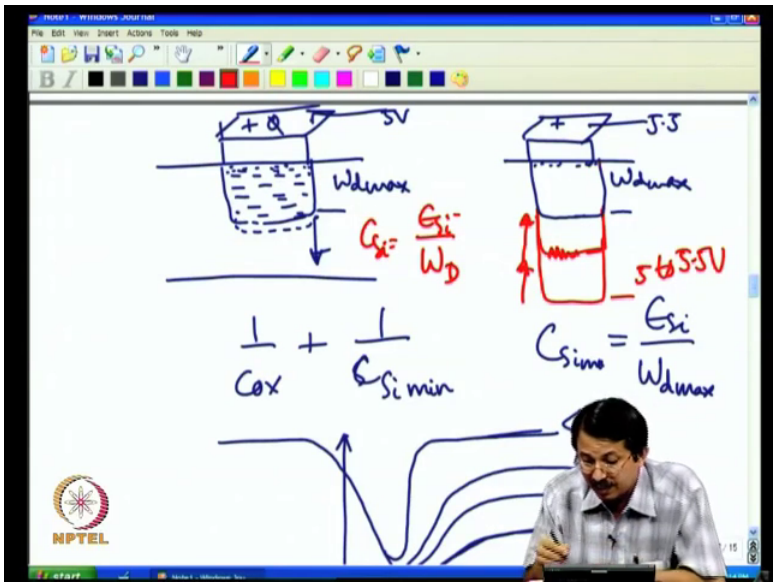

I actually had a depletion width which was deeper than what WD max would have predicted and that is why it is called deep depletion why is that because the positive charge has to be balanced by total negative charge total negative charge comes due to acceptor impurities and electrons. You will get sufficient electrons only if you wait for sufficient times, because you are not yet waited sufficient time instantaneously when I change from 5 volt to 5.5 volt. In fact, what happens is you would really have something like this.

When I go from 5 to 5.5 volt at time T equal to 0 when that step happens because I have not start generating the electrons, once I start generating the electrons this depletion width starts collapsing, because there are more and more electrons coming because of the generation and eventually for wait long enough it will go and settle down to this value you see and that is what I called a steady state going to 5.5 give enough time you generate enough electrons. So, that depletion width is still WD max, but now you are gone to 5.5 you did not wait for enough time you instantaneously wanted to measure capacitance.

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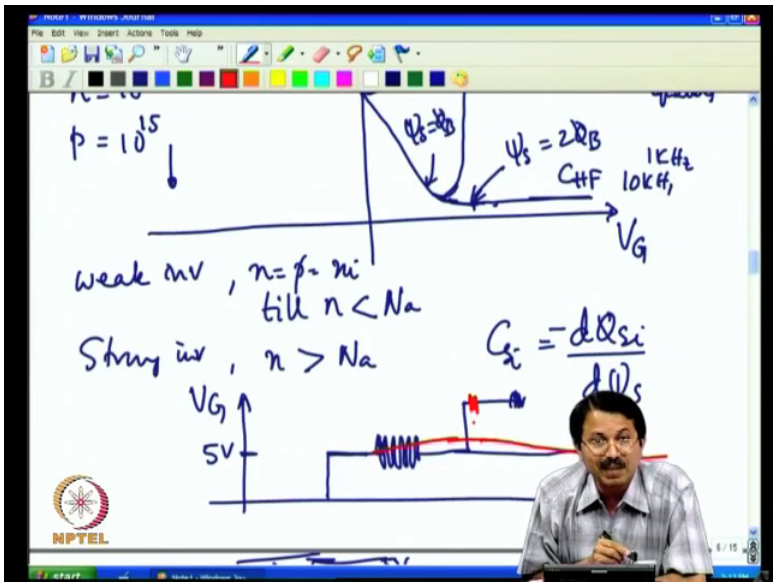

So, when you are trying to measure that capacitance the depletion width was here ok.

So, now this depletion width again will adjust itself to this high frequency because this depletion width is more than WD max they the fundamentals; will same, what is your total capacitance in silicon epsilon silicon divided by WD C silicon which will come in series with C ox, but WD is more than WD max because you did not wait enough you wanted to do the measurement immediately right.

So, if you do that you know you may get an erroneous C minimum value C minimum value which will not correspond to the steady state WD max value and that is the phenomenon which is called deep depletion as I have indicated here. So, the message again is that when you doing CV measurement your step size when you take a step size from one voltage to the other voltage give enough time before you start applying that ac voltage in other words have a very low ramp rate.

If you have a very low ramp rate, then you have a low ramp rate. So, you have a steady state from one voltage to the next voltage and then you are doing the capacitance measurement. Now maybe at this time, it is also important to mention when you do CV measurement you should do it in a properly covered dark probe stations, because you do not want any like to come in why remember the discussion that we were having. So, far in inversion especially you will have huge errors in capacitances in depletion and

inversion region if you have an ambient light why because ambient light can also generate electron and hole pairs.

So, your electron hole pair generation is accelerated by the light. So, if you do a CV measurement even if it is high frequency CV measurement if you do it with you know full blast light on the device you may actually see a curve which would look like this if this you do a HFCV with light because by shining light you have reduced the generation lifetime.

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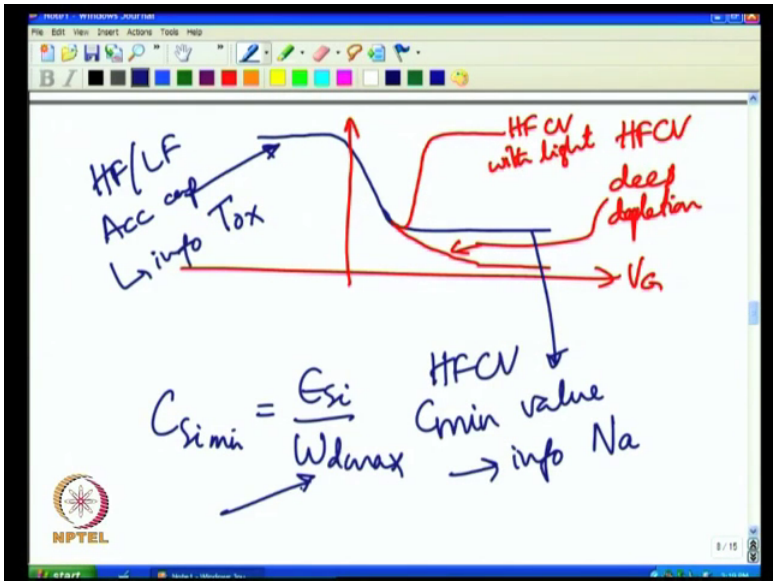

It is like photo vortex right you have a light you generate electron hole pairs when you did not have any light that is a thermal equilibrium you know given the room or whatever ambient temperature of the measurement that temperature has thermal generation the generation is only due to the ambient temperature, but if you have a light you will again get erroneous capacitance and it is important to do a high frequency measurement.

And get the right minimum capacitance because subsequently when you build devices and you want to analyze the device this minimum capacitance has very important role in analysis, because from this minimum capacitance we can actually extract the doping concentration. Although wafer manufacturer will specify 1 to 10 ohm centimeter resistivity 1 to 10 ohm is a large variation in doping concentration a particular wafer that

you are using right did it have 10 power 15 or 5 into 10 power 15 doping concentration that information you can precisely get if you do this measurement at precisely.

If you get a precise minimum value of this capacitance this minimum value of the capacitance as we will see little later in CV analysis this minimum value HFCV; C min value can give us information about doping concentration similarly it is important to get right oxide maximum value because this information either HF or LF, it does not change accumulation capacitance will give us information about T ox.

Because remember this is C ox C ox is epsilon ox over T ox whereas, this is C ox in series with that silicon with minimum capacitance, because you know C ox you can take out the effect of C ox you can actually get minimum silicon capacitance. Once you get minimum silicon capacitance you also know that C silicon minimum is epsilon silicon divided by WD max. And hence you get WD max correct once you get WD max you know you know WD max is related to doping concentration correct.

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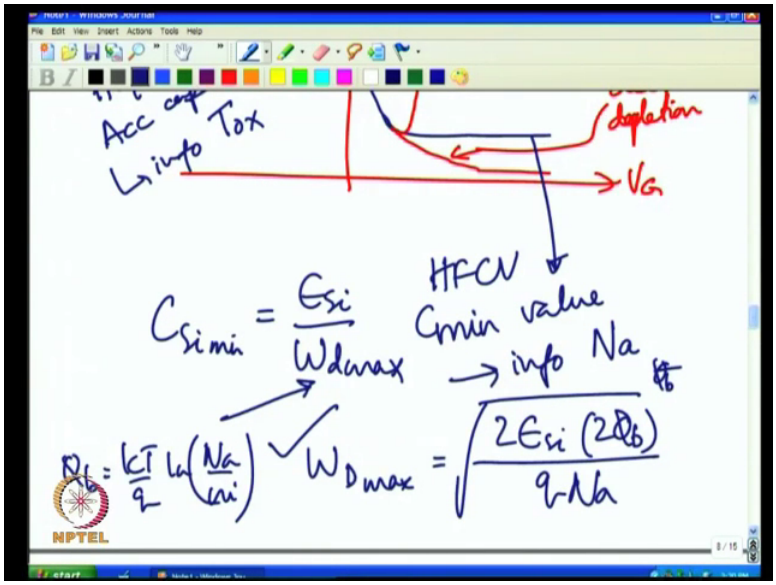

Because we already said WD max is essentially given by 2 epsilon silicon psi s what is psi s psi s is 2 5 B because I have reached inversion 2 5 B by qNa this needs to be solved iteratively because I know WD max all right, but 5 B also has Na term 5 B is k T over Q l Na over n i right that s your bulk potential 5 B right 5 B k T over Q l n Na over n i correct. So, you have a Na term here Na term here and you know the total value right you need to solve it, it is not an extra equation to solve, but you can do now iteration

technique and solvent. And hence if I have a precise estimate of minimum capacitance and precise estimate of oxide capacitance, then I can get precise estimate of substrate doping right and that is why when you do this measurement you have to be careful you make sure that you do not go into deep depletion you make sure that you do not have any other light interference and then do the measurement.

And similarly, you know if you are doing a measurement if the ambient I mean if you are for example, you were have a thermal check you heat the check right. If you increase the temperature you increase the thermal generation right again you would expect that as you start increase that temperature the HFVC start may probably start going away from this point and maybe start going look like this, because I am increasing the generation rate right anything that increases the electron hole pair generation late rate will start increasing the minimum capacitance in high frequency and start it make it higher and higher.

So, let us then summaries it for the day. So, we looked at MOS capacitor which is an ideal MOS capacitor all it meant was I considered a capacitor which as fictitious metal electrode with the same work function as my substrate work function and oxide had no charges and hence V F B is 0. So, under that condition we looked at the high frequency response and the low frequency response the response is different simply, because the charge in semiconductor comes either due to minority. I mean mobile charges could be minority or majority electrons are holds depending on whether your inversion or accumulation region and or depletion charge.

So, when it comes due to depletion charge then you get a different capacitance and that is what happens in high frequency because high frequency you do not give enough time for the chargers to generate and that is only in inversion you see not in accumulation because in accumulation; I am looking at the response of holes in a P type semiconductor. There are large number of holes there is no issue at all for holes to respond holes will instantaneously respond to any wiggle of gate voltage that you have on the gate right only in inversion your capacitances start deviating from each other only at low frequency you get the highest capacitance which is C ox similar to your accumulation, but at low high frequency you get a capacitance which is different which is determined by your maximum depletion region and that is true if you are doing this DC step and a steady state.

If you do not do that DC step under steady state you may reach this deep depletion condition. And if you reach the deep depletion condition then your high frequency minimum capacitance will be much lower than what would a theory predict based on WD max. And similarly any other aspect such as light or temperature which can influence the generation can also influence the minimum capacitance for the high frequency occur.

So, let us stop here today. And you know we will continue in the next class and we will start looking at all the non-idealities, such as fixed oxide charge, interface states and the slow called slow interface states. And you know a whole range of non-idealities how do the impact the capacitance voltage characteristics.