Circuits for Analog System Design
Prof.Gunashekaran M K
Centre for Electronics Design and Technology
Indian Institute of Science Bangalore

Module No. # 04
Lecture No. # 18

Error Budgeting for Op amp Circuits

We were discussing about operational amplifier introduce errors for DC application. There are various errors, which we have discussed earlier. There are offset voltage drift error, bias current drift error, input impedance error, output impedance error, c m R r introduced error and the gain drift of this. Then we have also discussed about the issue with offset voltage drift and shown one worked out example of the offset voltage drift, how the error was coming, and what should be done.

Then next we have discussed about bias current error and because of the bias current that is flowing in to the terminals of op amp, there is a DC error at the output, and then, how to reduce that. That is what we were discussing in the previous class. We will continue that in this class now.

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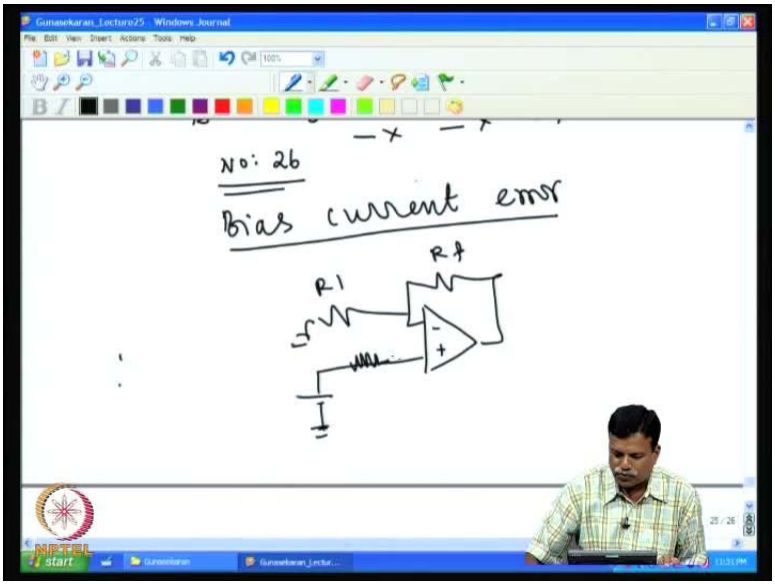

The bias current error is what that we going to discuss in detail today. In the earlier class, to remove the bias current error, the suggested method was that you have the two gain resistance here, say R_f and then R_1, and their plus input.

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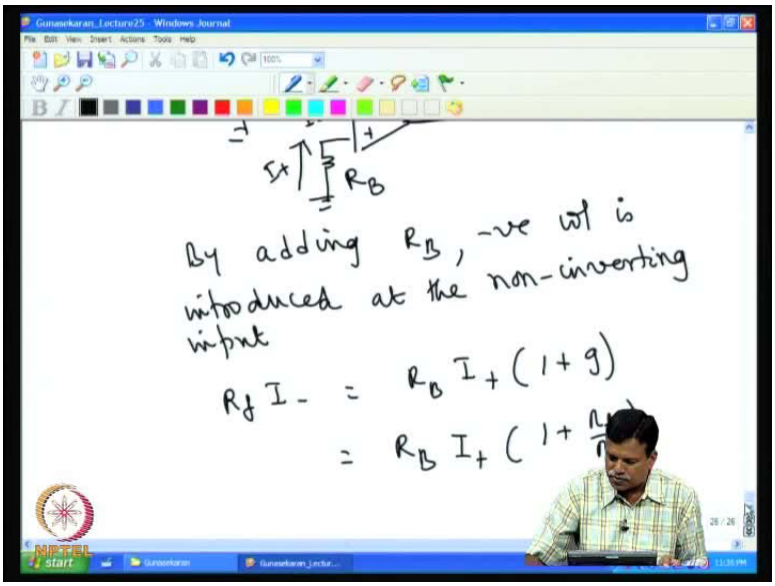

We are giving the input voltage and we had, for example, one series resistance here. There is one possibility. Or even before going into that for example, if I can look without the input. What we can do is you have the input voltage here, assume there is no input voltage, I supposed to get 0 output voltage that we can achieve by putting this resistance R_B. We had shown earlier, because of the bias current that is flowing into the input terminals of the op amp, current actually flows through this. From the output, it flows into this and then this flows into this. Then we assume, I minus equal to I plus. If I add this resistance then this current also flows this. I plus is flowing here then I minus is actually flowing here. This is actually I minus, this current.

By adding this resistance, you are generating minus voltage. By adding R_B, negative voltage is introduced at the non-inverting input. So, this negative voltage is compensator by positive voltage introduced by R_f.

The bias current that is flowing here to this terminal, produces a positive voltage here. The bias current flowing through this produce a negative voltage at the output. So, to compensate that, we have to make the output voltage equal to 0. That means, if I take R_f into I minus, it should be equal to R_B into I plus at come. That will make the output voltage equal to 0. There is no error due to the bias current.

That means, we assume that the input voltage is R_B into I_B, is amplified by 1 plus gain. I had to put 1 plus g here because whatever voltage that is applied here is amplified by the gain, that is, 1 plus R_f by R_1 and that is produced at the output.

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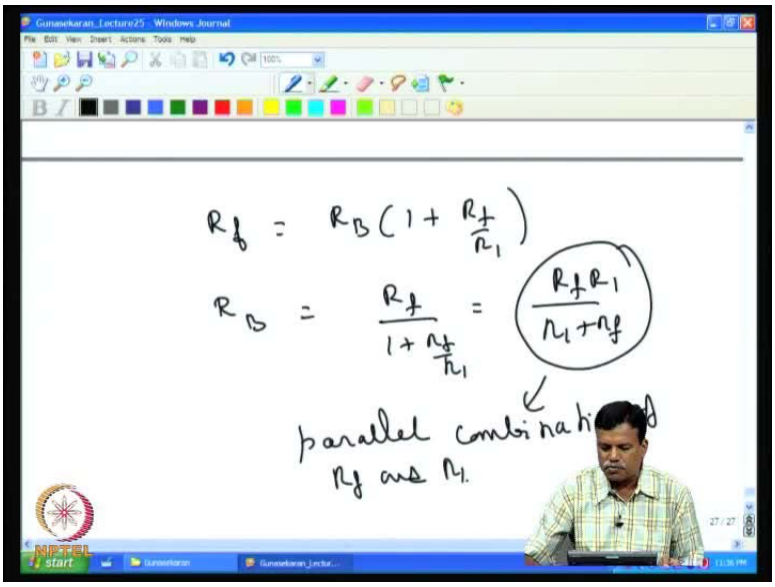

If you continue this, that will be R_B into I plus, then you will get 1 plus R_f by R_1. that is what you will get this amplify equate I plus and I minus, soon you will get R_f will be equal to R_B into 1 plus R_f by R_1. That is because we want to know R_B and what is to be connected there to what is to be connected at the non-inverting input to compensate the error that will make R_B equal to R_f by 1 plus R_f by R_1. On simplification, you will get this $1R_f$ and 2 R_1.

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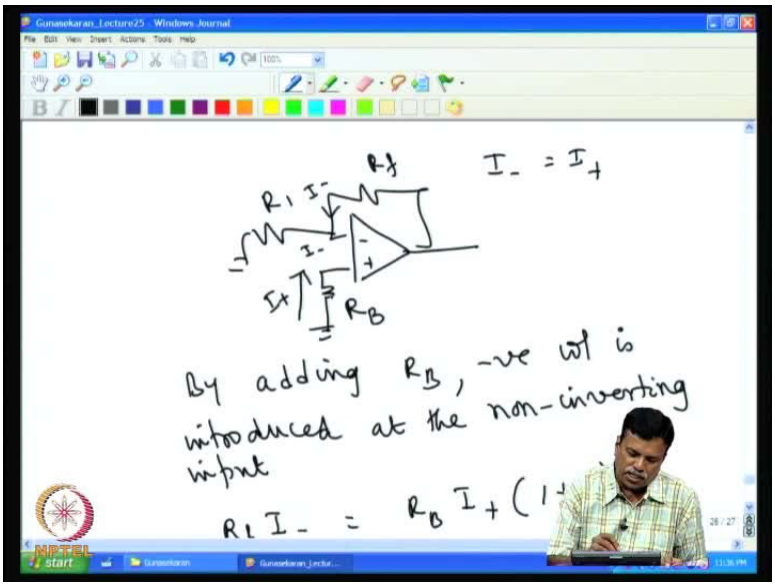

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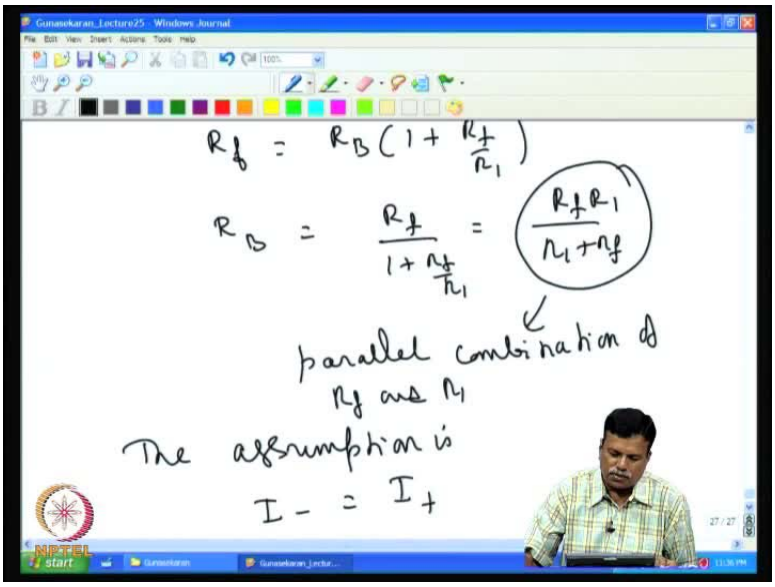

So, R_B will be parallel combination of R_f and R_1 because this is the nothing but appears as a parallel combination of R_f and R_1. That means, R_B value should be selected such that that is parallel combination of these, two is added here, that gives output voltage 0. Here the assumption is, I minus is equal to I plus. That is, the two bias currents are equal. But in actual case, they are not equal.

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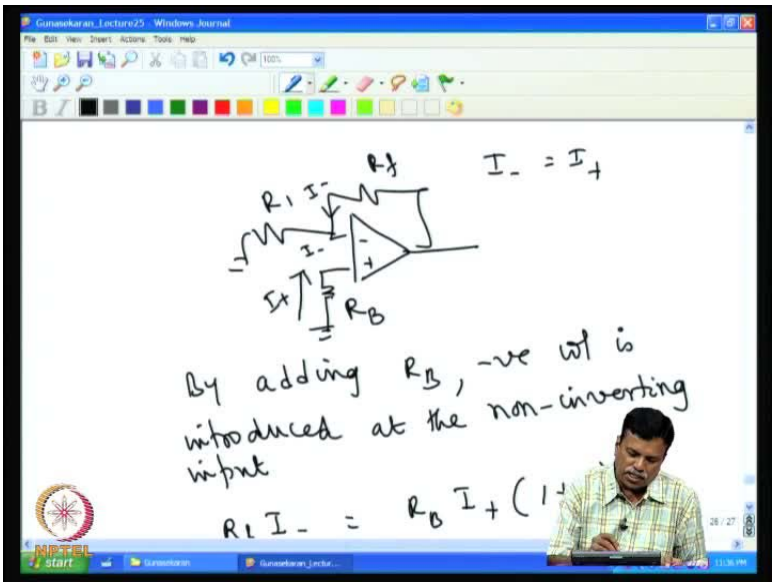

Now, we have to worry what happens if these two are not equal. If they are equal then one can make the parallel combination of these, two resistors can be put here, then one can forget about the bias current effect. But unfortunately, I plus and I minus are not equal and there are also changing with the temperature.

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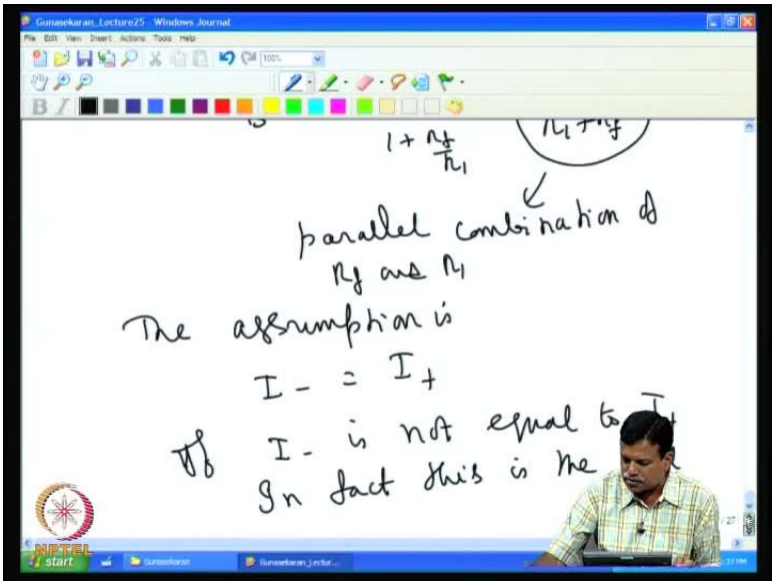

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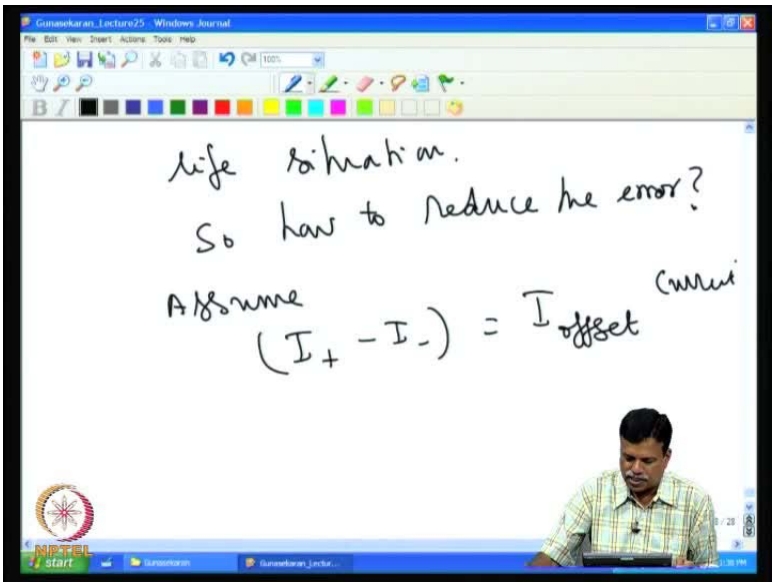

That means, we have to find out what is the net output error, if I minus is not equal to I plus. In fact this is the real life situation. How to reduce the error? Assume I plus minus I minus as I offset. So, the difference between the two currents, we call it as offset current. Offset current is the quantity that is given by most of the operational amplifier manufactures. If I know offset current, I should able to find out the error.

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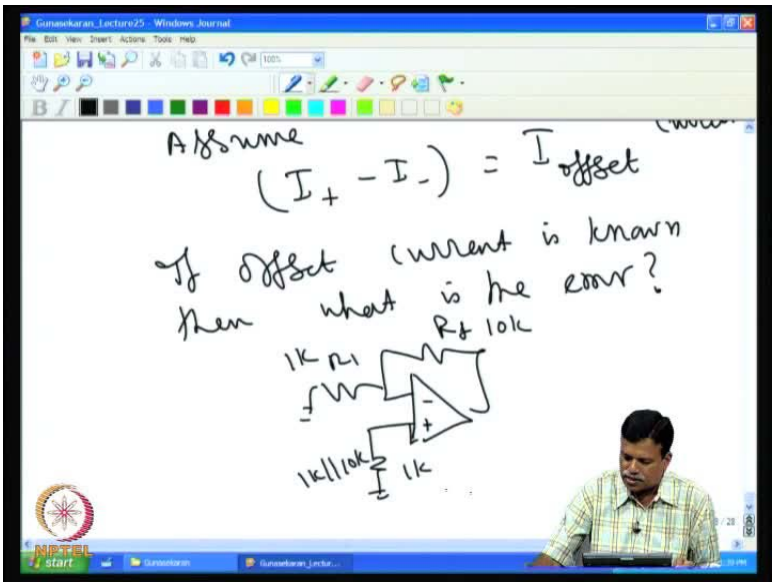

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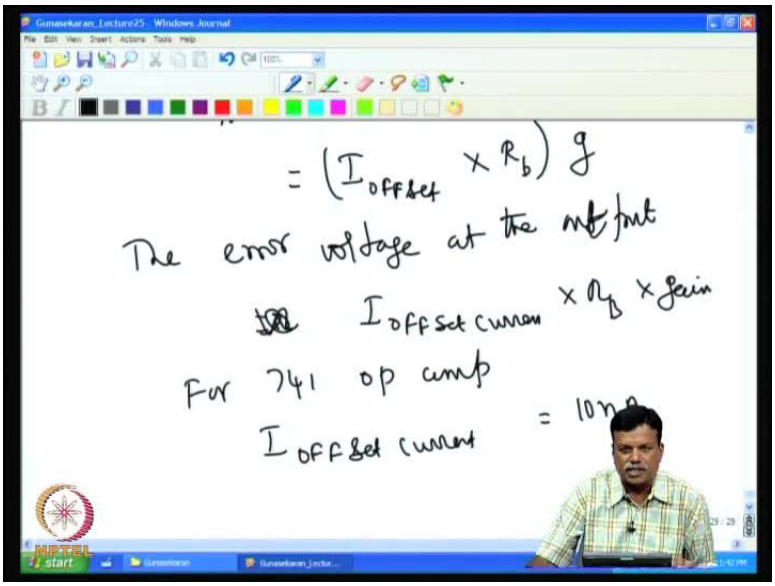

If offset current is known then what is the error? That is the question. If it is known, then if you look at the circuit again that you have the two resistance here, assume that I had put here – R_f and R_1 and it is 10 k and 1 k. In the parallel combination, these two will be 1 k parallel 10 k roughly. 1 k you will be getting it here. So, close to 1 k will be the resistance that you began to here. If offset current I offset is there, then the extra error that is coming here would be... Then v output error is equal to I offset into R_B into gain. We can assume that this plus current is more. One way of solving this would be assume this current is more and then this current is less. Then I can assume that this resistance is put parallel connection of this two, which makes output 0. So, I can neglect I plus, and I can subtract I minus and assume that only that much current is flowing here.

We can say now that net current flowing here would be the offset current. Offset current into this resistance will be the error voltage at the input, multiply by the gain, is the error voltage at the output. That is where this equation had come. So, the error voltage $v_{0,}$ that is the error voltage at the output, is equal to I offset current into R_B into gain.

Now, this offset current depends on the operational amplifier. For example, if I take 7 4 1 then offset current error is given as per example for 7 4 1 op amp. I offset current is equal to about 1 nano ampere. So if I have 1 k resistance then you will have only 1 micro volt. But if you 10 nano amperes, where as if you take bias current by itself there, it is fifty nano ampere level. Offset current is much smaller. The error reduced by the offset

current is smaller, if the resistance values are small. If the gain is 10, and if I used 1 k and 10 k, the error v_0 would be 10 nano ampere into 1 k into gain 10. That actually amounts to 10 power minus 4 volt at the output. That is point. 1 milli volt error at the output we give because of 7 4 1.

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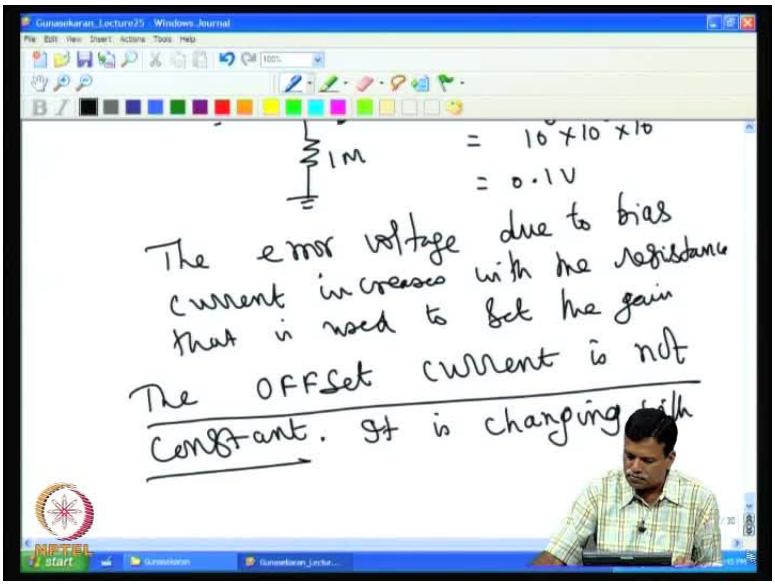

If I use gain 10 with 1 k and 10 k combination, if I go for higher resistance, the error comes very high. For example, if I set a circuit, that is, the same gain 10, I go for 9 meg and then 1 meg, which gives me the gain 10. Then I put this, which will be 1 meg. Then the error would be v_0 error would be 1 meg into 10 nano ampere into gain 10, so that will be 10 power 6 into 10 power minus 8 into 10, that is 0.01 volt. The error voltage due to bias current bias current increases with the resistance that is used to set the gain. Higher the resistance when we have, more problem due to bias current will be there. Actual problem is not the bias current or offset current. This offset current is not constant. The offset current changes with temperature change. This is the major problem rather than the offset current itself.

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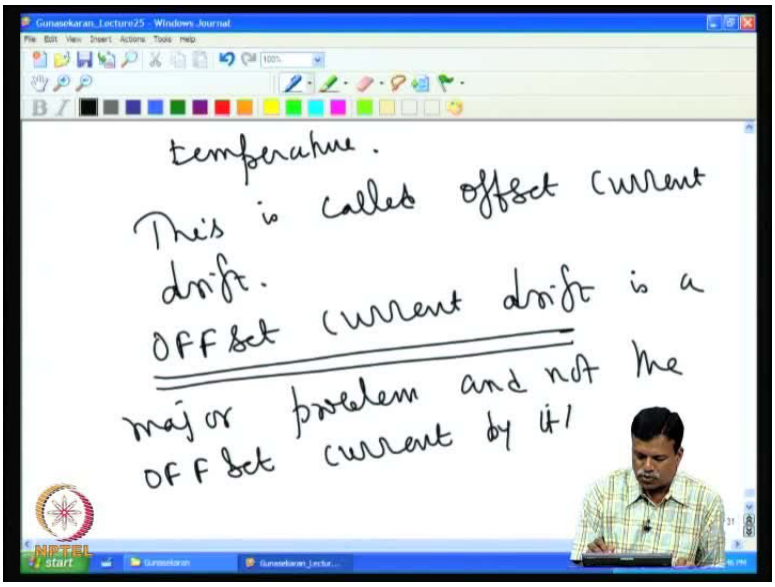

So, the actual problem is the offset current is not constant. It is changing with temperature. This is called offset current drift. Offset current drift is a major problem and not the offset current itself.

This offset current drift is the major issue, next to offset voltage drift, because offset voltage drift is independent of resistance that we are using. But offset current drift depends upon the resistance that we are using.

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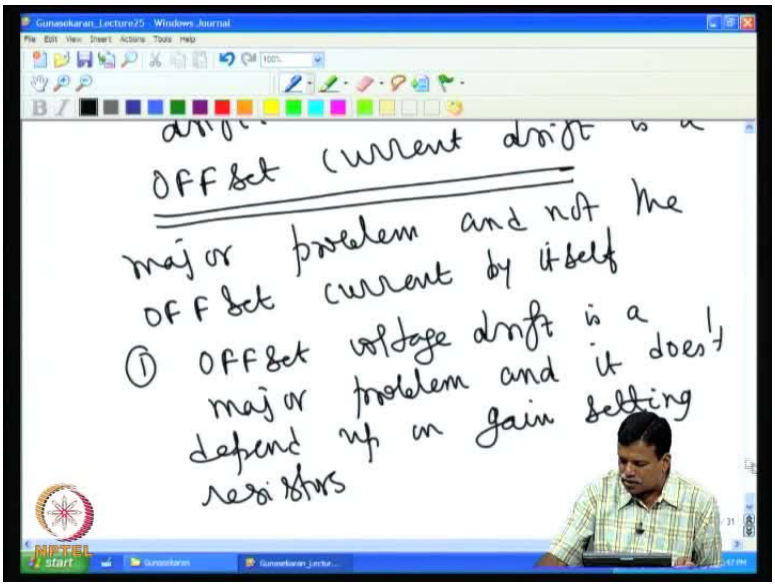

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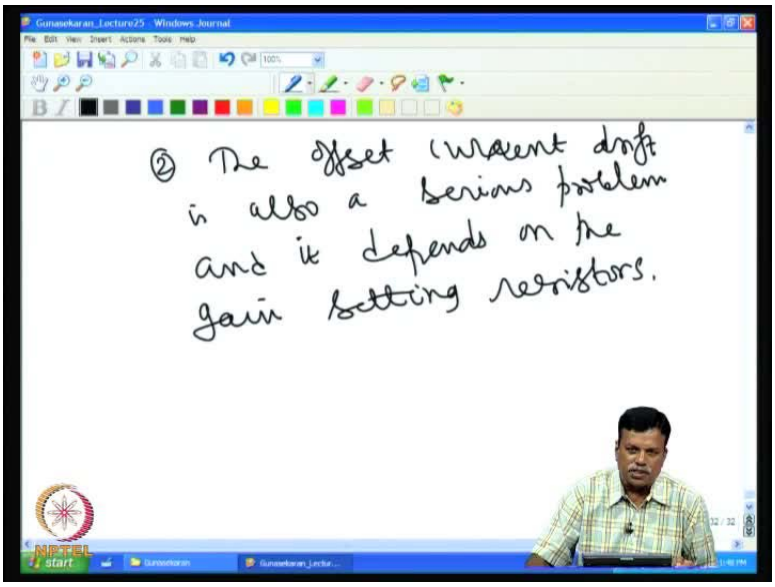

Offset voltage drift is a major problem and it does not depend upon gain setting registers. Now, the offset current drift is also a serious problem and it depends on the gain setting registers.

One has to be aware of these two problems, that is, offset current drift and offset voltage drift. And these two are the main limiting factors in operational amplifier DC applications. In AC applications, we need not worry about this parameter. If we were using operational amplifier for DC applications, one had to worry about these two parameters – offset current and offset voltage drift.

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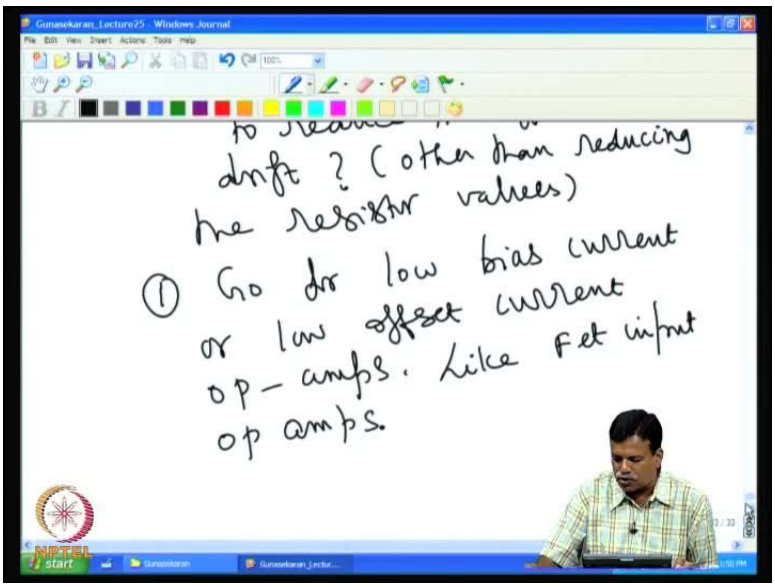

Now, is there anything that one can do to remove the offset current drift or offset voltage drift? What is that one can do to reduce the offset current drift? What we are trying to do is other than reduce in the resistance value in the feedback network. What else we can do is to reduce the offset reducing the resistor values.

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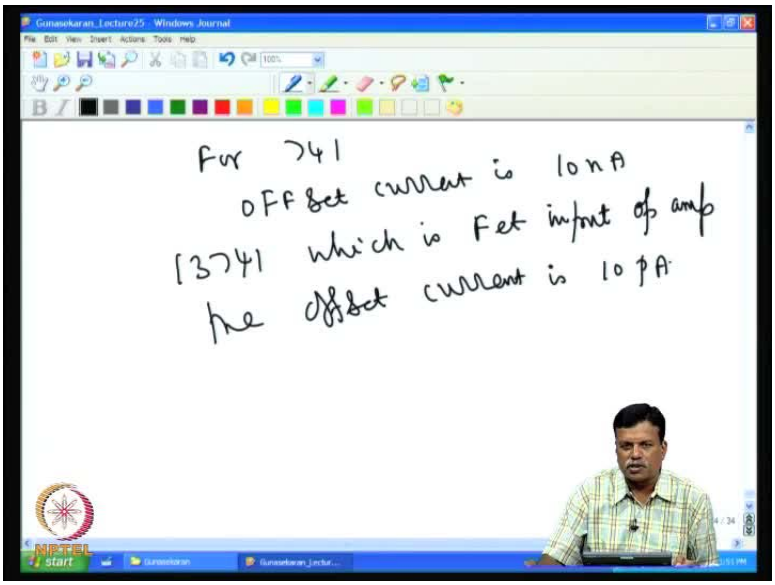

Only choice you have is to go for low bias current or low offset current op amps, like fet input op amps. If I use low bias current op amps, obviously the offset current will come down and offset current drift will also come down. Fet input op amps are the good choice to reduce the error due to the offset current. For example, if you compare 7 4 1, where offset current is 10 nano amps with a same think fet version available for 7 4 1, which is fet input op amp, the offset current is 10 pi amps. The pi amps, say about three others less, that is, about thousand less. So, the offset current drift officially comes out less and error introduced by that is also less.

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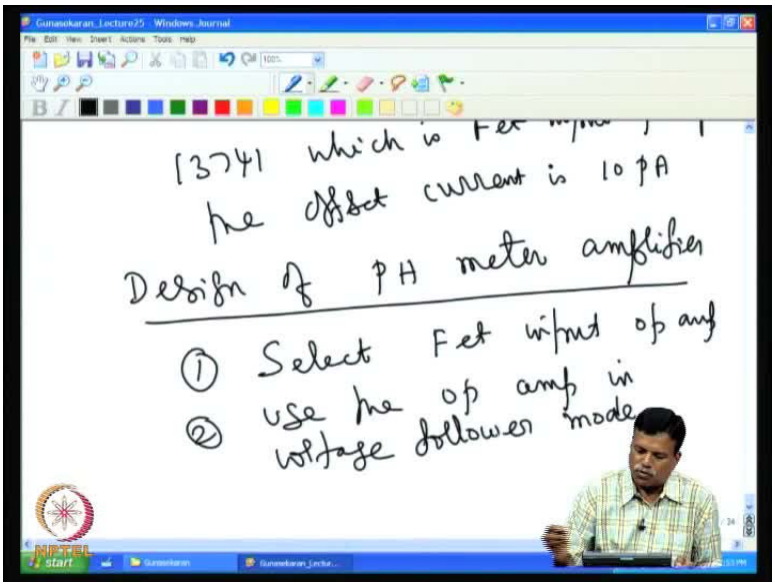

If you really want to use very high resistance values, one has to go for fet input op amp. For example, if we take ph meter amplifier then we can understand the issue with offset current much more easily. For example, take a design of ph meter amplifier. If I take p h meter amplifier, then the circuit that one... First thing is that we select fet input op amp. Second is the use of op amp in voltage follower mode. We will explain why one not is use in voltage follower mode in case of ph meter. This we will explain little later.

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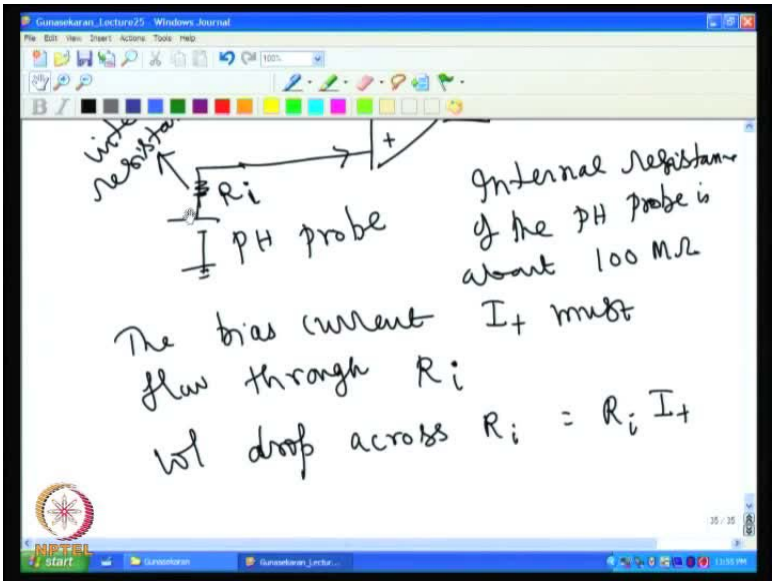

We will take the operational amplifier, then I use voltage follower mode, and the input i will connect ph meter. For example, you take ph meter, p h probe. We have taken this

example of ph probe because ph probe got very high internal resistance. Internal resistance of ph probe is about 100 mega ohms. So, the internal resistance is very high.

If you look at the bias currents, they actually flow here. The bias current that is flowing in to the inverting terminal has no problem because they do not develop any voltage as there is no resistance here. So due to current I minus, there is no problem. Where else? This bias current has to go through this to the plus input. Now, the bias current has to go through this 100 mega ohm resistance. When they go through this, the voltage occur on this. So, essentially, the bias current I plus, that is, non-inverting terminal bias current I plus, must flow through... I call it as R_i input through R I. Voltage drop across R_i would be R_i into I plus. Actually, the current is flowing like this. This voltage is minus, so the net input voltage will be voltage of the ph probe minus voltage stop that are occurred.

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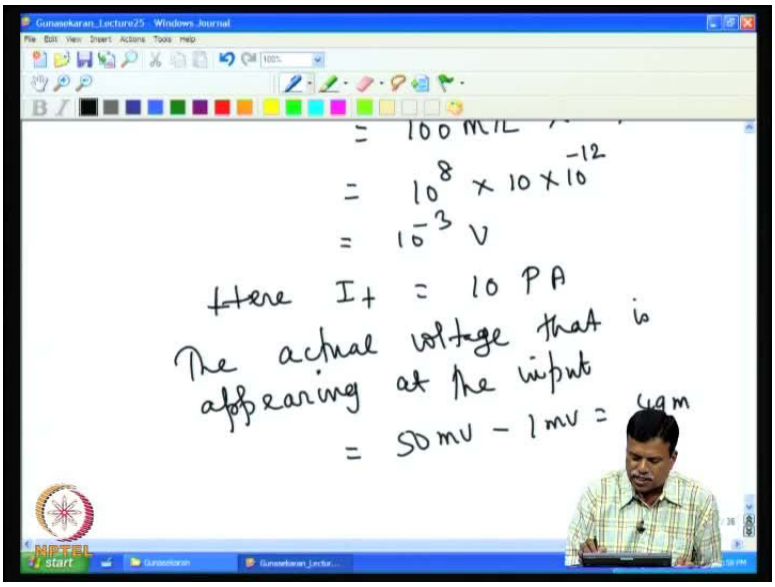

Assume that ph probe gives you 50 milli volt per ph. So, ph probe voltage is equal to 50 milli volt. We assume that. Then voltage across R_i is equal to 10 mega ohm, the resistance power 8, that is, 100 mega ohm into I plus, that is, actually 10 power 8 into I plus. Suppose, if it is a 10 picoampere, then it will be 10 into picoampere, so that will be minus 12. Then that will be 10 raise to the power minus 3 volts. Here we have taken I plus. I plus is equal to 10 picoamps. The bias current is actually very small. So, the error what you get is 1 milli volt. The actual voltage that is appearing at the input is 50 milli volt, which is ph amplifier minus 1 milli volt amplifier, that is, 49 milli volt.

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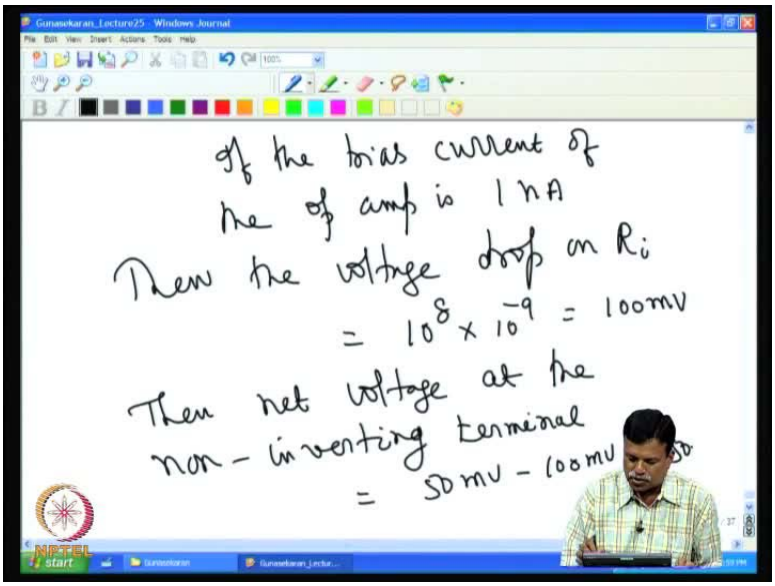

In this case, error is very small. Suppose if I use op amp, which is having 1 nano ampere bias current, that is, if the bias current is 1 nano ampere, then the voltage drop on R_i will be equal to 100 mega ohm into 1 nano ampere, that is, 10 power minus 9, that will be 100 milli volt. Then net voltage at the non-inverting input is equal to to 50 milli volt minus 100 milli volt, that is equal to minus 50 milli volt. It is a huge error.

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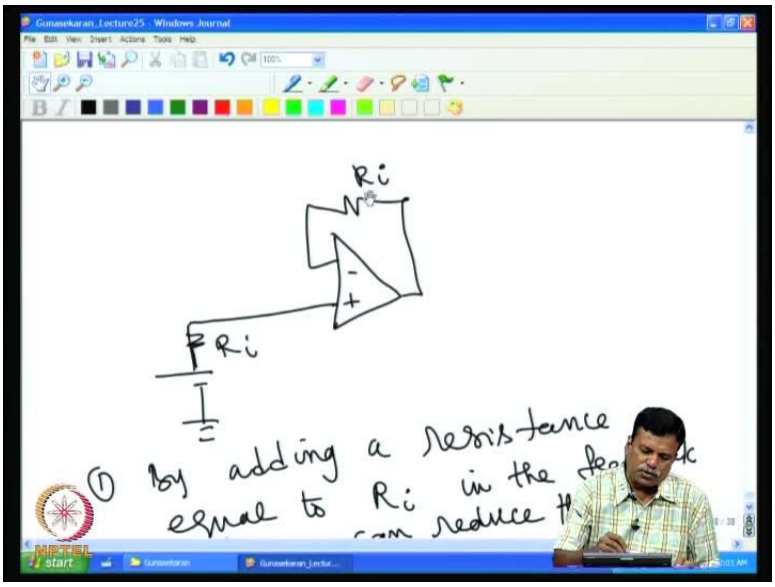

The input voltage 100 milli volt error comes because of the bias current. One can make a voltage follower to take care a part of the bias current because we can also have

resistance connected here. Then I can have plus here, if I know this is R_i. I will also keep R_i here. Then if these two bias currents are equal, if the bias current of this and the bias current this are equal and output voltage will be 0, so one can reduce the bias current introduced error in the voltage follower by adding a resistance R_i in feedback path.

By adding a resistance equal to R_i in the feedback path, one can reduce the bias current error. However, we can only reduce, we cannot make it 0 because of the two points. One, it is not easy to find out exact value R_i, and one will not able to put it here because the R i itself may be changing from transistor to transistor.

It is not easy for each transistor to find the R_i and putting the exact value. Nevertheless, error can be reduced by making more or less equal value of R_i. By connecting equal value of R_i in the feedback path here, reduces error because of the bias current. We know that even if I make it this two resistance equal, this and this equal, this current and this current may not be equal.

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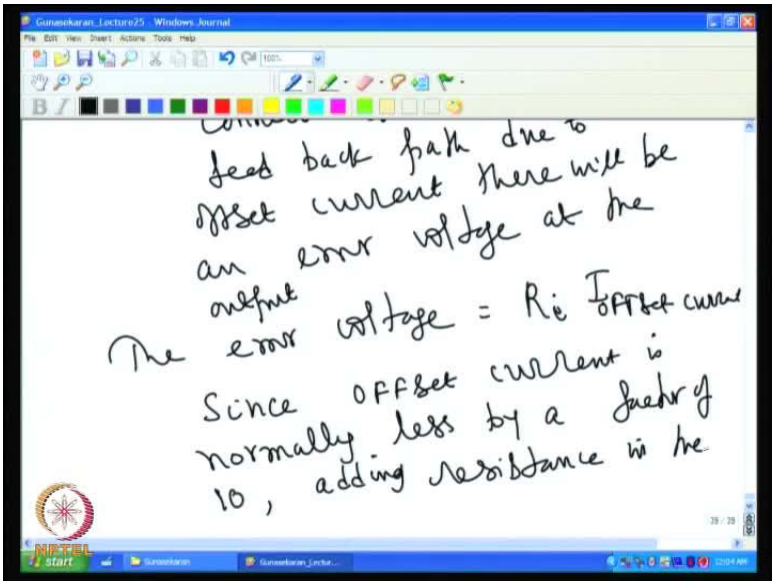

Even if the offset current of two resistances is equal, we will also have error. If we manage to connect R_i exactly in the feedback path due to offset current, there will be an error voltage at the output. In that case, the error voltage would be R_i into I offset. Offset current would be 1 all less than offset bias current. Since offset current is normally less by an order of by a factor of 10, adding a resistance in the feedback path reduces the error. This offset current is a serious issue in the very large.

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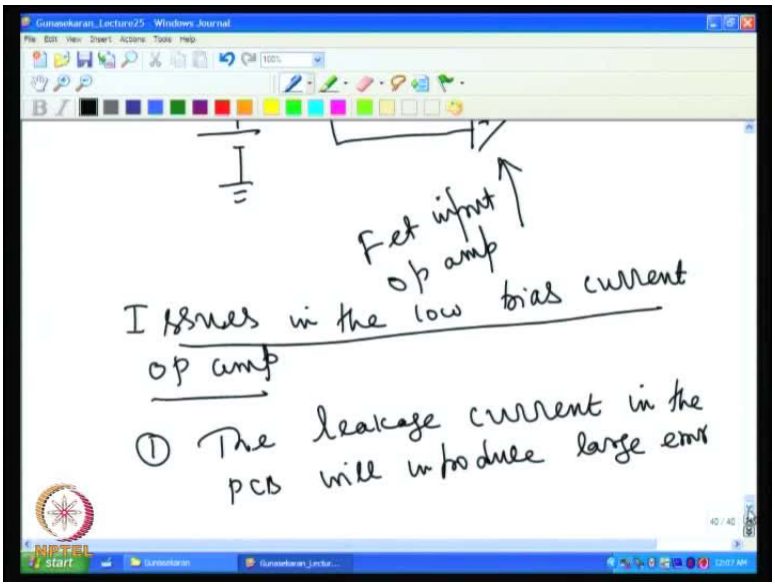

So for example, for the ph probe amplifier to work properly, the R ph choice will be -- you have a resistance connectivity here, which is about 100 mega ohm, and then select fet input op amp that makes the output error very small. For example, if you use 7 4 1 for this application, you will get a tremendous amount of error due to offset current. And then also, with temperature, offset current will change. They will have a large temperature drift. That is why, one have to worry about different types of op amps. This is like fet input op amp, low bias current, that is, basically low bias current op amp, and then low offset voltage drift op amp. That is why we have very many different types. Other we will list at the end.

Now we are discussing about the error drift, the offset current. Since we are at it, we also have to worry when you are selecting a low bias current op amp, when you making a printed circuit board layout. One has to be careful about other current that is getting in to the PCB, which is the much serious problem than this offset current itself. Let us see what is the care that we have to take when we are dealing with this low bias current op amp, issues in the low bias current op amp. The leakage current in the PCB will introduce large error. This one had to be aware of it.

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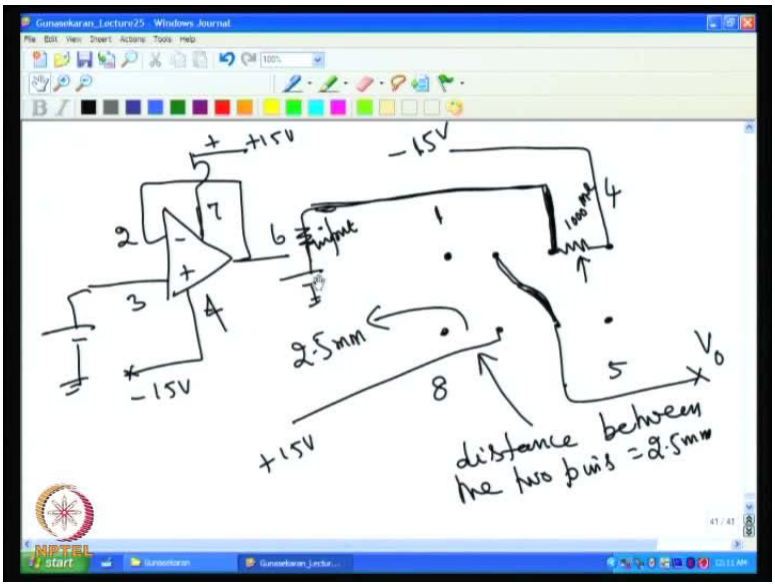

Now I can show you an example here. For example, if I take normal door in line package op amp, you will have the arrangement like this. That is, the op amp will look like this, that is, pin number… If you see, for example, we have this and we have two power supply terminals – plus and minus, and then this is input, this is output. So this is minus 15 volt, this is plus 15 volt, for example, if you take this pin number 3 and this is pin number 2 and this is 6, this is pin number 4 and this is 7. This is the typical configure most of that dual in line package op amp.

Now, physically they look like this. You have 8 pins -- 1 2 3 4, and then in another line, you have this 8 pins. So, if I take the pin numbers, assume this is 1 and then this is 4, and then you have 5 and then 8. This is pin number 8. That is you have here is pin number 1 and then assume this is pin number 8, that dual in line package, and the distance between this two pins is 2.5 mm.

The distance between the two pins hence is equal to 2.5 mm. Now, if you see this one – we would have connected this actually, this distance between these two is 2.5 mm. If you connect the circuit in reality, we will connect this one to minus 15 volt and then 5 6 7 will be connected to plus 15 volt. So we will take a layout and then I will connect this one to plus 15, then this is 2, and the 2 and 6 are to be shorted. So, I will connect 2 and 6 like this. Then, I have to connect pin number 3 as a input, so I will take pin number 3 and connect this out at the layout, we will make the PCB layout, so it has (( )) (40:15) thickness so this is input voltage... This is connected to the high resistance. This has very high resistance, that is, 100 mega ohm.

Now, in this case, this will be taken as output. This is made in a printed circuit board and we said the distance between these two is 2.5 mm. Even, if it is a printed circuit board, you will have some amount of resistance across this, it is not defiantly infinity. For example, if it is a circuit board then assume that this resistance, that is present between this and this, is thousand mega ohm. This is thousand mega ohm. This minus fifteen volt goes through this thousand mega ohm, and it actually goes like this, goes to the ground and completes the path.

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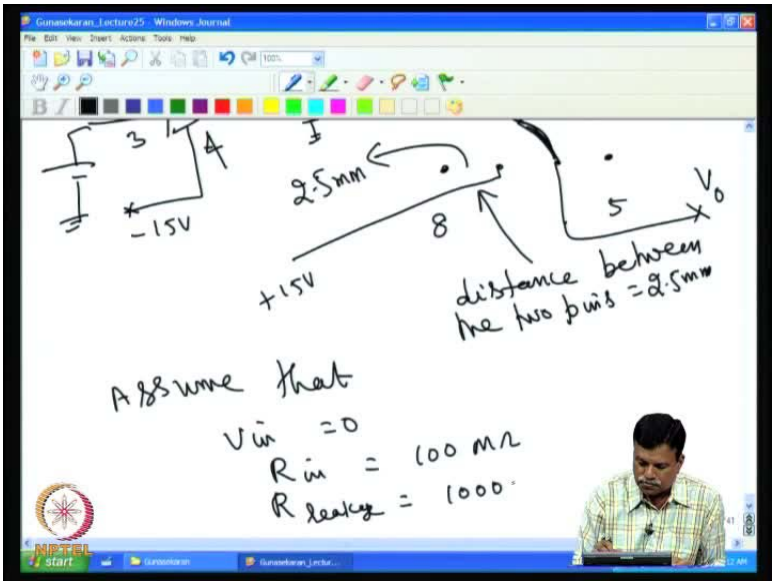

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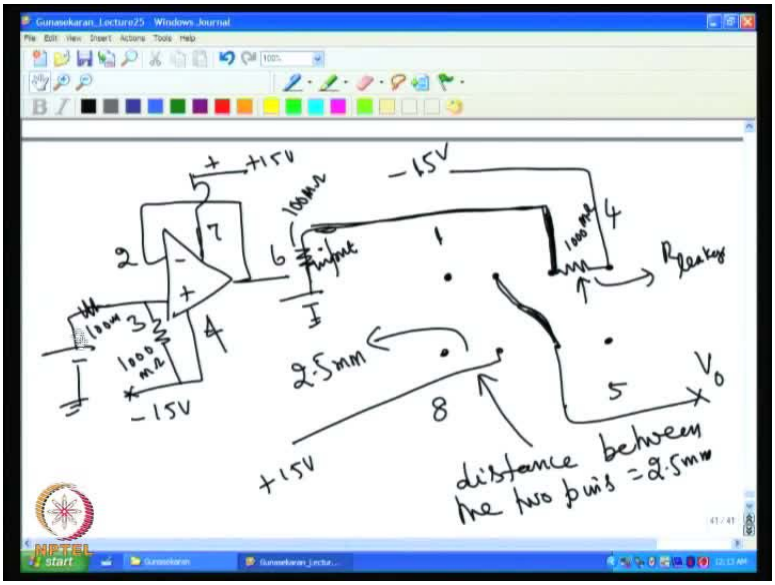

What really happens is minus 15 volt passes through this and that current produce a voltage across this. Assume that ph probe voltage is 0. Assume that v input is equal to 0, R integral is equal to 100 mega ohm, R leakage this is leakage resistance. R leakage is the 1000 mega ohm. That means, minus 15 volt is now divided between this 1000 mega ohm and 100 mega ohm because this is 100 mega ohm. The integral resistance is there and there. Assume there is no voltage. Since there is no voltage here, we expect 0 volt at the output, that is, if this is 0 then this is having 100 mega ohm, this 1000 mega ohm. If I draw the equivalent circuit, that is actually here.

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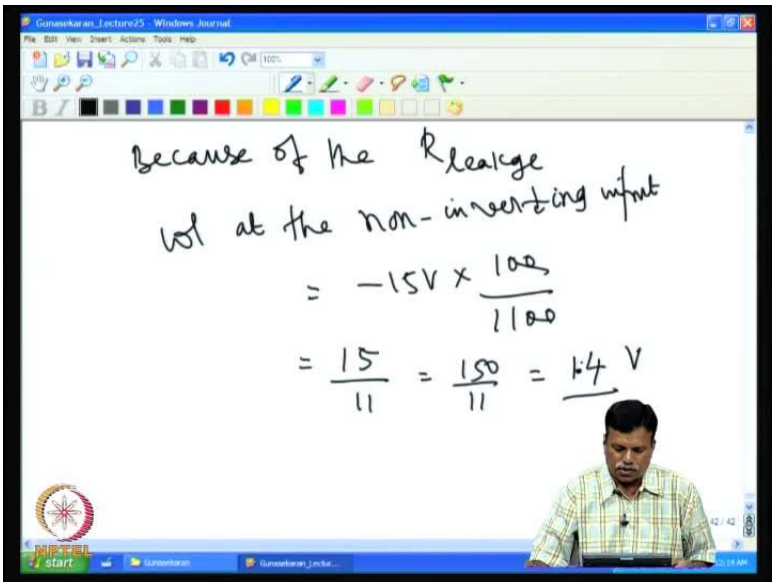

You get this minus 15 volt applied to the plus input through this 1000 mega ohm, and then it is divided between this 1000 mega ohm and 100 mega ohm. So, because of this leakage resistance because of the R leakage voltage at the non-inverting input, the voltage at the plus input terminal would be minus 15 into 100 mega ohm divided by 100. This is, 1100 mega ohm because we have 100 mega ohm and 100 mega ohm are in series.

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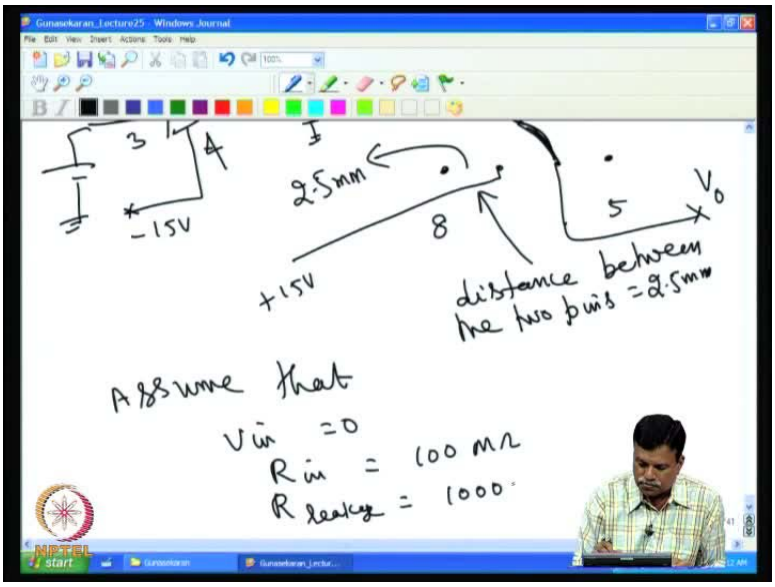

You get this? That actually comes to be 15 hole divided by almost by a factor of…, because this 1 by 11 so there you will have 1.4 volt nearly. Roughly 1.4 volt error voltage appears at the input due to the leakage resistance. This is a series problem I in variances circuit because we are now dealing with very high impedance, which is comparable with the PCB resistance.

If I want use this, then high impedance circuits with high resistances will be used, so that the voltage of less and the bias current effect is also less. Then, I have to go for some technique to remove this power supply leakage voltage that is coming because of the limited impedance of the PCB material.

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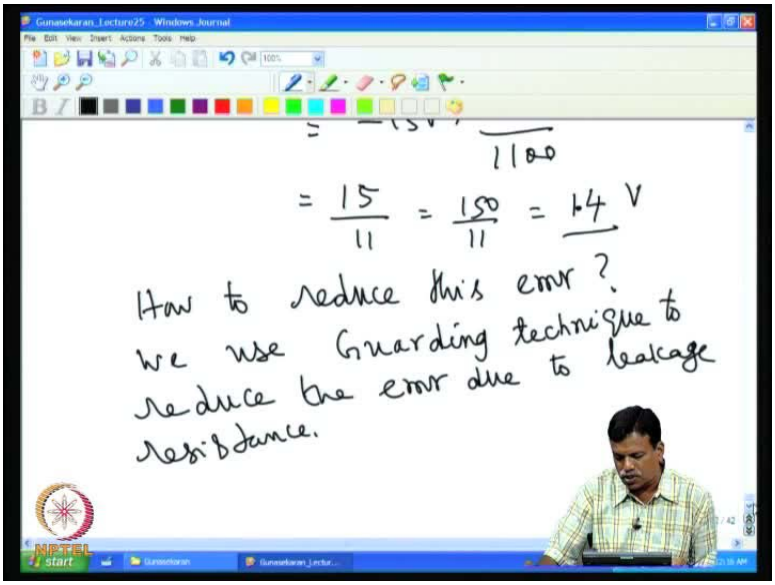

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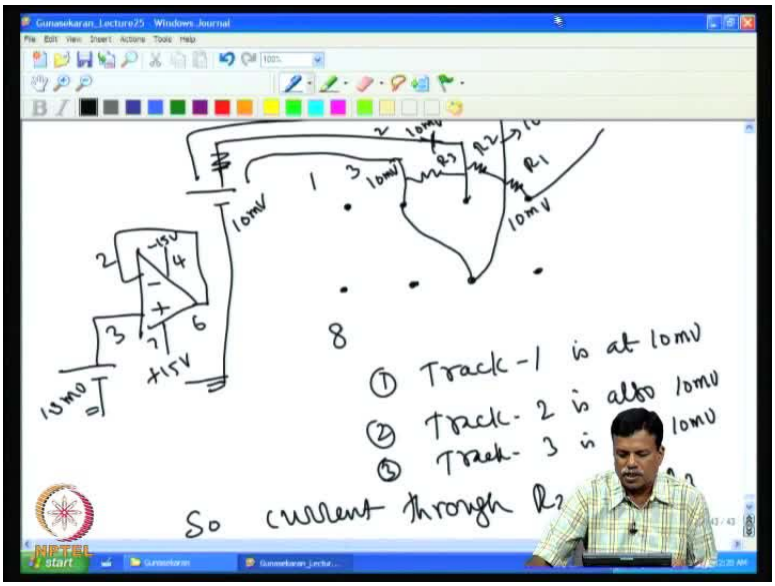

Now that is how to reduce this error? This is where the guarding technique comes into picture. We use guarding technique to reduce the error due to leakage resistance. What is that is done in the guarding technique. So, circuit looks like this. We take, for example, both the layout part and the circuit part. We have this eight pin AC, that is, pin number 1 and that is pin number 8, and what we want is this.

What you can do is the circuit calculation. This is will be same -- 1 and the 6. So, 1 and 6 are joined. Then 3 is a input, so take 3, apply in the input it as large resistance here. Then, at this point, I take the pin circuit board and extend it like this. Similarly, this part also I take and extend it like this. This terminal, which is the input terminal, is called at both end sides, and one this and this are actually not connected anywhere. Here or here, it is just extended like this. Now, this makes this error leakage between this and this. It is not at all issue because of now what happens is we have this spilt and see we have now leakage resistance between this and this. So, I call this as R 1, this is R 2, and this is R 3. But then, we know that output voltage is same as input voltage. For example, if this is 10 milli volt, then I know that this also 10 milli volt, and then the output voltage is also 10 milli volt, so this also 10 milli volt sitting. You have named it as 1 2 3, so the track number 1 is also 10 milli volt, and track number 2 is also 10 milli volt, track number 3 also 10 milli volt. So, track 1, 2, 3, all, are at same volt.

Since all are 10 volt, so current through R_1, current through R_2, and R_3 are 0. This resistance has no affect. Now, if you see R_1, this is connected to minus 15 volt supply. This is pin number 4, which is op amp supply, which is minus; this is 2, this is 3, this is 6 and then 4 and this is 7. It is minus 15 volt this is plus 15 volt. The pin number 4 is at minus 15 volt.

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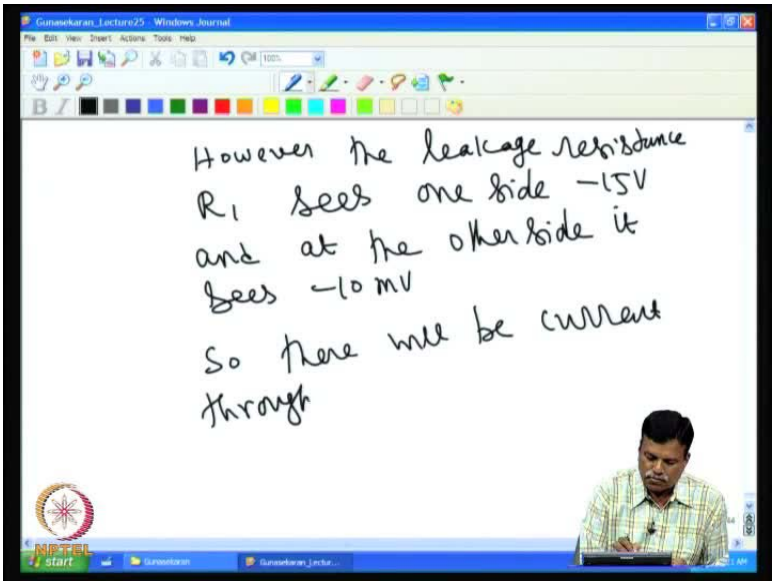

So current through R_1 is possible. Now, this is at 10 milli volt, output is at 10 milli volt. We assume, here is 10 milli volt, so the output is 10 milli volt, and this is minus 15 volt, so there will be a current through the R_1. The leakage resistance R_1 will current.

The leakage resistance R_1 sees one side at minus 15 volt and at the other side minus 10 milli volt, so there will be a current through R_1. However, this current will not produce any error at the output. There will be current through R_1 and that current actually flows through the output terminal.

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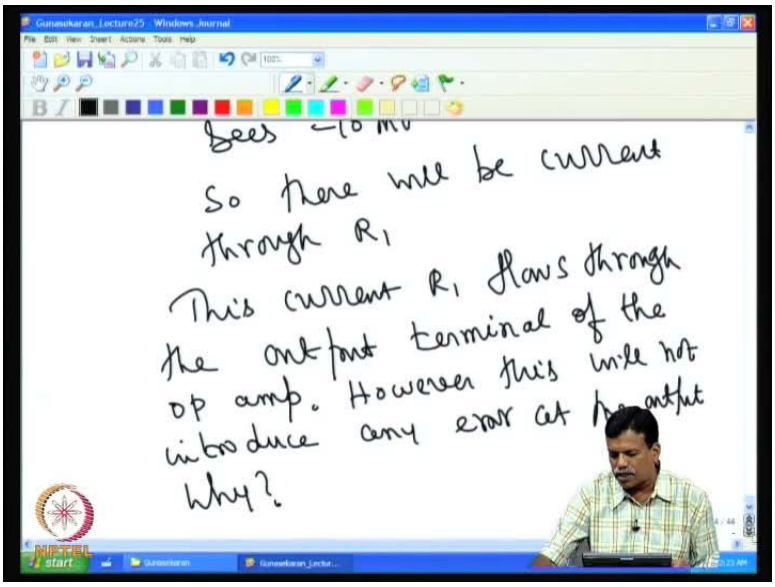

If u see this -- this current minus current take -- this current actually flows through R_1 and goes like this but will not produce error at the output because the output invariance is 0. So eventually, we say the current flows through R_1, flows through the output terminal of the op amp.

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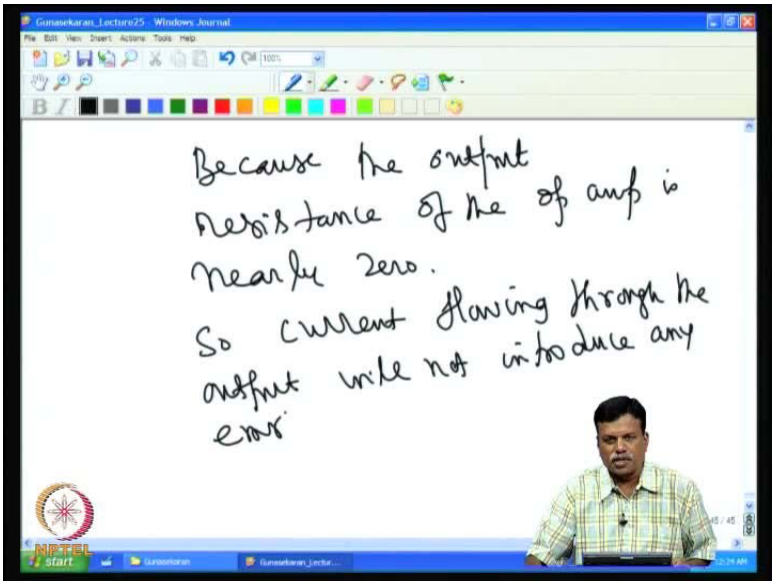

However, this will not introduce any error at the output. But the question is why it will not reduce any error? The answer is because the output terminals of op amp is almost close to 0, so current flowing through the output will not introduce any error. so (( )) the output (( )) is resistance is 0 .

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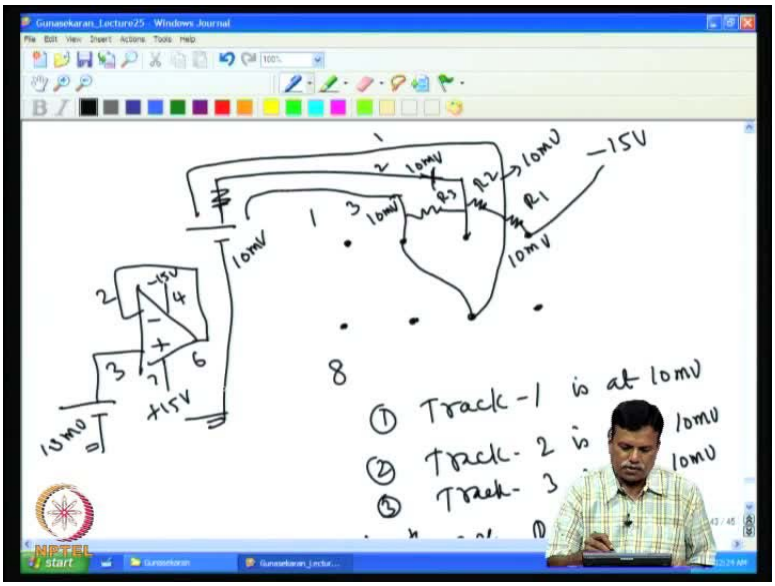

The current flowing through this will not introduce any error. So, this system works well. We may wonder that what happens if I connect 1 resistance between 2 and 6 because in this case, we are directly shorted this resistance. Instead of that, if I connect resistance between 2 and 6, for example, here I add a resistance then what happens? I will show in the separate figure to avoid confusion. Here, we add an introduce resistance in the feedback which is equivalent to input resistance to reduce the bias current error.

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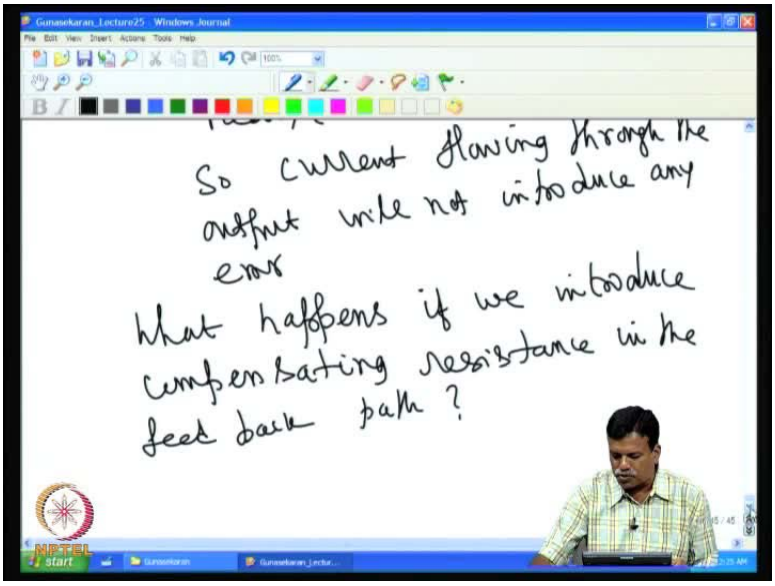

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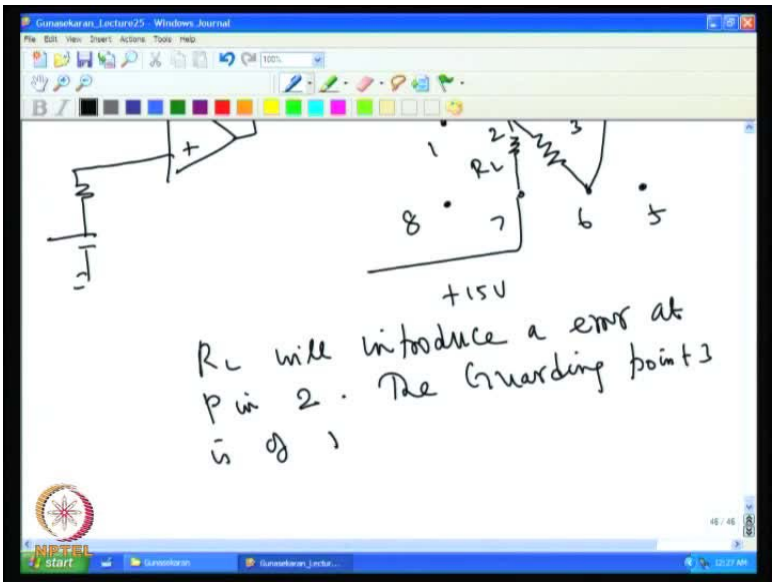

What happens if we introduce compensating resistance in the feedback path? Actually that is a serious problem here because if I put the resistance, then it looks like this. That is, you have op amp, I introduce resistance here, which is equivalent to input impedance.

Now, if I look at that in the layout path, then as you said, we will have pin number 2 and 6 shorting it, I have to put resistance. Now, the different distance between these two is only 7.5 mm, even if I manage to put resistance 2 to 6… then 6. (( )) This is to be connected here. Then, I will be following this. That is guarding technique I will be using. I will be using here between this two, guarding technique, and this is connected to minus 15 volt, this is connected to plus 15 volt; this is pin number 2, this is pin number 1, this is 3 4 5 6 7 8.

Since this is very high resistance, the leakage resistance between this and this will produce the voltage at 2. This is R leakage R_L. I will introduce error at pin number 2 and the guarding point has no use. The guarding point 3 is of no use. So, one has to be careful when you are using registers in the feedback path to reduce the offset current because, as we have shown here, using a guarding technique reduces the error due to the leakage and so on. But if we are using a resistance in the feed feedback path, then guarding technique also will not work. So, one has to aware of this.

The bias current or the offset current or the offset current drift is a major source of worry for a circuit designer, particularly, if you are dealing with DC voltage. If your input

signal is having a very high input resistance, then also the bias current is a serious problem and one had to be careful in a selecting in the op amp for the particular application. That is why we have op amp, which is called fet input op amp, which has a very low bias current. Similarly, we have op amp, which has a very low offset voltage drift. We will see more about these issues in the later classes. Thank you.