Physics of Nanoscale Devices
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Lecture - 56
Strain Engineering, Thermoelectric Effects

Hello everyone. Today we will continue our discussion on strain engineering or quantum confinement we will build from quantum confinement and study the strain engineering in silicon. And we will also start a new topic the topic on Thermoelectric Effects in Devices.

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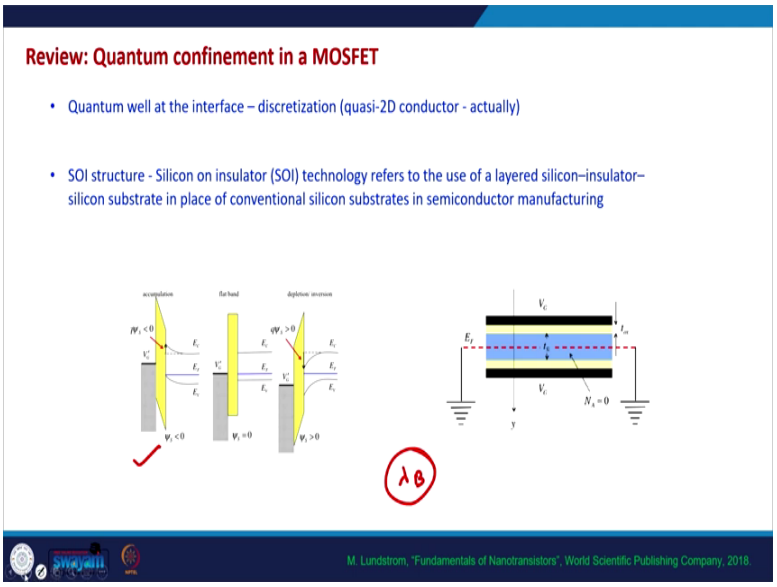

So, what we have been seeing is that even in bulk MOSFET there is a confinement of electrons in the inversion layer and in ETSOI structure this confinement is there because of the geometry of the devices. So, that is why we need to consider and this these, all both of these confinements are of the order of the de Broglie wavelength of electrons.

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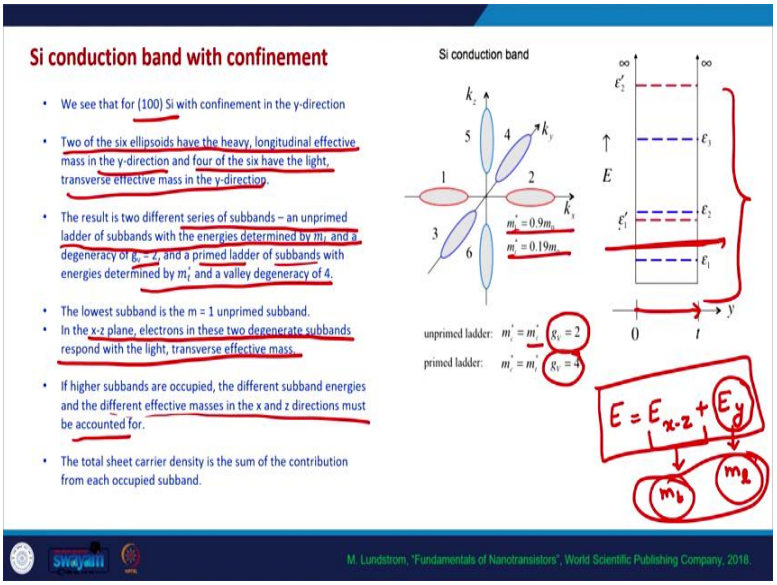

So, in both the cases we need to consider the quantum mechanical nature of this confinement. So, if we take a 100 silicon wafer by 100 silicon wafer we mean that the surface of the wafer is in this plane actually.

So, this is the plane at which this crystal has been sort of sliced and for this the two of the six ellipsoids in ISO energy surfaces in constant energy surfaces. Two of the six ellipsoids have the heavy, longitudinal effective mass in y direction and 4 of the 6 have light, transverse effective mass, that we have seen as well that.

Now, we get two kind of electrons heavy electrons and light electrons. The heavy electrons have a degeneracy of 2 and the light electrons have degeneracy of 4. The result is a two different series of subbands an unprimed ladder of subbands with energies determined by the longitudinal effective mass with degeneracy 2.

And a primed ladder of subbands with energies determined by the transverse effective mass. So, this we have also seen in our previous discussion. So, generally we assume that the lowest subband which is the unprimed subband.

If we assume that, if that is filled in that case we need to take along y direction we need to take the mass to be longitudinal effective mass, and in x z plane the electrons risk have the transverse effective mass. So, in order to calculate the total energy of electrons, we need to calculate the x the energy in x z plane and energy in y direction.

So, what it means is that this energy in y direction is discrete energy and in order to calculate this energy we need the longitudinal effective mass, but the electronic mass in x z plane is the transverse effective mass.

So, this is a subtle point in this in understanding this and in calculating various energies or in calculating the total energy of electrons in silicon, ok. So, please keep this in mind and if higher subbands are occupied, the different subband energies and the different effective masses in x and z directions must be taken they must be taken into account properly.

So, like this lowest subband in which the longitudinal effective mass will be the effective mass in y direction and the effective mass in x and z direction will be the transverse effective mass. Like this we need to consider the masses in all the subbands, ok. So, that is how we can account for the quantum confinement in MOSFETs both in inversion layer and both and in ETSOI structures as well, ok.

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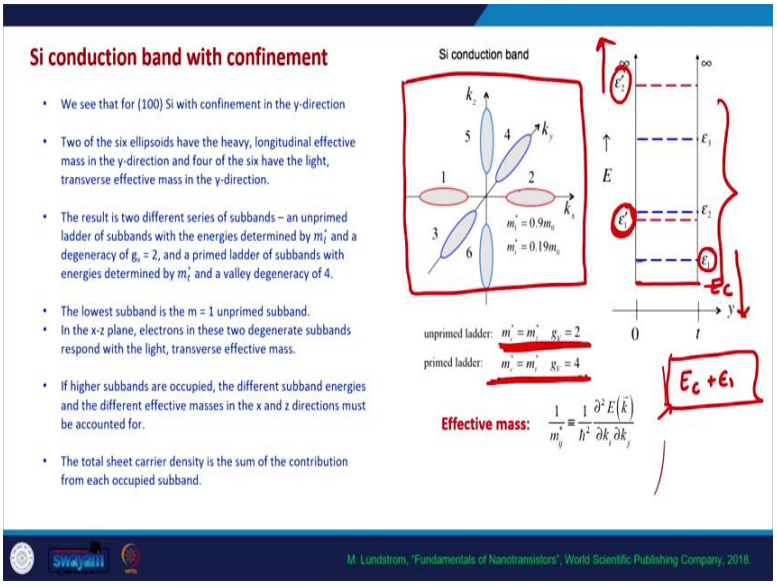

So, the all almost all the MOSFET theory will be the same. Here instead of E_C. So, this is the bottom of the conduction band instead of E_C we need to consider E_C + €1.

If we are considering just the first subband, ok. So, all those calculations will be modified in this way. The number of channels in the MOSFET the density of states all these things will be modified in this way.

So, since we have already done a discussion on the subbands and here the only novel point is that now there are two kind of subbands with different degeneracy's one is the subband with heavy electrons having degeneracy 2 and subband with light electrons having degeneracy 4.

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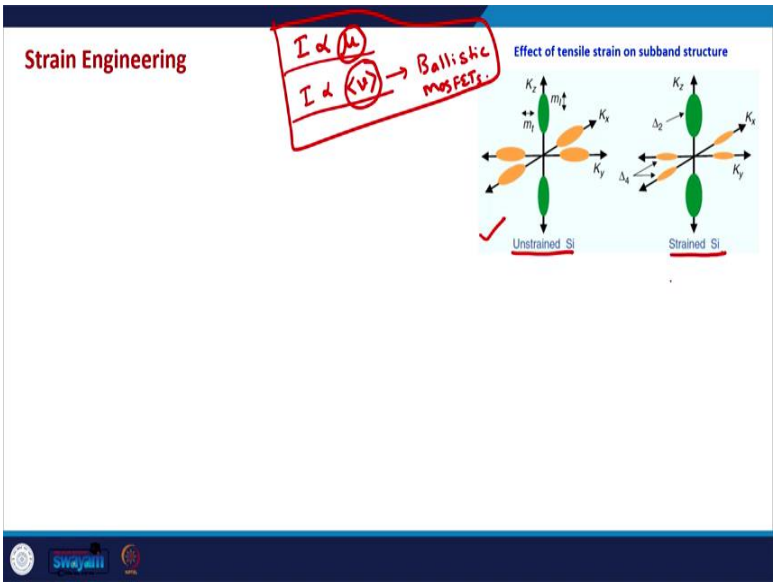

So, with this background let us go to the strain engineering in silicon and the strain engineering essentially means that, the device performance is enhanced by applying an a applying a mechanical strain.

So, generally one of the ways in which electron performance is increased is by scaling. But, apart from that we can increase the drive current by applying strain as well because, if you recall the drive current is directly proportional to the mobility of electrons in bulk MOSFET and it is directly proportional to the average velocity or injection velocity in the case of ballistic MOSFETs, ok.

So, if we can somehow enhance the mobility or the injection velocity then we can improve the performance of the MOSFETs even by keeping the channel length same. So, this is a picture in which we apply a biaxial strain on silicon and this is the constant energy surfaces in conduction band for the unstrained silicon and these are the constant energy surfaces in the case of strained silicon.

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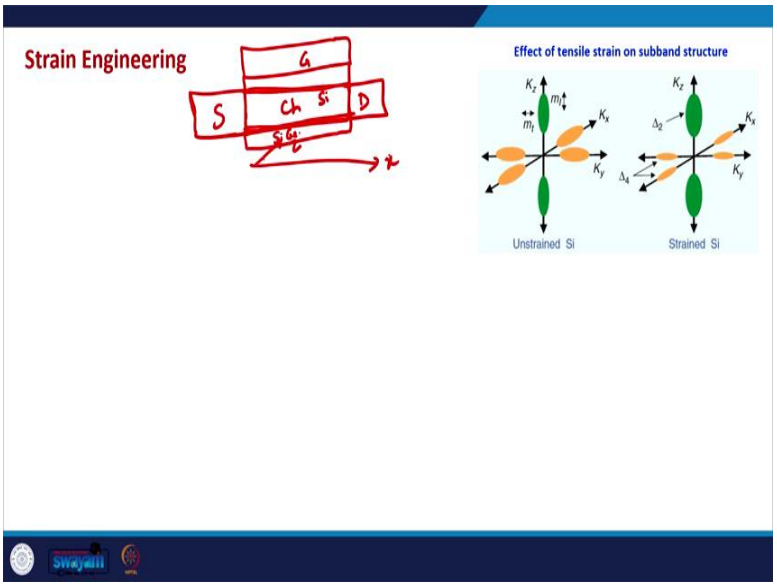

Please remember that the direction in which the stress is applied or the strain is applied is extremely important and this is the case of biaxial strain. What it means is, that if this is our MOSFET let us say this is the source, this is the channel, this is the drain.

Let us say this is DG ETSOI MOSFET or let us not consider DG ETSOI because, things will be complicated in that case. This is just SG ETSOI MOSFET single gate is there. So, we have silicon and silicon might be the silicon layer is generally very thin.

So, what we do is that we put a small layer of silicon germanium. So, essentially this channel silicon material is grown on the substrate of silicon germanium layer. And there is a difference in lattice constants of silicon and silicon germanium.

So, what it does is and so what it does is that at the interface or in a thin or up to a distance in silicon. The lattice constant of silicon is modified according to the lattice constant of silicon germanium. Generally the lattice constant of silicon germanium is greater than that of silicon.

So, what it does is that it essentially applies a tensile strain in x direction as well as in z direction and that is why it is known as the biaxial strain. So, this kind of strain in which we have a silicon germanium substrate and on top of that we are growing the channel silicon, that essentially pulls the silicon lattice both in x direction and in z direction. And in that case this is how the these, constant energy surfaces of the silicon are modified.

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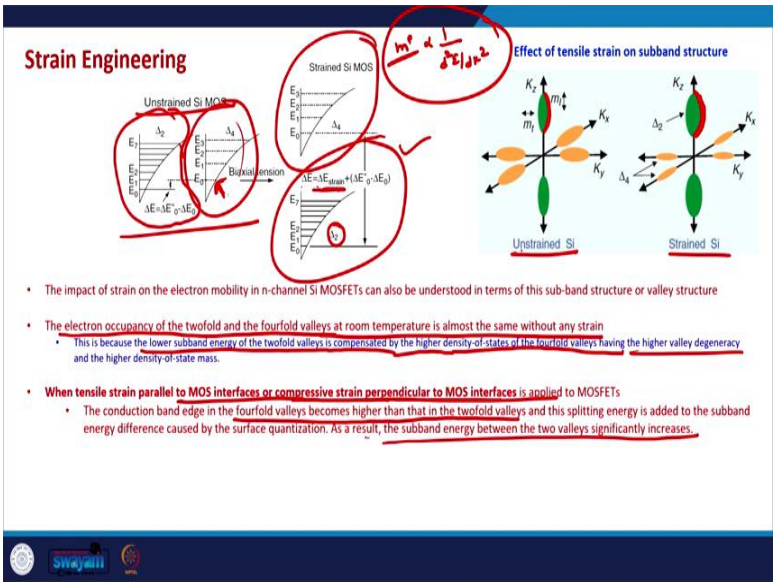

So, let us try to understand it in a more physical way. So, this is the unstrained silicon and in unstrained silicon MOSFET as we have already seen because of the quantum confinement there is energy splitting.

So, now, this is these Δ2 are the two heavy electron valleys and Δ4 are four light electron valleys. So, these are these Δ2 corresponds to if you we go back to the previous slide Δ2 corresponds to the unprimed energy levels. So, two of the valleys these are like 2 valleys in the E k diagram of the silicon. So, these two valleys correspond to the unprimed ladder or correspond to the longitudinal effective mass and rest 4 valleys correspond to the transverse effective mass.

So, because of the quantum confinement there is a difference in energy between these two between these or this degeneracy is lifted, as we have also seen here. As we have seen that the energy of the 2 valleys is now less and the energies of the rest of the 4 valleys is more and that is shown here in this way.

If you remember these are the various this is the quantum well structure in the bulk silicon and the electronic energy levels in these 2 valleys will be given by these are the unprimed energy levels and in 4 valleys these are the these, are like the primed energy levels. And as you can see, there is a difference between the ground state energy of these two valleys and this difference is there because of the quantum confinement in y direction.

In bulk silicon generally it is not there this difference is not there, but because of the confinement this degeneracy is lifted in at the interfaces at in the inversion layer of the MOSFET or in the ETSOI MOSFET.

Now because of the strain what happens is that there is a, this energy difference between these 4 valleys and 2 valleys is further increased. So now, the energy of these 4 valleys is even more than the or even larger than the energy of the 2 valleys.

So, what it means is that because of the biaxial strain, if we go back to our previous diagram again. What it does is, that these €1, €2, €3 these unprimed energies are have, they go down and these primed energies go up.

So, the degeneracy is further lifted in a way or now the energy difference is even more between the two kind of electrons relatively, we cannot say for sure which energy goes down, which energy goes up. It is a relative difference between the these two kind of valleys that is increased.

So, in unstrained silicon all the six valleys are very close to each other in strained silicon 4 valleys are way above than these two valleys. In unstrained silicon now as you can see that the electrons can jump from these primed energy levels to unprimed energy levels as well because, they are quite intermixed with each other.

So, that is one thing that happens when the strain is applied that is this energy difference between the two kind of valleys is increased. This term valley comes from the E k diagram and these 6 lobs.

These 6 ellipsoids in constant energy surfaces these correspond to 6 valleys and because of the quantum confinement 2 valleys have heavy electrons and 4 valleys have light electrons and that is why the degeneracy was lifted.

But now, because of the stress as well the degeneracy is further lifted 4 valleys are even higher in energy levels in energy values as compared to the 2 valleys now, ok. This is one thing that happens. Second is so these are the ellipsoids after the strain is applied on silicon. These are the.

So, in this figure particularly the strain has been applied in x and y direction and z is the direction of the confinement. In our previous analysis, we have taken the y direction to

be the direction of confinement and x and z direction to be the direction in which the strain is applied. So, please so what we can do is we can modify K y and this can be K x, K z.

So, because of the biaxial strain, what now happens is even these ellipsoids are modified as you can see. And in these two valleys, in this direction of confinement along the y direction if you closely have a look the curvature in this direction was less now the curvature is more.

This is unstrained and this is strained. So, even in the two valleys the mass the since the curvature is now increased and mass is inversely proportional to the curvature. So, mass is reduced even in these two valleys.

So, two things happen because of the strain, one is the effective mass of electrons in $\Delta 2$ valleys in these two valleys is decreased because, the curvature is increased so the effective mass is decreased.

Second is, the energy difference between the valleys is increased. These four valleys are now far apart, these two kind of valleys are now far apart. These four valleys and two valleys are now very far apart from each other. Two things happen one is the effective masses are modified in all the valleys in fact. And second is even this delta E strain is introduced in this energy splitting. So, because of these two things what happens is generally without strain in unstrained silicon.

The electron occupancy of the twofold and the fourfold valleys at room temperature is almost the same. So, even there is a difference in energy levels, even though there is a difference in these energy levels in unstrained silicon the electron occupancy at room temperature is almost the same.

And the reason for that is that the lower subband energy of the two fold valleys is compensated by the higher density of states of the fourfold valleys having the higher value degeneracy.

So, the electron occupancy in unstrained silicon in both kind of valleys is almost the same actually; and the reason for that is that the density of states is higher in higher

energy levels. So, that is why and moreover the valley degeneracy is more here so, but the energy levels are small here. So, these two effects are counterbalanced, ok.

But, when the tensile strain parallel to the MOS interface is applied or per or compressive strain perpendicular to the MOS interface. So, if we apply this tensile strain in x and z direction or compressive strain in y direction. The conduction band edge in fourfold valleys become higher, so this happens. As a result the subband energy between the two valleys between the two kind of valleys increases this energy difference between the two valleys actually increase.

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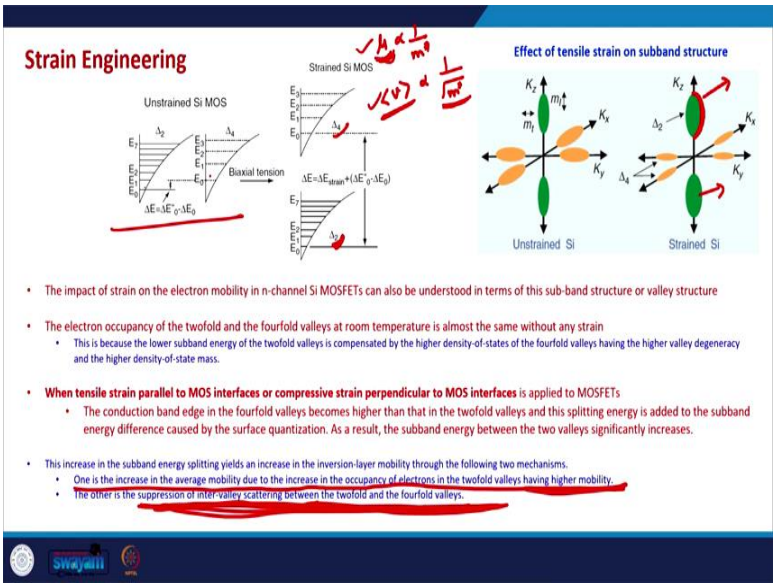

So, that leads to increase in the mobility or injection velocity of electrons in the channel and there are two reasons. One is the increase in the average mobility is due to the increase in the occupancy of electrons in the two fold valleys with higher mobility.

So now, as we just saw that the effective mass of the electrons is reduced and mobility is inversely proportional to the effective mass, moreover the injection velocity is also proportional to the effective mass. So, if this is reduced m star is reduced, the injection velocity in ballistic MOSFETs or the mobility in bulk MOSFETs will be increased.

So, one thing is that. Second is, the suppression of inter valley scattering between the two fold and the fourfold valleys. Now, since there is a big energy difference between the two fold and the fourfold valleys, now the inter valley scattering is reduced.

In unstrained silicon what happens is that, there is a huge there is a significant interaction between the twofold valleys and fourfold valleys electrons and this electron interaction is mediated by the phonons.

And that is why because of this scattering the mobility or injection velocity is suppressed. Now since, the energy difference between the fourfold and the two fold valleys is more this inter valley scattering is suppressed and that is why the injection velocity of the electrons is now more or the mobility of the electrons is more.

So, there are two reasons that a tensile strain in x z direction works. One is the electrons in the two fold valleys now have higher mobility because of the reduced effective mass. And second is, the separation of the inter valley scattering between the two fold and the fourfold valleys. And by doing this we can achieve higher mobility and higher injection velocity in the MOSFET.

But if we apply the other kind of strain, if we for example, apply compressive strain in x z direction in that case reverse might also happen. So, this strain engineering needs to be done very carefully, we first need to understand what kind of strain produces enhancement in mobility along the channel direction along the direction of electron movement and what kind of strain produce suppression of mobility, ok.

Essentially two takeaways are there one is because of the strain effective mass effective masses are modified, second is inter valley scatterings are reduced and because of these two things the injection velocity and the mobilities are increased. So, please keep these things in mind these are certain points although I would recommend all of you to go back and read some good papers on strain engineering, then things will be more clear.

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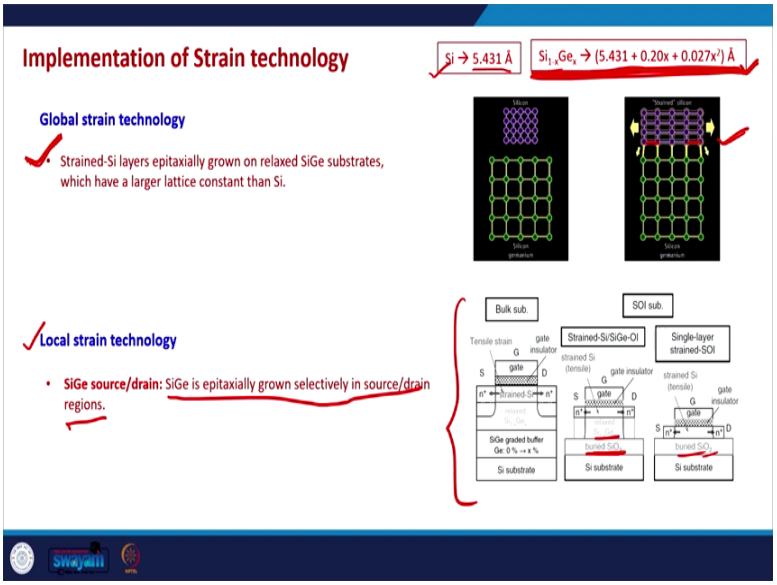

So, this is the way this strain technology is implemented. Generally as I already pointed out to you in order to make a silicon channel or make a strained silicon channel in order to make a MOSFET channel in which silicon lattice is strained in a specific direction.

What we do is? We grow silicon on the substrate of silicon germanium and the lattice constant of the silicon is 5.43 angstroms. The lattice constant of silicon germanium is given by this relationship.

So, depending on the amount of germanium in silicon germanium lattice, the lattice constant can be determined from this formula. So, as is clear as the germanium content increase increases in silicon germanium the lattice constant increases.

So, if we grow a silicon lattice on top of silicon germanium substrate this is how it looks like, this is a qualitative picture of the silicon grown on silicon germanium substrate. And now as you can see that in one direction or in a certain direction the bond lengths the lattice constant is modified.

And this modification in lattice constant actually modifies the band structure as well, that also modifies the E k relationship and that actually gives rise to these kind of valleys in strain silicon, ok.

So, generally the strain technology is broadly categorized as global strain technology in which all the channel is, all the channel silicon is strained and that is done by growing

one of the one of the most prominent techniques is by growing the channel silicon on silicon germanium.

So, as you can see here in the bulk MOSFET this channel silicon is grown on relaxed silicon germanium and in ETSOI in SOI MOSFETs similarly we have a very thin layer of silicon that is grown on silicon germanium.

And below that is buried oxide similarly here. Yeah. So, that is known as the global strain tech strain technology. Local strain technology is that silicon germanium is epitaxially grown in the source and drain regions.

So, that it selectively or it locally modifies the lattice of the silicon in channel just close to the source and drain contacts. In this case the entire channel the silicon lattice constant in the entire channel will be modified in this case the silicon lattice will be modified only locally.

And these are complex actually physically these are complex things. In order to properly understand physics we need to do first principal calculations or do experimental measurements on what happens when a particular kind of strain is applied.

So, here we have seen just a glimpse of strain technology I would recommend that with this background. Please go back and read some recent papers on strain technology that will give you the, that will sort of let you appreciate the beauty of this kind of technique in nano MOSFETs.

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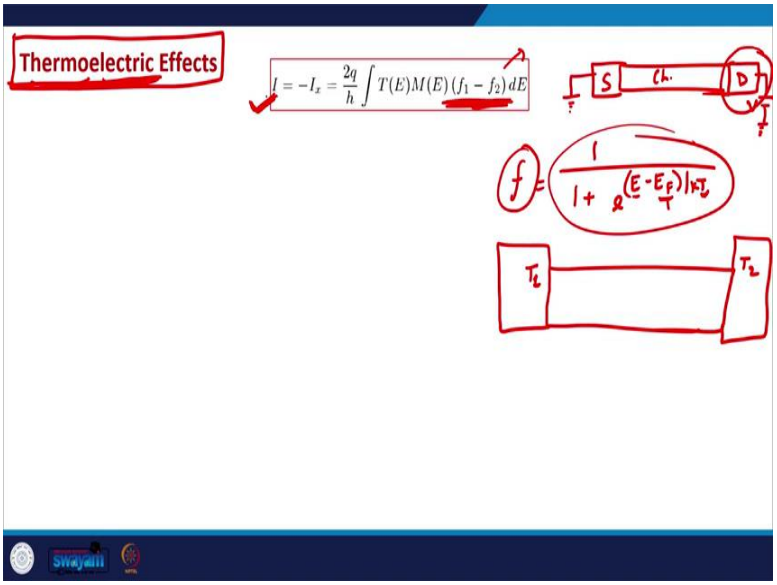

So, with this we conclude the strain technology and now, let us come to a new topic the topic on thermoelectric effects. And what are what is what do we mean by thermoelectric effects?

As the name suggests thermoelectric means, something to do with thermal energy as well as electrical energy and thermoelectric effects in specially in electronics and electrical engineering means the conversion of temperature difference in a voltage or vice versa essentially or conversion of heat energy in electrical energy and vice versa ok; and as all of us are aware that in devices heat dissipation is one of the main challenges especially in integrated circuits.

So, it is quite important to understand how heat impacts the electronic circuits ok. And that is what we will try to see here and we will start we start with our basic equation of current that we derived using the general model of transport.

This is a pretty I would say this is a pretty general expression for the current and in if you recall the derivation there we assume that a voltage is we assume that there is we have a two terminal device, a device with source and drain and one of the terminals is grounded and we apply voltage on the second terminal.

And because of this voltage difference the Fermi levels are modified and because of the modification in Fermi levels, now source contact is trying to put electrons in the channel and drain contact is trying to take electrons out of the channel.

So, during that derivation we just assume that that there is a flow of electrons from the source side to the channel and there is a flow from drain side to the channel, ok. Apart from that we did not had any specific I would say any specific assumption in this derivation.

So, this is a pretty general expression for the current and what it means is if we try to look at it closely the current depends on the difference of the Fermi levels on the two sides of the conductor essentially.

So, if there is a difference in Fermi levels, whatever be the cause of difference there would be a current in the conductor. And if you remember the expression of the Fermi function, this is how the Fermi function looks like kT. So, the Fermi function depends on the electronic energy, it depends on the Fermi level, it also depends on the temperature.

And by applying a voltage, what we do is we modify the Fermi level on one side of the conductor and that is how the Fermi level is or the Fermi function is also modified on this side of the conductor. And that is why this term becomes non zero and there is a non zero current in the conductor.

But, if you have a close look on the Fermi function expression, the Fermi function also depends on the temperature and if we have a conductor and if we put the conductor let us say on left side it is at temperature T1 on the right side it is at temperature T2.

Because of the temperature difference, the Fermi functions will be different on each side of the conductor or in other words, if we have a bulk contact on the left side which is at temperature T1 and on the right side the temperature T2.

Although the Fermi levels might be the same because, the Fermi level may not change, but because of the temperature difference the Fermi functions will be different on two terminals. And in that case at certain energy levels this $f_1 - f_2$ may be non zero and the current might flow in the conductor.

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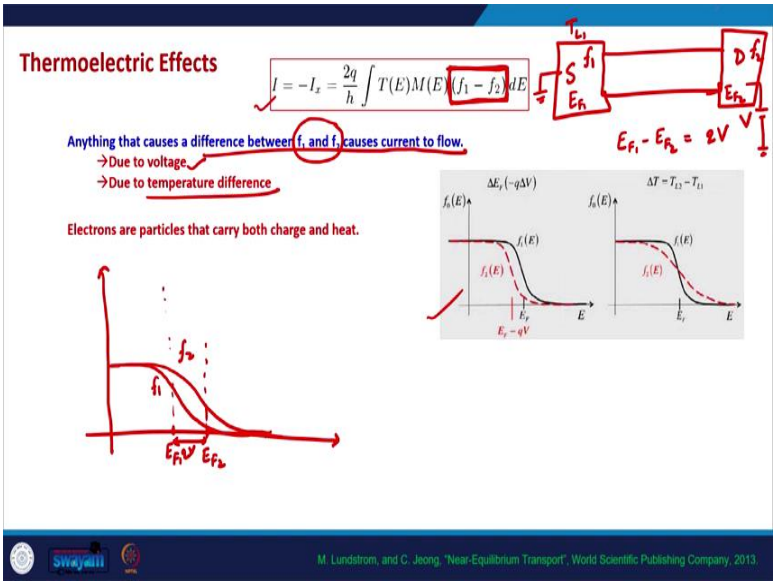

So, that is essentially the I would say the key point here. That the key point is whenever there is a difference in Fermi functions across the two terminals of a conductor then, it will have a flow of electrons.

And that flow of electrons will give current to us. So, anything that causes a difference in f_1 and f_2 can cause a current to flow and f_1 and f_2 can be different because of the voltage difference and because also of the temperature difference, ok.

So, with this let us quickly have a look how f_1 and f_2 or how the Fermi function depends on voltage and how it depends on temperature. So, this is a plot let me just for the sake of better understanding, let me draw it here as well.

If we have a two terminal device and this is source this is drain, the source Fermi function is f_1 the drain Fermi function is f_2. And if we apply a voltage on the drain side ground the source side the drain Fermi level will be so, if the Fermi level here is E_{F1} the Fermi level here is EF_2. E_{F1} - E_{F2} will be two times V.

So, which means E_{F2} will be lesser thane f_1. So, E_{F1} will be here E_{F2} will be here and this differences dependent on the voltage. So, f_1 will be a curve around E_{F1}, it will be something like this and f_2 will be around f_2. So, it will be something like this. So, this will be f_2 this will be f_1.

And because of the difference between f_1 and f_2 now there will be a non zero current in the conductor. Similarly, now let us say if we have on the left side the temperature is T_{L1}

which means the lattice temperature T_L means lattice temperature on right side we have T_{L2}.

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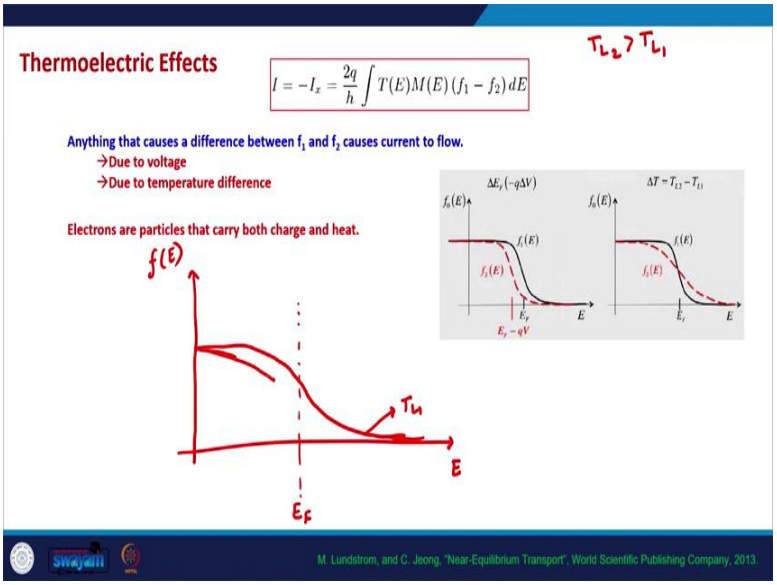

The way the Fermi functions will be modified is, the Fermi level would not change in this case. So, the Fermi level will be the same we are plotting Fermi function as a function of energy and at temperature T_{L1} let us say the this is how the Fermi function will look like. So, this is T_{L1}, ok. If T_{L2} is more let us say T_{L2} is greater than T_{L1} in that case this Fermi function will be even more broaden.

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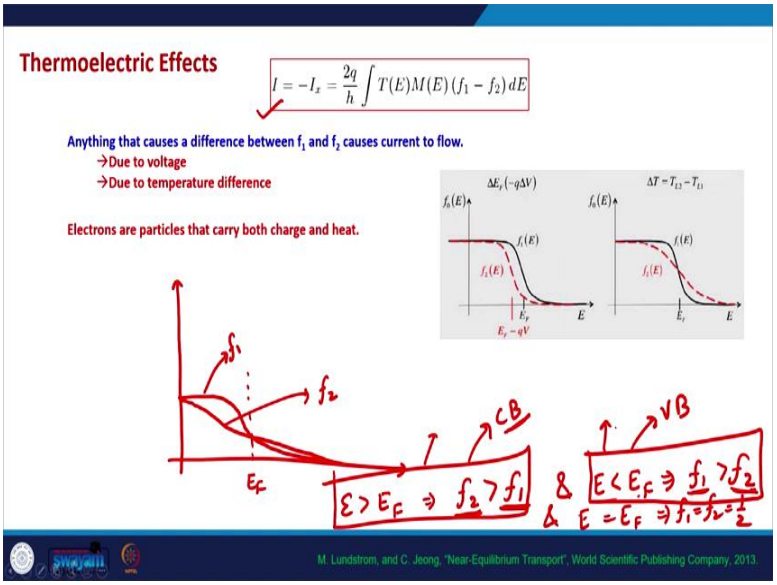

Let me redraw it this is the let us say the Fermi level at Fermi level, the Fermi function is always 1 by 2. So, that is what we will do and if the temperature is increased this is how it looks like. So, what happens is that this is f_1 which means, Fermi function at T_{L1} and this is f_2 the Fermi function at T_{L2}. So, for energy is greater than E_F above Fermi level f_2 will be greater than f_1.

And below Fermi level, f_1 will be greater than f_2 also at Fermi level both of them will be same, ok. Now the temperature difference is creating a new kind of difference in the Fermi functions.

Above Fermi level, the Fermi function of right contact is larger than the Fermi function of the left contact and below Fermi level the Fermi function of the left contact is larger than the Fermi function of the right contact, if the right contact is put at the put at higher temperature.

So, if the channel material is n type material in which the conduction happens above Fermi level in the energy levels above Fermi level, in that case there will be a net flow of electrons because of the difference in the f_1 and f_2.

If the channel is p type in that case the conduction will happen in the energy levels below Fermi level in the conduction band basically. So, that will be because of this difference, in conduction band this is in the valence band.

So, the electron current will be there because of a temperature gradient, in conduction band it will be there because of f_2 larger than f_1 and in valence band it will be the current will be there because, f_1 is greater than f_2.

So, if we have the channel material to be n type in which the valence band is almost full, conduction band only the conduction band conducts in that case there will be a net current or if we have p type there will also be a net current. In intrinsic carrier there would not be a net current because, the flow of electrons in the flow of volts will neutralize each other, ok.

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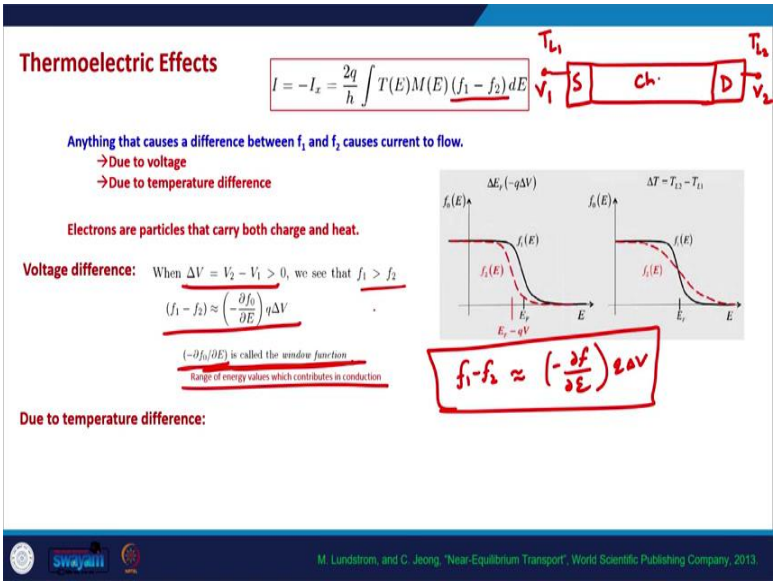

So, because of the voltage difference ΔV, so let us draw this conductor again we have a source, we have a drain, we have a channel and let us say this is on V_1 voltage this is on V_2 voltage. This is on T_{L1} temperature this is on T_{L2} temperature. So, if V_2 is greater than V_1 in that case f_1 is greater than f_2.

And if you remember in near equilibrium transport f_1 - f_2 is equal to (-δf/δE) times q times ΔV. This is the near equilibrium transport in which the voltage difference is small ok and in near equilibrium transport instead of f_1 - f_2 we just put (-δf/δE) times q times V_0.

And this minus (-δf/δE) is known as the Fermi window function ok, just to quickly review and this also gives us the range of energy values which contributes in current conduction actually. So, that is why it is so, the current conduction happens just in the just in a certain window of energy values that is given by the Fermi window function.

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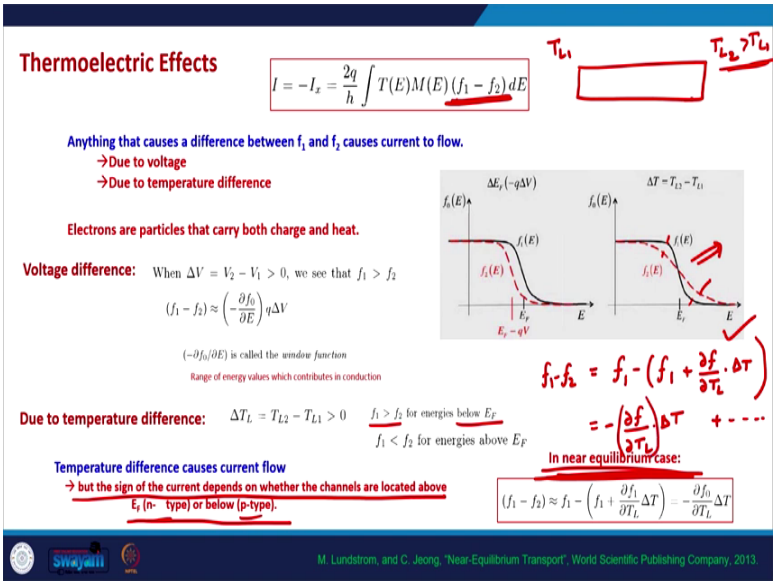

Now, because of the temperature difference, now ΔT_L is $T_{L2} - T_{L1}$. So, here we have T_{L2} we have T_{L1}; f_1 is greater than f_2 below E_F, f_2 is greater than f_1 above E_F. So, as I just told you that depending on if the channel is n type the what happens is in n type channel conduction happens because of the electrons in conduction band.

So, we will see it again when we come to this idea in the next class. So, we will see again, but just to briefly tell you about it the conduction the sign of the current depends on whether this channel are n type or p type basically, which is clear from this difference as well.

So, this is a small I would say a small homework for you, what would be the direction of current in an n type material when T_{L2} is greater than T_{L1} and what would be the direction of current in a p type material when T_{L2} is greater than T_{L1}.

So, just go back and try to see the directions just from this plot of Fermi function. Let us do a bit of bit of maths here in the case of temperature difference let us see the conductor is the two points of conductor are at different temperatures in that case.

In near equilibrium case, which means that the temperature grade temperature difference is not so much it is not too much actually, temperature difference is very small in that case this forcing function in the current f_1 - f_2 can be written as f_1 as it is f_2 can be approximated by the Taylor series expansion around f_1.

So, this can be $\delta f/\delta T_L$ times ΔT, ΔT is T_{L2} - T_{L1} and higher order terms can be ignored because this ΔT is small. So, higher order terms will have ΔT^2, ΔT^3. So, those can be ignored if ΔT is a small number.

So, with this it can be written as $-\delta f/\delta T_L$. Where δf is assumed to be δf_1 because, that is we are expanding f_2 around f_1 ok. Now, what is $\delta f/\delta T$? Let us try to see that.

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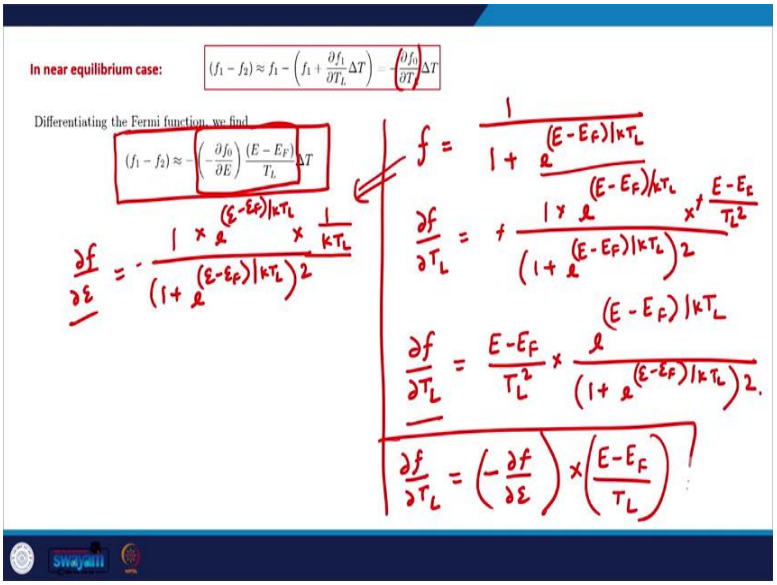

So, $\delta f/\delta T$ is essentially this number, but how do we get this number, $\delta f/\delta T$ is actually this particular number. So, let us quickly try to do this maths f is $1/[1+\exp(E-E_F/kT)]$. What is $\delta f/\delta T$?

So, if this is T_L, $\delta f/\delta T_L$ would be $-1/1/[1+\exp(E-E_F/kT_L)]^2$ times this. So, the derivative of this will be $\exp(E-E_F/kT_L)$ time's derivative of this it will be $-(E-E_F/T_L^2)$.

So, this minus go away. So, we will have $(E-E_F/T_L^2)$ times $\exp(E-E_F/kT_L)$ divided by $[1+\exp(E-E_F/kT_L)]^2$.

So, this is $\delta f/\delta T_L$ ok and from this expression on the Fermi function what is $\delta f/\delta E$, it is $-1/[1+\exp(E-E_F/kT_L)]^2$ times $\exp(E-E_F/kT_L)$ times $1/kT_L$. So, if we compare this and this what we can do is, we can write del f by del T_L is equal to $-\delta f/\delta E$ times $(E-E_F/T_L)$, ok. So, this is what we obtain.

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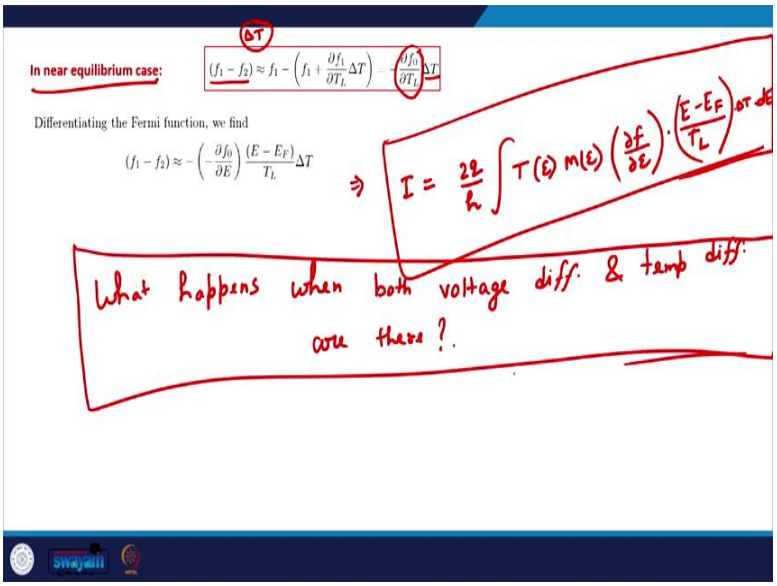

And that is why this in near equilibrium case in which ΔT is a small number in that case f_1 - f_2 can be written as -δf/δT_L times ΔT and which can further be written as minus.

So, this δf/δT is -δf/δE into (E -E_F)/T_L times ΔT. So, which means that now the current because of the temperature difference will be 2q/h if we just to quickly show you we just need to put f_1 - f_2 here 2q/h ∫T(E) M(E) (f_1 - f_2).

So, the current because of the temperature difference will be 2q/h ∫T(E) M(E) (δf/δE) [(E -E_F)/T_L] ΔT dE and so, this will be the current when no external voltage is applied just temperature difference is there.

The left contact is on T_{L1} temperature, the right contact is on T_{L2} temperature. We already know what will be the, what would be the current when left contact is at voltage V_1 and the right contact is at voltage V_2.

Now, let me give you a small homework here, what happens when both voltage difference and temperature difference are there, what happens? So, please work out the maths of current in the case when there is a voltage difference across the conductor as well as there is a temperature difference.

And that is the key to understand the thermoelectric effects. Just to summarize the thermoelectric effects, thermoelectric effects are the conversion of thermal energy to

electrical energy which means, if there is a difference in temperature across a conductor there will be there might be a current flow through the conductor.

And that is known as the thermoelectric current and vice versa. If there is a current through the conductor there would be a temperature difference across the conductor. So, that is what we are trying to understand and in this case what will happen when both voltage difference and temperature difference are present. So please try this, we will see this in the next class.

Thank you all, see you in the next class.