Physics of Nanoscale Devices
Prof. Vishvendra Singh Poonia
Department of Electronics and Communication Engineering
Indian Institute of Technology, Roorkee

Lecture - 55
ETSOI MOSFETs, Quantum Confinement, Strain Engineering

Hello everyone, today we will discuss many modern concepts in MOSFET theory and one is this idea of ETSOI MOSFETs. We have seen a glimpse of it in our previous class when we discussed the geometric screening in MOSFETs. Second we will discuss in some detail about the quantum confinement in MOSFETs.

And third a modern technique to enhance the performance of devices and that is known as strain engineering which essentially uses strained silicon in channel to have more mobility of electrons. So, that is what we will see and before going into these details let us quickly look have a look at what we have seen so far.

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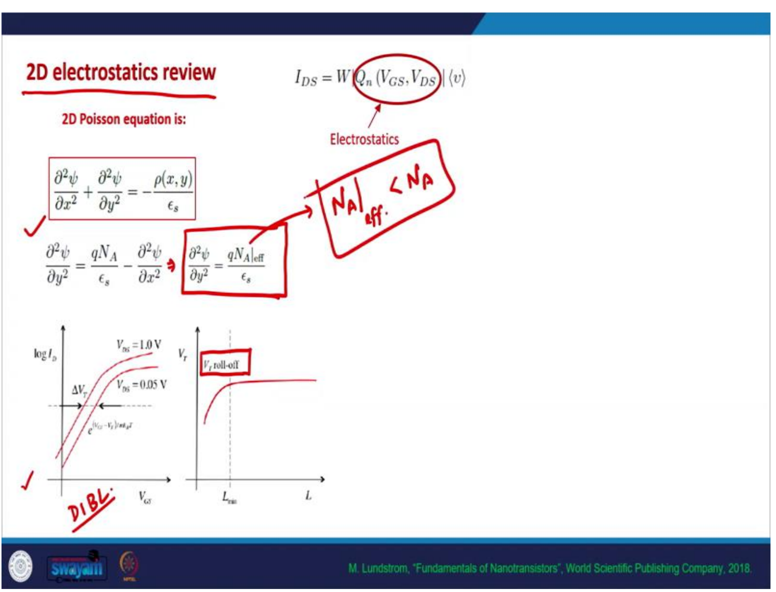

So, what we discussed in our previous class was that for smaller devices for nano MOSFETs we need to consider 2D electrostatics because in addition to the electric field in y direction the electric field in x direction is also prominent. And moreover we observe what is known as DIBL drain induced barrier lowering which essentially means that in nano devices the threshold voltage is decreased as the drain voltage is increased.

Secondly, it has been observed in small channel MOSFETs that the threshold voltage reduces as a function of length.

So, as the channel length reduces the threshold voltage also reduces and this is known as the threshold voltage roll off which means that the threshold voltage goes down below a certain channel length. And in order to account for all these things we need to consider the 2D electrostatics and in 2D electrostatics we take the 2D Poisson equation and we solve this in the channel of the MOSFET.

And what we obtain is that the 2D Poisson equation can be approximated by the 1D Poisson equation. But now the doping in the channel needs to be replaced by effective doping and this effective doping n a effective is less than the actual doping of the channel. So, by considering the 2D electrostatics we can account for all these effects that arise in the small channel MOSFETs.

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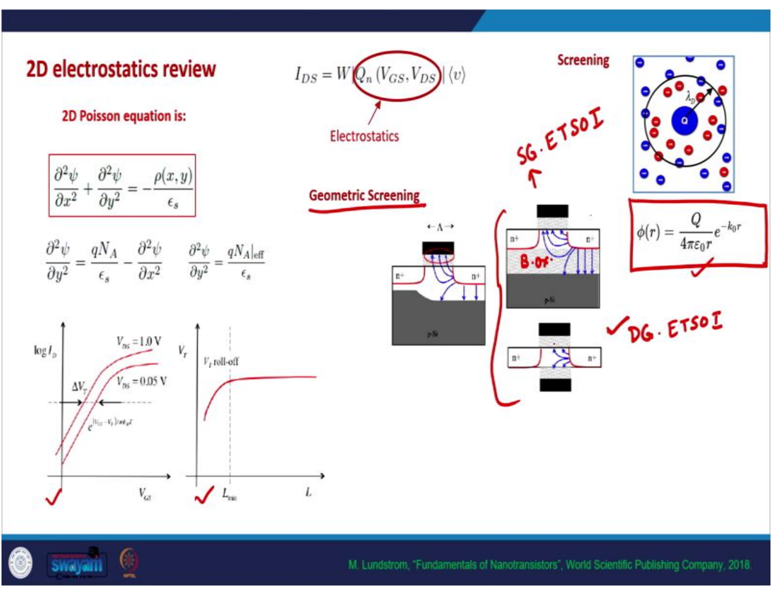

Second in order to mitigate these bad effects or in order to maintain the consistency of our devices we use technique called geometric screening. And geometric screening is another form of screening and the screening in materials with mobile charge carriers is that when a charge perturbation is produced mobile charge carriers rearrange in such a way that after a certain distance the effect of the charge is negligible. And in presence of mobile charge carriers we need to use the screened coulomb potential relationship.

So, that is what the expression for the screen potential screened coulomb potential and the geometric screening. In geometric screening technique what we essentially need to do is we need to neutralize or we need to avoid the drain electric field lines to reach to the source electric field line.

So, we need to stop the drain electric field lines to reach to the source electric field. And in order to do that we need to sort of cover the channel with gate from as maximum number of signs as possible. And that is why these kind of geometries also known as double gate SOI geometries in which instead of bulk silicon we use silicon on insulator which is a silicon on a buried oxide and we can use single gate ETSOI techniques.

We can make single gate ETSOI MOSFET which looks like this SG ETSOI MOSFET and this is DG ETSOI MOSFET. So, generally in ETSOI techniques in SOI techniques there are two broad categorization, one is the PDSOI technique Partially Depleted Silicon On Insulator and second is FDSOI technique which is Fully Depleted Silicon On Insulator. So, as the name suggests in FDSOI the channel is fully depleted and FDSOI is an extremely thin silicon on insulator.

And this is essentially FDSOI MOSFETs this is single gate this is double gate. And as is clear from the figure the geometric length the geometric screening length in DG SOI MOSFET is smaller as compared to the single gate ETSOI MOSFET ok.

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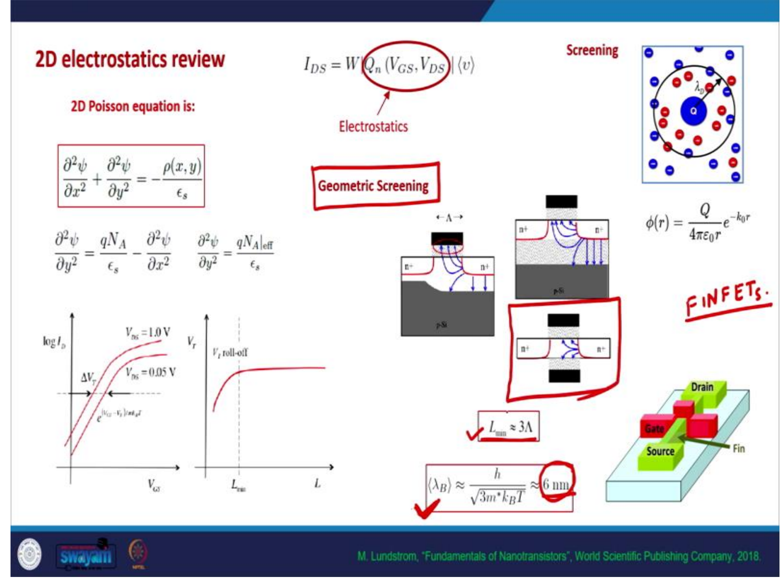

And in this series in order to use geometric screening technique to avoid DIBL and threshold voltage roll off. A normal geometry of MOSFETs was suggested in 19 and late 9; in 1980s 1990s and that was used in making small channel MOSFETs. And this is this is known as FINFETs in which the channel is a vertical channel now and the channel is surrounded by the gate on 3 sides. In some cases in some geometries the channel can be surrounded by the gate from 4 sides as well.

And so, generally what we try to do is we try to make sure that the channel length is at least thrice of the geometric screening length in order to avoid any change, any inconsistency in the threshold voltage arising due to the low channel length. Second, concept that we started was the concept of quantum confinement and by a rough calculation what we calculated was that the De Broglie wavelength of electrons in these materials is around 6 nanometers at room temperature.

So, if the electrons are confined in this kind of dimension. So, if the electrons are there in a material which is 5 to 10 nanometers in that case the material length is of the order of the De Broglie wavelength. And in that case we need to consider the quantum mechanical nature of the electrons. So, this quantum confinement idea this we will see after a bit first let us analyze a little bit of let us do a bit of analysis of the DG SOI MOSFETs.

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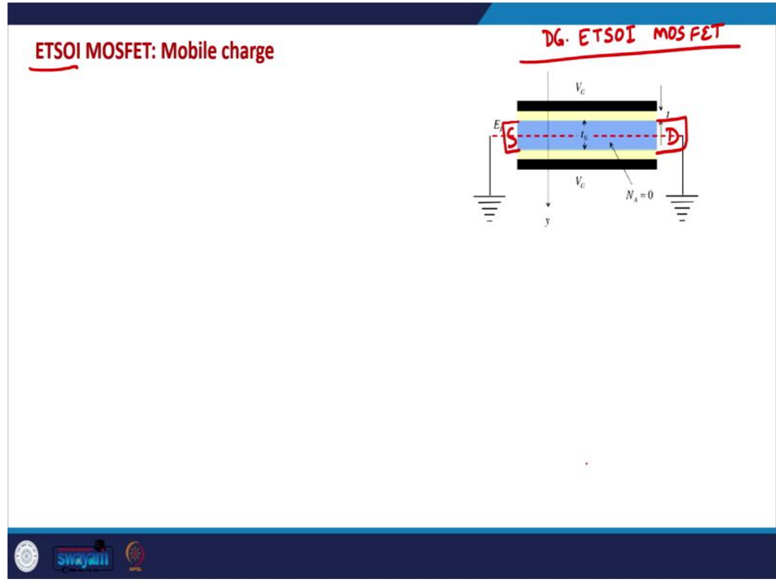

So, DG SOI MOSFET is an ET is comes from the ETSOI technique ETSOI means Extremely Thin Silicon On Insulator. And in this case the MOSFET looks like this the active region of the MOSFET looks like this in which the channel region is an extremely thin silicon on insulator. And on both sides of the channel on the top and the bottom side we have the gate electrodes and on this side we might have we would have source on this side we would have drain ok.

So, this is how; this is how the channel region of the DG SOI MOSFET looks like DG ETSOI MOSFET. In fact, double gate extremely thin silicon on insulator MOSFET. So, this kind of MOSFET offers an advantage of having good very small geometric screening length, so that we can make very small channel lengths. Generally, this kind of; this kind of MOSFETs are used in around 20 nanometer channel length or so ok.

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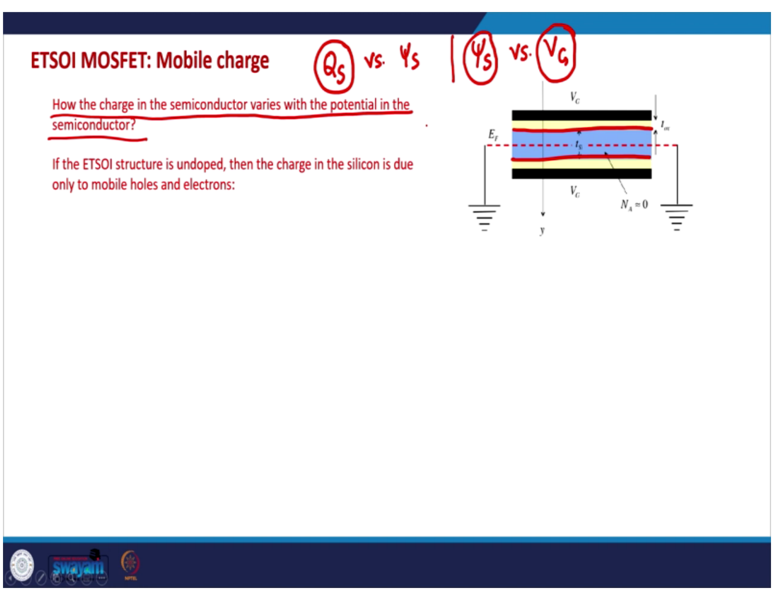

So, in DG in this DG ETSOI MOSFET generally the ETSOI structure is undoped when we use an extremely thin silicon on insulator the E ET SOI structure is undoped. And here now what we will try to do is we will try to understand how the charge in the semiconductor varies with the potential in the semiconductor. So, the kind of analysis that we did for the MOSFET we will try to do that kind of analysis for DG ETSOI MOSFETs what it means we will try to understand Q_S versus Ψ_S.

And finally, we will try to understand Ψ_S versus V_G because V_G is the external voltage that we apply on the MOSFET. Ψ_S is the voltage that appears at the surface of the

semiconductor that appears at the interface of the semiconductor and oxide and Q_S is the charge in the semiconductor ok. And as is visible from this figure there are two gates here and in DG ETSOI MOSFET structures.

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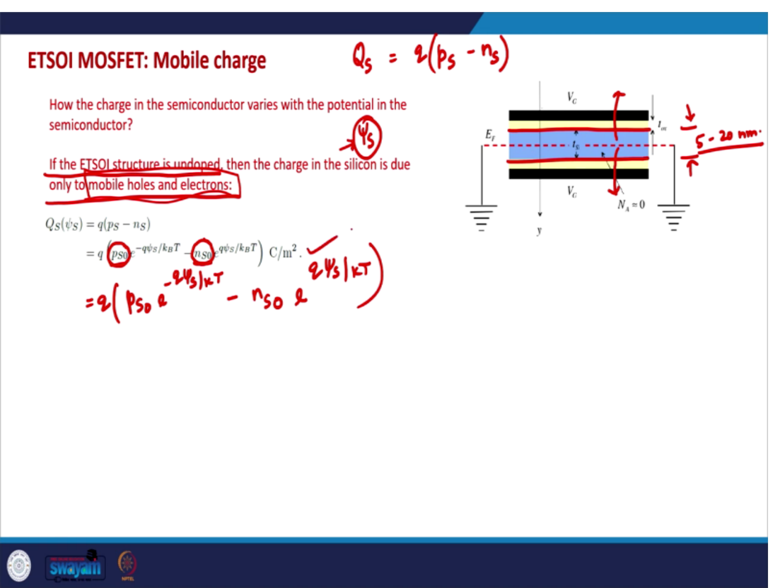

What we can do is or what we can assume is that the charge in the semiconductor or what we can say is that almost half of the charge in the semiconductor is mirrored by the upper gate and half of the charge in the semiconductor is mirrored by the lower gate. Typically, the thickness of this silicon layer is around 5 to 20 nanometers ok.

And so, the total semiconductor charge can be considered to be divided in two components half of the charge is mirrored by the upper gate half of the charge is mirrored by the lower gate. So, in this case if we try to understand what is the total charge in the semiconductor and if this ETSOI structure is undoped in that case that in that case the charge due to depletion depleted.

Since now no dopants are there. So, this depletion charge is extremely low and the only charge that is there is because of the mobile holes and electrons. The depletion charge appears because of the uncompensated dopant atoms and in this case the uncompensated dopant atoms are not there. So, this charge the depletion charges is extremely is negligible I would say is not there and those total semiconductor charge is just because of the mobile holes and electrons it is just because of the holes and electrons.

And so, that is why we can write the total semiconductor charge to be q times number of holes minus number of electrons in the semiconductor. And now the number of holes and electrons in semiconductor are function of the semiconductor potential.

So, if the number of holes without any semiconductor potential is p_{s0} and number of electrons without the semiconductor potential is n_{s0} which means when there is no gate voltage the number of holes in the system is p_{s0}. And when there is no gate voltage the number of electrons is n_{s0}. When we apply a gate voltage and generally the same gate voltage is applied on the on both the gates.

So, both the gates are sort of connected to each other in that case a semiconductor potential psi S appears in the at the interfaces ok. And in that case what happens is that the number of holes and the number of electrons get modified. So, now, with Ψ_S potential if the potential is positive the holes will go down number of electrons will increase.

And if the potential is negative the number of holes will go up and number of electrons will go down this we have also seen in our discussion of the conventional electrostatics of the MOSFETs. So, in presence of a semiconductor potential the total number of holes and electrons are $q[p_{s0}\exp(-q\Psi_S/kT) - n_{s0}\exp(q\Psi_S/kT)]$ ok as is written here ok.

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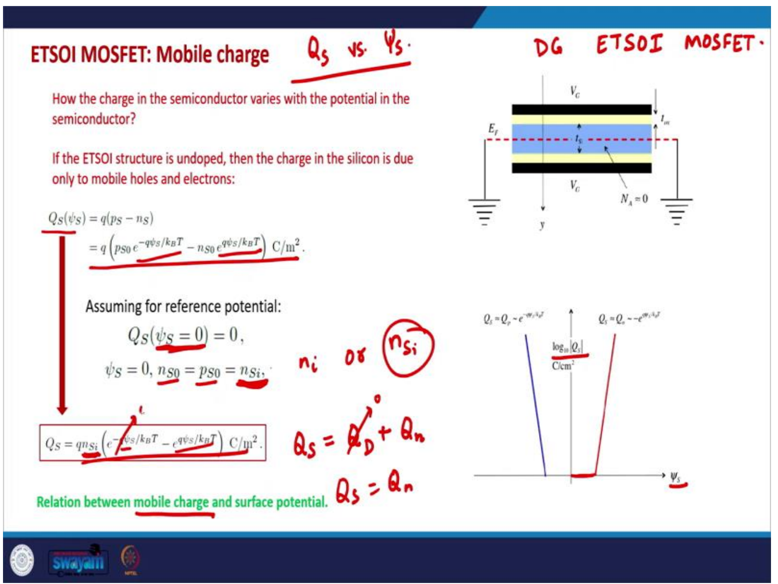

So, now let us assume that when the semiconductor potential is 0 which means we are operating at a reference potential in that case n_{s0} and p_{s0} is equal to the intrinsic carrier concentration of electrons and holes in the silicon, in the semiconductor essentially. So, n_{s0} and p_{s0} will be equal to n_i or $n_{silicon}$ and that is what we will replace in here.

So, this expression of the semiconductor charge becomes q times $n_{silicon}$ intrinsic carrier concentration in the silicon times $\exp(-q\Psi_S/kT)$ - $\exp(+q\Psi_S/kT)$. So, this is the total charge per unit area in the channel in this DG ETSOI MOSFET. So, this is DG ETSOI MOSFET just to sort of emphasize this. And now if we draw a relationship between the mobile charge which is essentially the total semiconductor charge.

So, now the if you recall the total semiconductor charge is the depletion charge plus mobile charge in this case it is not there. Q_S is equal to Q_n and that is equal to this number. And if we plot $\log Q_S$ as a function of Ψ_S which means we want to understand the dependency of the semiconductor charge on the semiconductor surface potential in that case that looks like this. If we plot $\log Q_S$ versus Ψ_S up to a certain Ψ_S these exponential.

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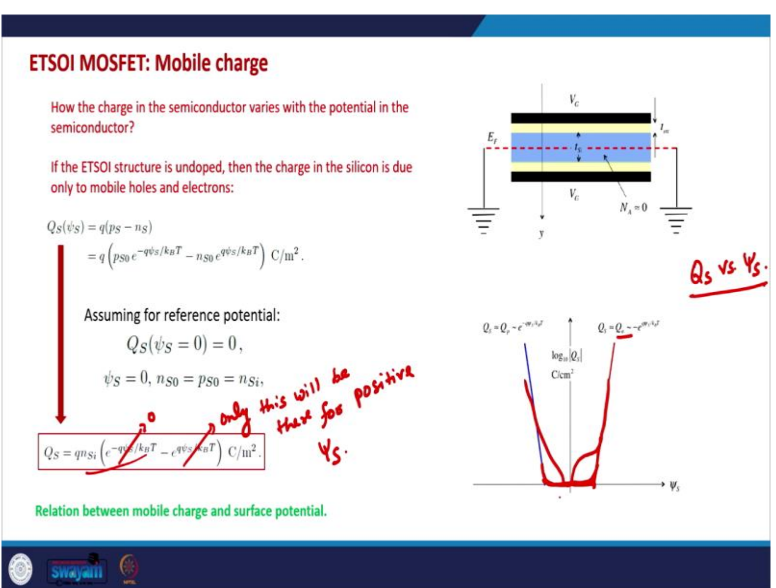

So, for example, if we are looking in the positive Ψ_S regime in that case this will be almost 0 this negative part will be 0. Because it will be a negative exponential and only this will be there only this will be there for positive Ψ_S this will be almost 0 for negative psi for positive Ψ_S.

So, it will be a log of Q_S will be just directly will be proportional to Ψ_S. So, it will be a line after a certain Ψ_S below this Ψ_S generally it is extremely small value. So, it is not shown here, but it should be something like this. Similarly, on the negative side the second term will be 0 and only the first term would be there and it will be almost the same kind of plot.

So, this will be the charge versus semiconductor potential relationship in the case of DG ETSOI MOSFET. So, as if this, so, this is quite close to or if we compare this to the charge versus Q_S versus Ψ_S relationship for the MOSFET in that case in conventional MOSFETs in addition to Q_n we also have Q_d. So, we have this kind of relationship there and this side we have this kind of relationship ok. So, this is somewhat different than the conventional MOSFETs.

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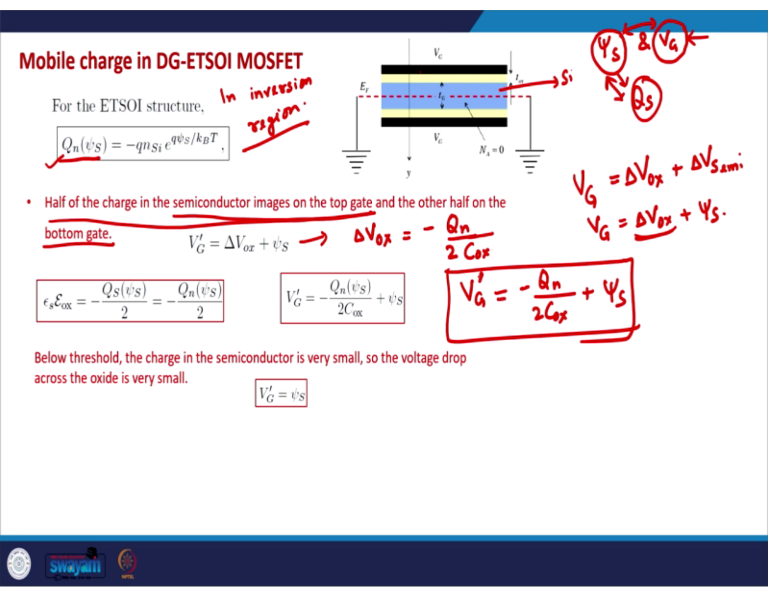

Now, what is the mobile charge sort of in the DG ETSOI MOSFET? The total charge in the semiconductor is just the mobile charge and if we assume in the inversion region in inversion region which means we have applied a positive potential.

And so, N type of channel has been formed in the silicon this has been inverted and now this has become N type in that case this term first term would be 0 and only this term would be left. So, this will be the mobile charge in the DG ETSOI MOSFET and this will be equal to $-qn_{silicon}\exp(q\Psi_S/kT)$.

So, we can what we can assume is now we are trying to find out a relationship between Ψ_S and V_G because as I have already mentioned this we can change V_G externally. So, V_G is in our hands and Ψ_S is the potential that appears on the semiconductor interface and this psi s essentially governs the charge or electrostatics in the MOSFET.

So, in addition to this relationship we would also like to understand this relationship. And whatever mobile charge is there in this DG ETSOI MOSFET we can assume that half of the charge is or semiconductor images half of the charge of the semiconductor is imaged by the top gate and the other half is by the bottom gate.

So, in that case what happens is in that case we can see what is the charge across the these top and bottom oxides essentially. Because if you remember the basic relationship between V_G and Ψ_S, V_G is $\Delta Vox + \Delta V_{semiconductor}$ and $\Delta Vox + \Psi_S$. So, we need to know what is the voltage drop across the oxide and in order to know the voltage drop across the oxide we need to know what is the voltage across the voltage on each sides of the oxide.

So, here if the total charge in the semiconductor is Q_n we can assume that $Q_n/2$ is there for the top gate and $Q_n/2$ is there for the bottom gate. And so, using Gauss's law as we did before, we can find out ΔVox. So, ΔVox is $-Q_n/2Cox$ because $Q_n/2$ is the charge Cox is the capacitance of the oxide on each side.

So, that essentially gives us V_G' is equal to $-Q_n/2Cox + \Psi_S$ ok. And just to sort of remind you this prime is there because we are not writing down flat band voltage here. If we explicitly consider the flat band voltage in that case we can just write V_G there ok. And the most important or one of the most important regions of MOSFET operation is the sub threshold region.

So, below sub threshold even this charge is not significant. As we have also seen in the previous plot in the previous slide this is the threshold I would say the threshold condition below this the charge is also charge is insignificant.

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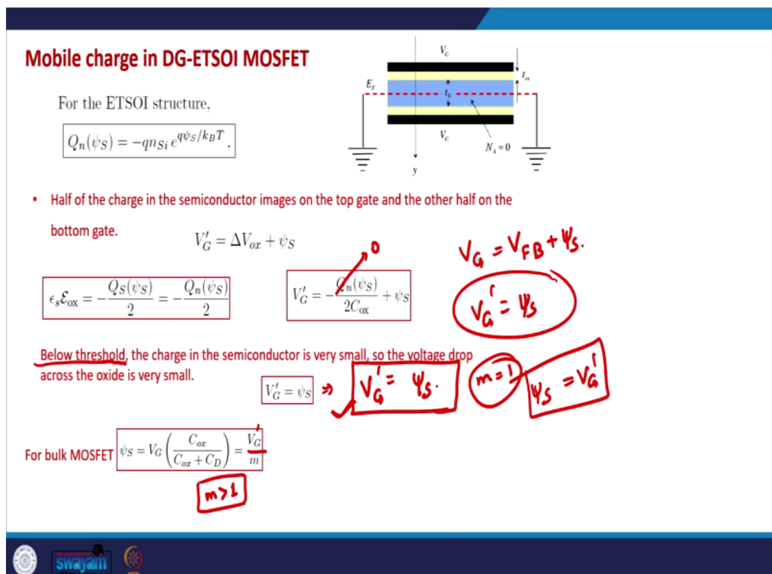

So, below threshold here what happens is even this charge is 0 and what we can say is that V_G' is equal to Ψ_S. So, in DG ETSOI MOSFETs below threshold voltage the semiconductor potential is almost equal to the or is equal to the gate voltage if we are not considering the flat band voltage.

Otherwise, V_G will be V_{FB} + Ψ_S just or V_G' is equal to Ψ_S. And that is an important relationship because in bulk MOSFETs what happens is that Ψ_S is equal to V_G/m or V_G'/m to be more precise. And where m is always greater than 1, we try to minimize; m we try to bring m as close to 1 as possible.

But it is not we cannot do it all the time, but in DG ETSOI MOSFET this is naturally there naturally m is equal to 1 and that is why Ψ_S is equal to V_G'. So, that is an advantage here because all the voltage that we apply on the MOSFET drops across the semiconductor in this case below threshold voltage.

So, in some threshold regime what we can say is that the gate has very good control over the channel that is a very important part of this device operation here because that gives us better performance as compared to the bulk MOSFET.

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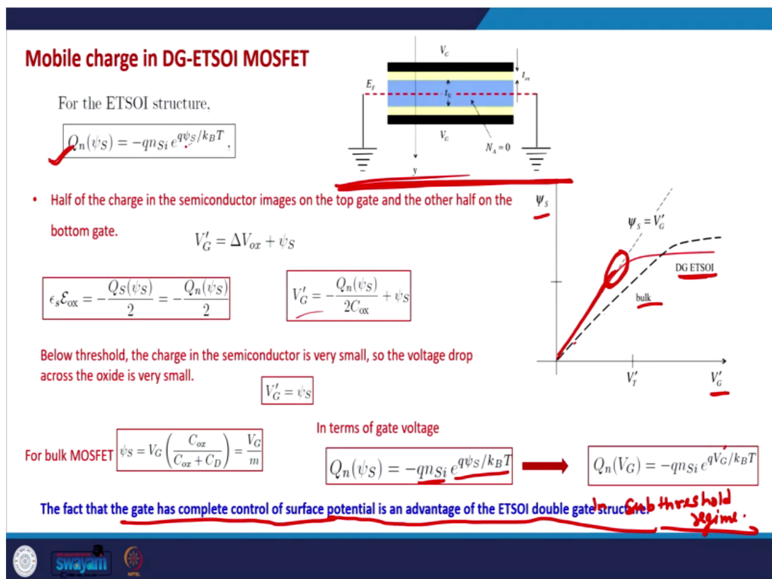

So, in terms of gate voltage if we now represent the mobile charge, so, the mobile charge is $-qn_{silicon}$ $\exp(q\Psi_S/kT)$ and now Ψ_S is just equal to V_G'.

So, Q_n can be represented in terms of gate voltage like this in sub threshold regime. So, now, the gate has complete control over the surface potential and that is an advantage of DG ETSOI structure. And if we compare the two plots the plots for bulk MOSFET and DG ETSOI MOSFET for Ψ_S versus V_G relationship what we see is that below threshold voltage in DG ETSOI MOSFET Ψ_S and V_G' are one and same essentially.

In the case of bulk MOSFET however, below threshold voltage Ψ_S closely follows the V_G' line, but it is not exactly the same it is somewhat different, but it deviates after the threshold voltage. Similarly, deviates in the case of DG ETSOI as well and the deviation in the case of DG ETSOI is even more. But we are mostly concerned about this regime and in this regime DG ETSOI MOSFET has better control over the channel.

So, the gate in double gate ETSOI MOSFET has better control on the channel as compared to the bulk MOSFET. And that is one of the main advantages of using DG ETSOI structure apart from geometric screening. So, that is why this is an important MOSFET technology specially for nano MOSFET specially for the some 20 nanometer or 40 nanometer that kind of channel length range.

In that range this is quite important MOSFET technology. And here we have seen the relationship between the charge in the MOSFET, the semiconductor potential and the gate voltage ok.

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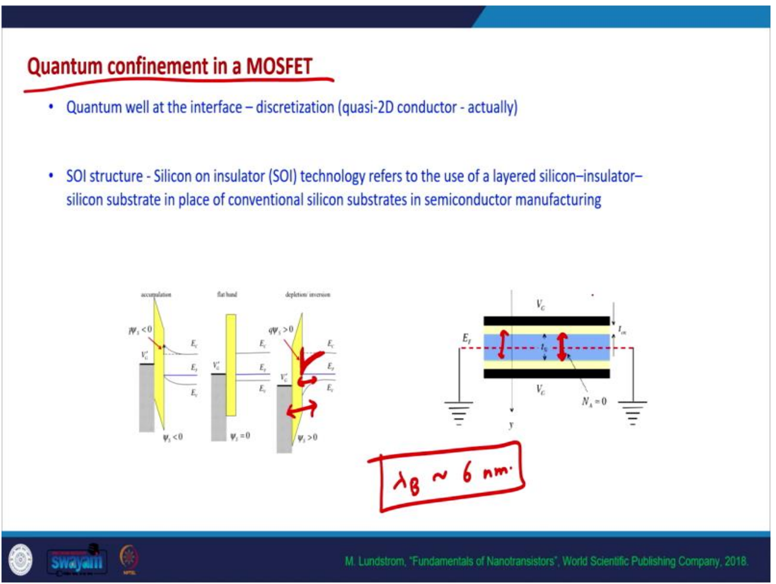

Now, let us come to an important concept in MOSFETs which is the idea or which is the quantum confinement in a MOSFET. And this topic we started in our previous class as well, but now since we have better understanding of ETSOI MOSFETs. So, we would be able to do it in a better way. So, as we saw in the last class the electrons in the inversion regime even in a bulk MOSFET are in a potential well and this potential well is like this.

Similarly, in ETSOI MOSFETs electrons are confined only in this distance and generally the De Broglie wavelength of electrons at room temperature is around 6 nanometer. So, if these confinements if this ETSOI silicon dimension is 10 nano meter or around that dimension or if this potential well is 5 to 10 nanometer in that case we need to consider the wave nature of electrons. And we need to consider the quantization in this direction or in this case quantization in this direction. So, both of these directions are y directions.

So and generally, what we observe is that the thickness of the inversion layer is few nanometers only around 4 to 6 nanometer of this range. So, what we can say is that in the inversion layer electrons are always confined in y direction and we need to consider this kind of quantum mechanical confinement in MOSFETs even in bulk MOSFETs. In

ETSOI MOSFET this confinement is there because of the geometry of the MOSFET as well.

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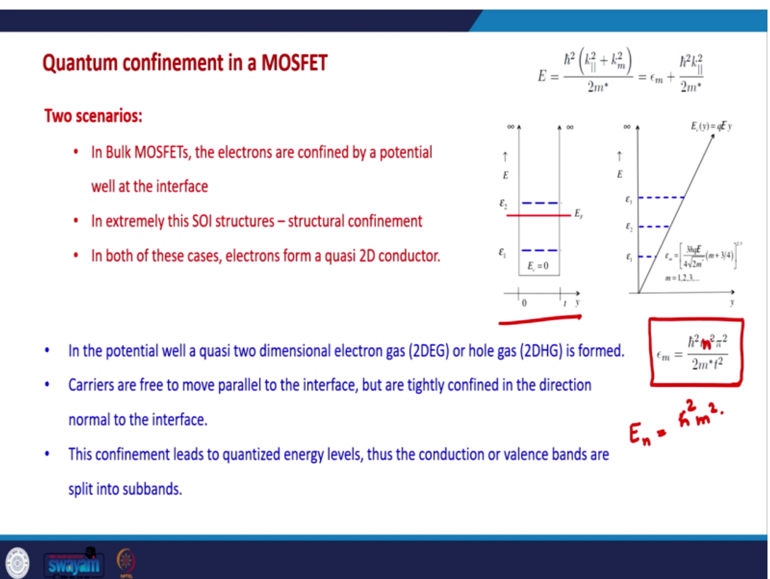

So, that is what we will try to understand now and. So, this is the kind of confinement that is there in bulk MOSFETs. This is the shape of the quantum well that is formed in the bulk MOSFET at the interface of the oxide and the semiconductor. And this is the kind of confinement that is there in ETSOI structures or most of the SOI nano scale SOI MOSFETs this is the case this kind of confinement is there.

So, now what happens is because of this potential well the electrons movement is confined in the y direction and confinement leads to discretization of energy levels. So, the electronic energy levels will be discretized in y direction and they may be continuous in x and z direction.

So, in y direction what happens is in this kind of potential well the electronic energy levels are given by this value as we have seen in particle in a box situation as well that the energy levels are given as h bar square m square.

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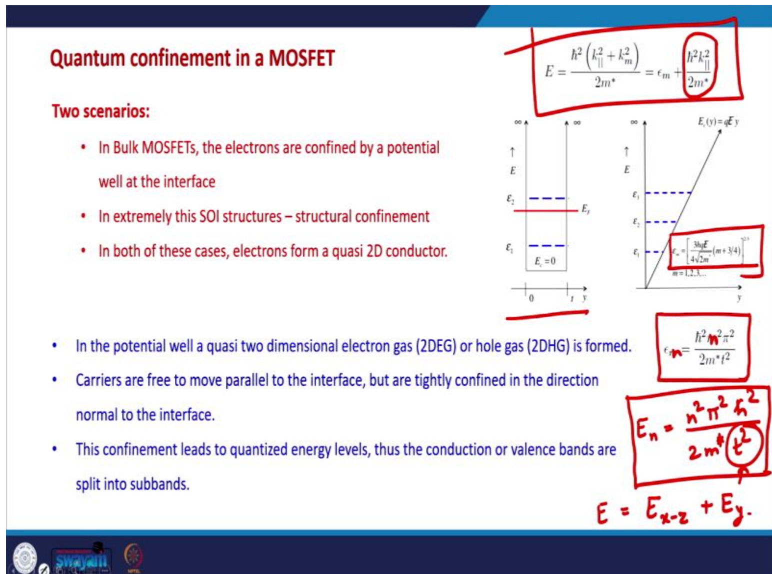

Now, this is not m square this is n square there is a typo in that equation that is written there. n square pi square h bar square divided by two m star t square, where t is the thickness of the ETSOI MOSFET.

Or t is the thickness of the inversion layer as well. So, we can generally for the sake of better understanding we can assume that even in bulk MOSFETs this kind of confinement is there. Although, if we do a proper analysis in a triangular quantum well which is there in bulk MOSFETs inversion layer there the energy levels are given by this relationship various energy levels are given by this relationship here ok.

So, what happens is that in y direction the electronic energy levels are discrete and they are given by this expression in x and z direction which is the transverse plane in that plane electronic energy levels can be continuous. So, the total energy of the electron is given by the energy in x z plane plus energy along y direction and that is what is written here as well.

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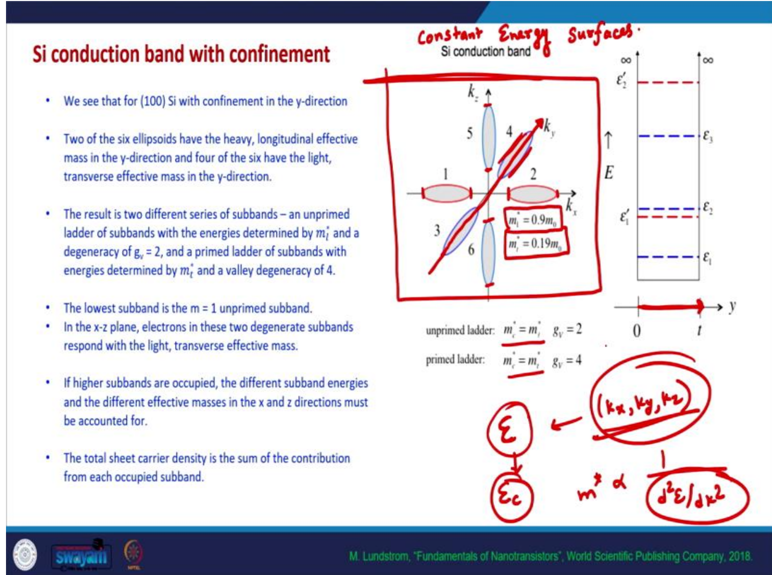

Now, something interesting happens here if we closely look at the band structure of the silicon. This is these are the ISO energy surfaces at the bottom of the conduction band or these are the constant energy surfaces. What it means is if we plot all the k values all the k_x k_y k_z points we have seen this before as well, but let me repeat it.

If we plot all possible combinations of k_x k_y k_z that give electronic energy close to or electronic energy equal to E and if we plot all these k points in case of silicon that gives us these 6 ellipsoids and these are that is why known as ISO energy surfaces or constant energy surfaces. And this for this particular case it is this energy is close to the bottom of the conduction band.

So, we always try to analyze close to the bottom of the conduction band because that is the point where most of the conduction takes place. So, close to the bottom of the conduction band the ISO energy surfaces look like this. And now in the channel because of the quantum confinement because of this kind of confinement what happens is that electrons are confined in y direction, electrons movement is restricted in y direction they are all the free to move in x z direction.

So, if we look at along y direction in this particular plane in this direction the electronic mass or the longitudinal effective mass of the electron will be given by the this curvature. Because if you remember the effective mass of the electron is inversely proportional to the $\delta^2E/\delta k^2$ square basically E k curvature. In this case this curvature is

actually representative of $\delta^2E/\delta k^2$. So, in this direction the effective mass will be given by this curvature and in x z direction the effective mass will be given by these curvatures essentially these curvatures.

So, as you can see in the longitudinal direction longitudinal means along the direction of the confinement the curvature is less. So, the effective mass will be more in the transverse direction the curvature is more. So, the effective mass will be less. So, that is why the longitudinal effective mass is 0.9 times the rest mass of the electron and the transverse effective mass is 0.19 times the rest mass of the electron.

So, what happens now is that because of these two kind of effective masses now there are two kind of energy levels that are generated in the system.

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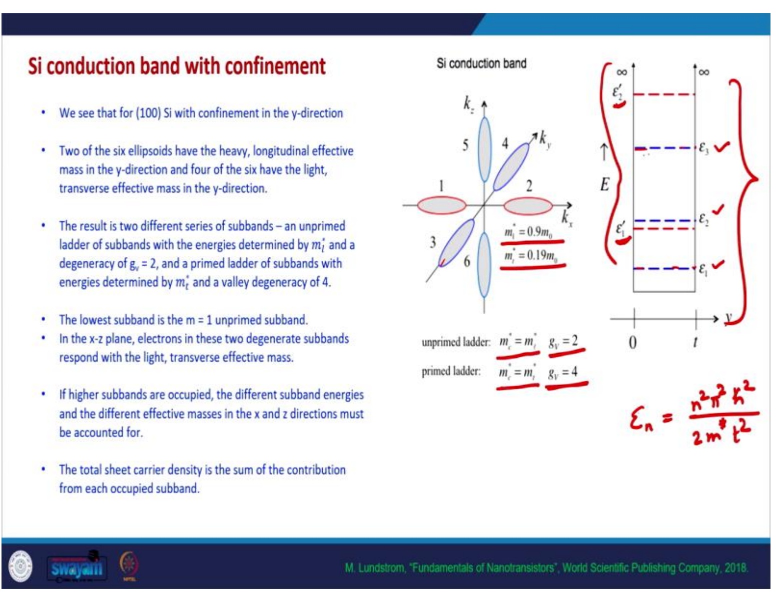

So, since we have, so we have two kind of electrons now in the system one kind of electrons have double degeneracy because there are 2 ellipsoids in the longitudinal direction and their mass is more. And another kind of electrons have less mass the transverse effective mass and their degeneracy is 4 because there are 4 ellipsoids corresponding to the transverse direction.

So, because of this difference because of these two kind of electrons in the system now we have two set of energy levels two set of discrete energy levels. And for heavy mass

the energies will be less because if you remember the energy the due to confinement is $n^2\pi^2\hbar^2/2m^*t^2$.

So, energy is inversely proportional to the effective mass. So, for the heavy electrons the energy levels will be low and for light electrons the transverse direction electrons the energy values will be high. So, the heavy electrons energies are represented by these €1, €2, €3 and the light electrons energies are represented by €1' and €2'.

So, these are the unprimed energy levels and these are the primed energy levels red ones are the primed blue ones are the unprimed. And these are because of the confinement in y direction because of the confinement in the y direction this degeneracy is now broken. In a bulk silicon generally what happens is electrons are free to move in any direction. So, the total mass, so the total conductivity of the electron is the sum of all the conductivities or the average of all the conductivities.

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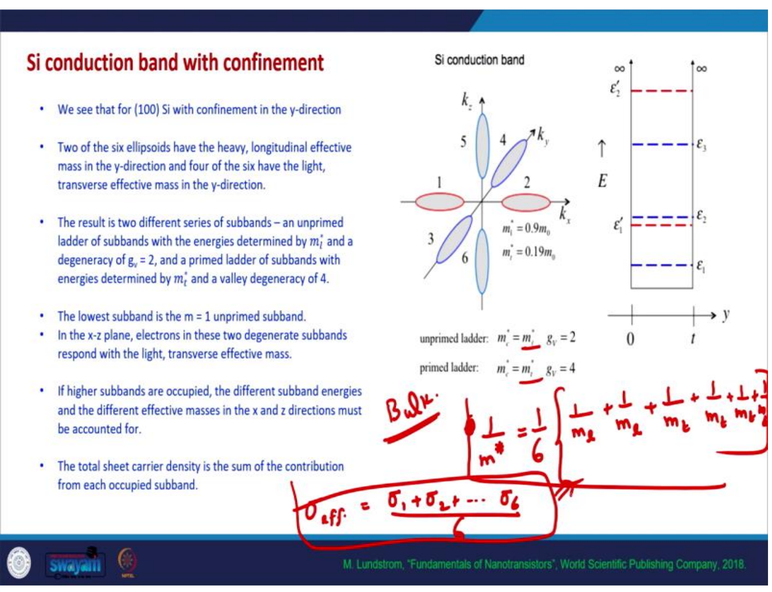

And that is why the net effective mass is the average of the conductivity is inversely proportional to the effective mass. So, if we in a bulk silicon if we try to calculate the conductivity effective mass it will be given by the average of the it comes from the.

So, the conductivity is effective conductivity is $(\sigma_1 + \sigma_2 + \ldots + \sigma_6)/6$ its average of all the conductivities. And each of these conductivity is inversely proportional to the

effective mass. So, this $\sigma_{effective}$ can be written as $1/m^*_{effective}$ and all these. So, these 6 conductivities correspond to these 6 ellipsoids.

So, in generally in any direction the 2 ellipsoids have longitudinal effective mass and 4 ellipsoids have transverse effective mass. So, that is why the net effective mass can be written as $1/m_l + 1/m_t$. So, the 2 have longitudinal and 4 have transverse like this.

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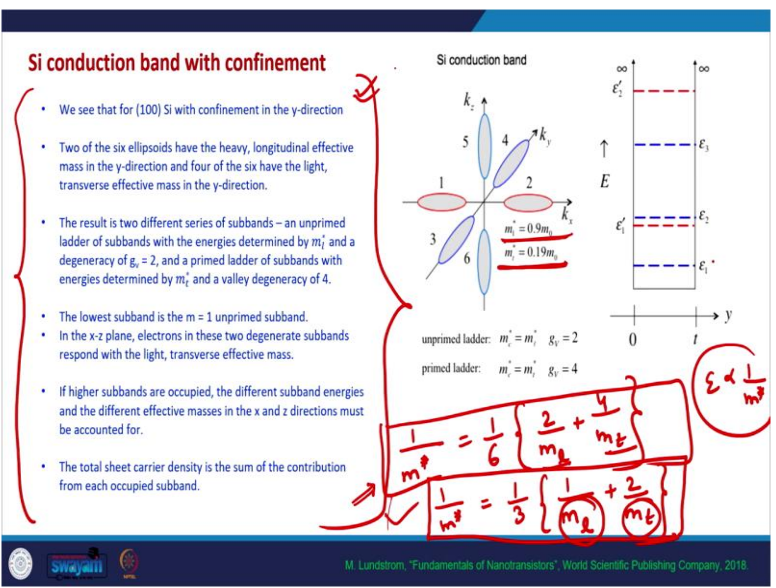

So, this expression actually gives us this kind of expression and from here we obtain what is known as the conductivity effective mass of the electron which is given by (1/6) $[2/m_l + 4/m_t]$ or $1/m^*$ is equal to (1/3) $[1/m_l + 2/m_t]$.

So, if the longitudinal and transverse effective masses are given for a particular silicon wafer in that case we can calculate the conductivity effective mass or the total effective mass of the electron that we need to calculate conductivity by this expression. So, this is an important expression and this is true for bulk silicon.

But as soon as there is confinement because of now what happens is in one direction also there are two kind of electrons and these the energies of these two kind of electrons are now inversely proportional to the mass. So, this degeneracy is lifted between the longitudinal effective mass electrons and transverse effective mass electrons and that is why we will have two kind of sub bands in the system.

So, I would recommend all of you to go back and go through the class where we discussed the idea of sub bands how do we consider sub bands in a quasi 2D material and exactly the same thing is happening here. Because here also we need to consider sub bands, but now we have two kind of sub bands one is because of the heavy electrons having longitudinal effective mass and one is because of the light electrons having transverse effective mass ok.

So, this is the picture that is there in the case of confined electrons in the case of quantum confinement in MOSFETs. So, please remember that in bulk silicon there is all the all these valleys are degenerate, but now in this case because of the confinement the degeneracy is lifted. Now, there are two different kind of sub bands in the system. So, this is a summary of or this is the text to understand this phenomena this degeneracy the lifting of degeneracy.

Because of the quantum confinement I would recommend all of you to go through this text carefully ok. So, this brings us to another an important idea in nano MOSFETs which is the strain engineering. Strain engineering essentially means using a strained silicon as I told you in the beginning of the class to have better performance.

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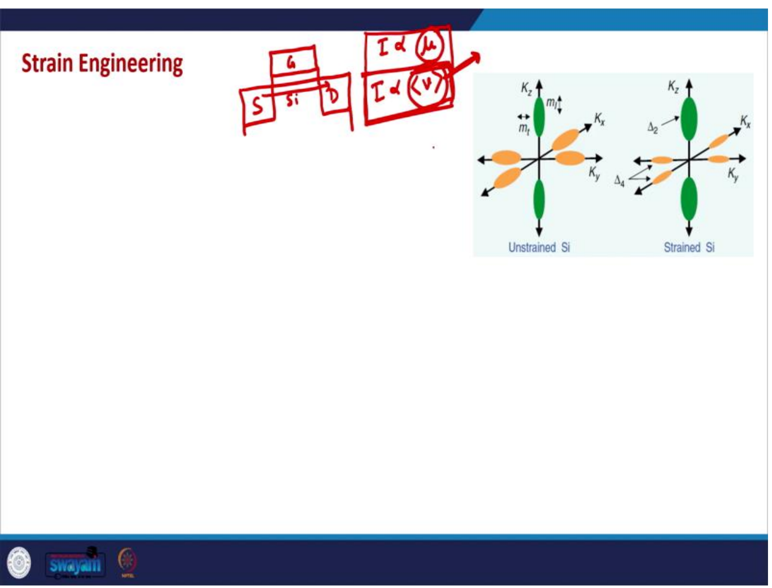

And in strain engineering essentially what we do is we apply strain or generally let me give you an example of biaxial strain. Biaxial strain means that if this is the MOSFET source drain or let me draw ETSOI MOSFET.

So, we have this kind of structure silicon is there this is the silicon channel source and drains are there this is oxide this is the gate electrode. Now, the current in this MOSFET depends on how fast the electrons can go from source to drain or what is the mobility of electrons in the MOSFET. So, if you remember in bulk MOSFETs current is directly proportional to the mobility and even in ballistic MOSFETs current is directly proportional to the injection velocity at the top of the barrier.

So, in order to have a better current better performance of the MOSFET at a given voltage we would like to increase the mobility of electrons or the injection velocity of the electrons. And one of the techniques is to use strain silicon strain silicon means that instead of using a normal silicon in the channel we now use a silicon whose lattice structure has been changed.

And we will see that for certain kind of change in the lattice structures the velocity of electrons the injection velocity of electrons will increase that will increase the current drive current in the MOSFET. And that can give us better performance without scaling. So, that is one of the modern techniques to enhance the performance of nano MOSFETs and let me not start that this topic right now because it will involve a longer discussion.

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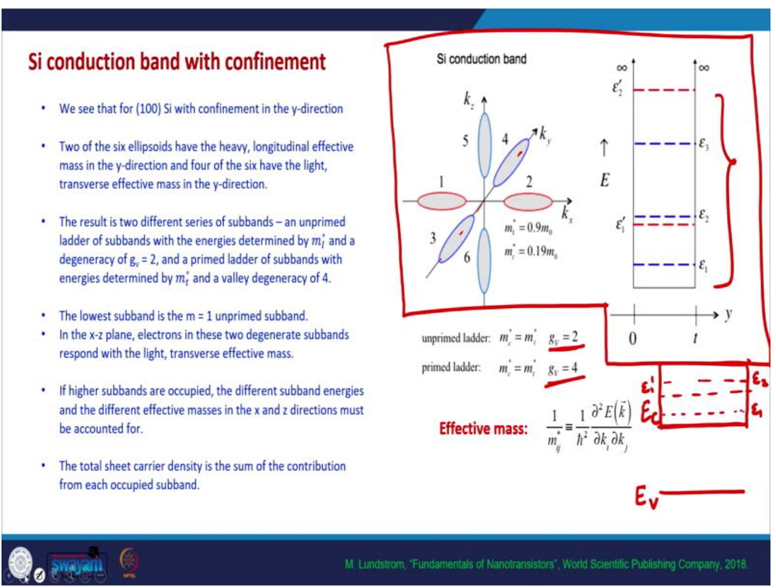

So, if we understand the idea of quantum confinement and how various sub bands or how 2s kind of sub bands are formed we can understand the strain engineering or the strained silicon as well. Please remember that these unprimed energies they have

degeneracy equal to 2 because they have 2 lobs corresponding to them. There are 2 ellipsoids that give us longitudinal effective mass and the transverse effective mass is given by 4 ellipsoids. So, their degeneracy is 4 ok.

So, in any case, so generally in bulk silicon what we do is we consider the top of the valence band in the bottom of the conduction band. But in the case of quantum confinement or in inversion layer or in ETSOI MOSFET in addition to these energy levels we also need to consider the sub bands. So, we need to consider epsilon 1 epsilon 1 prime and these essentially these energy levels. So, the electrons will be occupied in the conduction band in these two sub two kind of sub bands.

So, please review the idea of sub bands that we discussed while we concluded our discussion of the general model of transport and then this idea of quantum confinement will be clear to all of us. So, with this kind of background with this background of quantum confinement in MOSFETs our next topic of discussion will be the strain engineering or how to use strained silicon to have better performance of devices. So, that is what we will do in the coming class.

Thank you all. See you in the next class.