Physics of Nanoscale Devices
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Lecture - 53
MOSFET 2D Electrostatics

Hello everyone, today we will discuss a very important topic in nano MOSFET electrostatics which is the 2D Electrostatics of MOSFETs.

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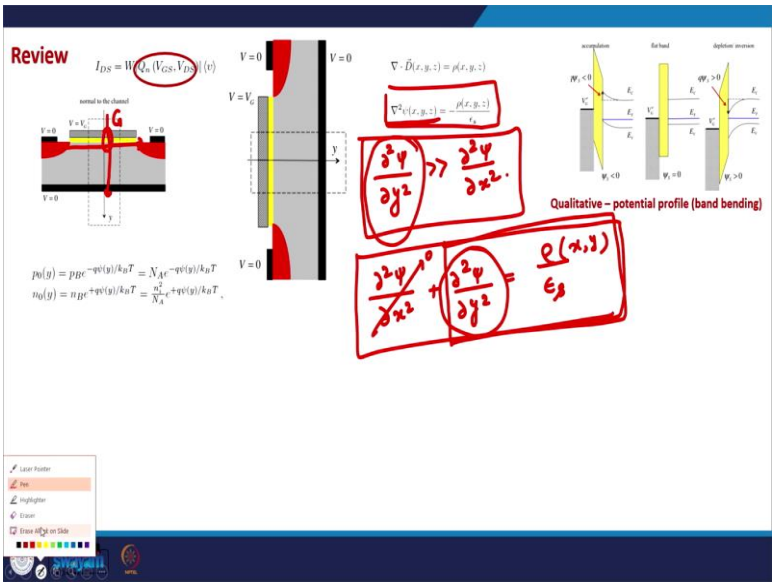

And if you recall what we have been discussing so far is actually 1D electrostatics, which means that we have only considered the Poisson equation in y direction which is the direction normal to the channel, which is from the gate through the channel to the substrate or to the body this direction only.

And there are valid reasons to do that because in conventional MOSFETs, the thing is that the electric field in this direction and especially in this region is extremely strong as compared to the electric field in this direction. Or in other words what happens is that this quantity the second derivative of the potential which appears in the Poisson equation that is so this $\delta^2\Psi/\delta y^2$ is large as compared to $\delta^2\Psi/\delta x^2$ in the case of long channel or in case of conventional MOSFETs.

And that is why we can just do proper electrostatic treatment of the MOSFET just using the electrostatics in y direction, because if we consider the electrostatics both in x and y direction in that case the Poisson equation will look something like this.

$\delta^2\Psi/\delta y^2$ it should be equal to ρ/ϵ_S ok, but in most of the conventional MOSFETs this quantity is almost 0 or this is extremely small as compared to this one. And so that is why we can just solve this Poisson equation and do our electrostatics which is the conventional electrostatics in MOSFETs.

So, just to quickly review that we have seen is, what we have seen is that in order to understand this 1D electrostatic picture, we sort of tilt the MOSFET in this direction. So, that this y direction becomes the horizontal direction and the bands look like this in various regimes of MOSFET operations.

This is the accumulation regime when negative gate voltage is applied on a p on a N-MOSFET. Which means that this negative gate voltage will attract lot of holes at the interface bit on the at the interface of oxide and semiconductor and it will lead to the accumulation of holes. This is the flat band situation and this is the depletion or inversion region when a positive gate voltage is applied.

So, this picture, this band diagram picture in y direction when the MOSFET is tilted, this gives a very good intuitive understanding of the electrostatics of the MOSFET and MOS capacitor.

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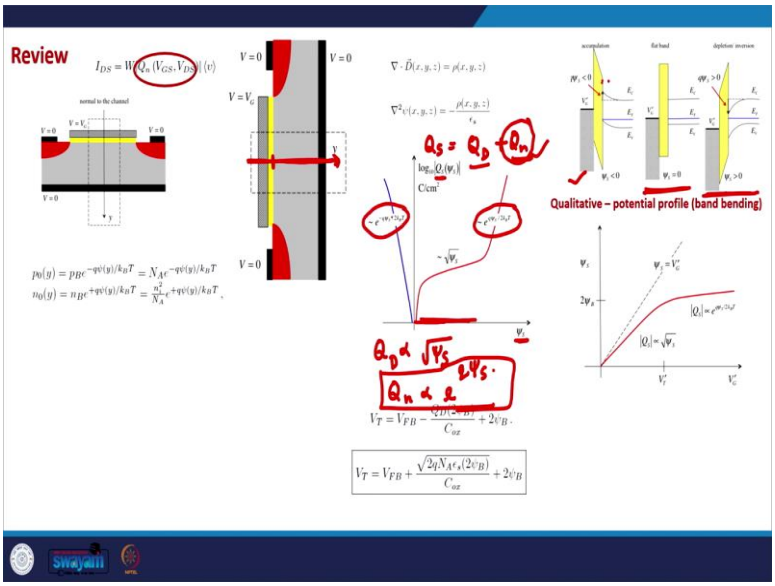

Second is after; so we have already gone through this and after this we saw that the semiconductor charge Q_S. And the surface potential the semiconductor surface potential which is the electrostatic potential right at the interface of the oxide and the semiconductor at this point, which is just the beginning point of the semiconductor this follows this kind of relationship.

And as we can see that for low Ψ_S values we the MOSFET is operating in depletion regime and in the depletion regime, the charge is directly proportional to the square root of Ψ_S. But for a large positive value the MOSFET operates in a in inversion regime and in inversion regime the charge is mainly due to the mobile electrons and that is that has exponential dependence. So, this is the depletion charge and the inversion charge has the exponential dependence on Ψ_S.

The total semiconductor charge this Q_S is actually the sum of Q_D + Q_n which is the depletion charge plus the charge due to inversion or the charge due to mobile carriers. In the accumulation regime there is no depletion and the only charge that is there is because of the accumulation of majority carriers and that has exponential dependence. So, this is an important relationship of the semiconductor charge as a function of semiconductor surface potential.

Because this gives us a lot of idea of how things are going on at various gate voltages. Then we also saw the relationship between Ψ_S and V_G, which is the dependence of Ψ_S on

the externally applied gate voltage. V_G is the voltage that we apply on the device and Ψ_S is the voltage that appears on the interface finally, all most of the electrostatics is governed by the Ψ_S, but this Ψ_S is controlled by the V_G voltage.

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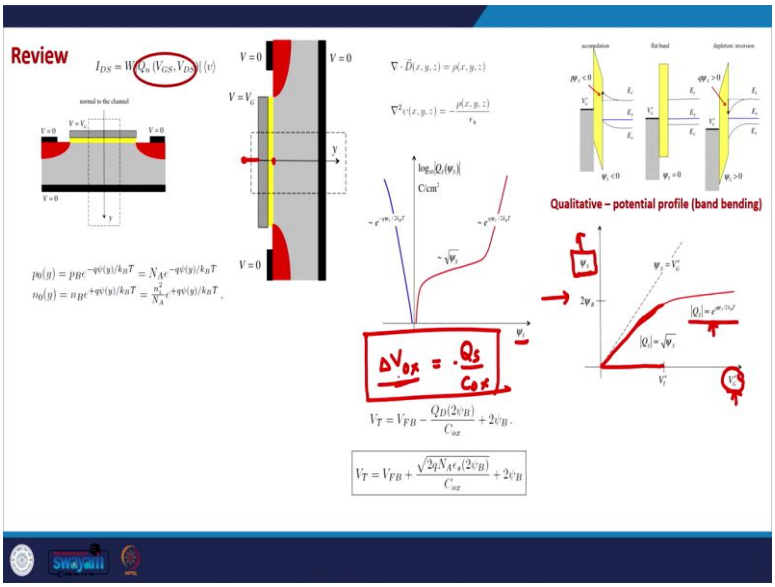

So, we would also like to understand the relationship between Ψ_S and V_G and this is how it looks like. And as you can see from this picture below threshold voltage the Ψ_S voltage is approximately equal to the applied gate voltage. So, the Ψ_S curve follows the V_G line, but as soon as the gate voltage approaches the threshold voltage and it is more than threshold voltage in that case the Ψ_S does not increase much, because the semiconductor charge which is the inversion charge increases exponentially.

And this exponential increase in semiconductor charge actually increase the voltage drop across oxide, because the voltage drop across oxide is $-Q_S/Cox$. So, if this Q_S is more, then ΔVox will be a large number. So, this is the relationship between Ψ_S and V_G.

So, that is how we can understand the relationship between Q_S and V_G, if we sort of couple these two both of these plots.

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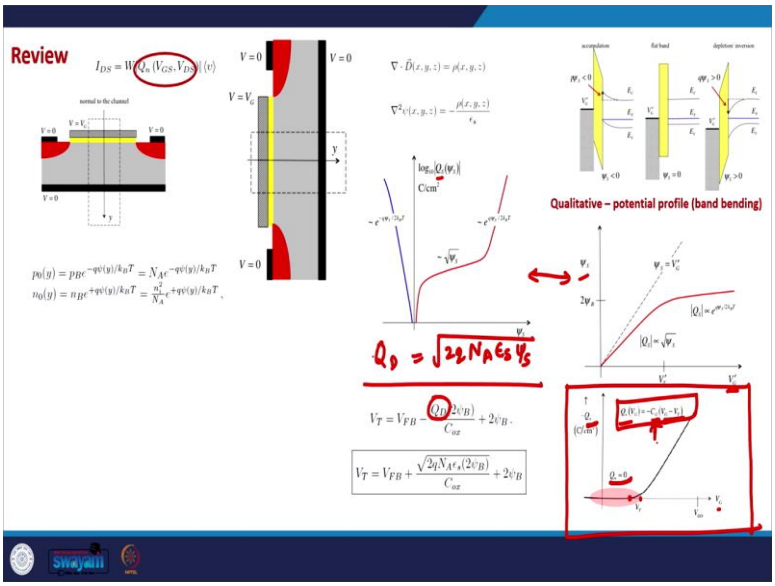

Finally, there is. So, we have seen that the depletion charge is directly related to the surface potential via this relationship and we would also like to know how the mobile charge is related to the gate voltage. So, this is I would say a qualitative picture of the relationship between Q_n which is the mobile charge in the MOSFET, which is the charge due to the inversion layer due to the electrons in the inversion layer.

And as we can see from this plot that in the sub threshold regime, which is the case when V_G is less than V_T in that case Q_n is extremely small number and its almost equal to 0, well below the threshold voltage it is almost equal to 0. It starts increasing exponentially as the gate voltage approaches the threshold voltage and then it increases abruptly ok.

Finally, what we see here is that this Q_n can be written in terms of the gate capacitance above the threshold voltage and it follows this particular relationship, because the gate capacitance also involves the semiconductor and oxide capacitance. So, after a certain value of V_G after, once the V_G is greater than V_T in that case V_G is well above V_T in that case this gate capacitance is almost constituted by the oxide capacitance. And that is why we see this linear kind of relationship.

After that we saw how to derive the threshold voltage for the MOSFET and the threshold voltage looks like this. The threshold voltage is equal to the flat band voltage, which is the voltage that we need to apply in order to align the or in order to flatten the bands in

the semiconductor, when the Fermi levels of the semiconductor and the gate are not aligned.

So, in many cases what happens is without any externally applied voltage. The Fermi level of the gate and the Fermi level of the semiconductor are not aligned and that is why there is a band bending at 0 bias and in order to neutralize that band bending we need to apply the flat band voltage.

So, by considering the flat band voltage and the depletion charge, this is the formula for the threshold voltage and as we can see the threshold voltage is the voltage when the semiconductor potential Ψ_S is equal to $2\Psi_B$. Which means that the semiconductor at the interface is as n type as the semiconductor is p type in the bulk.

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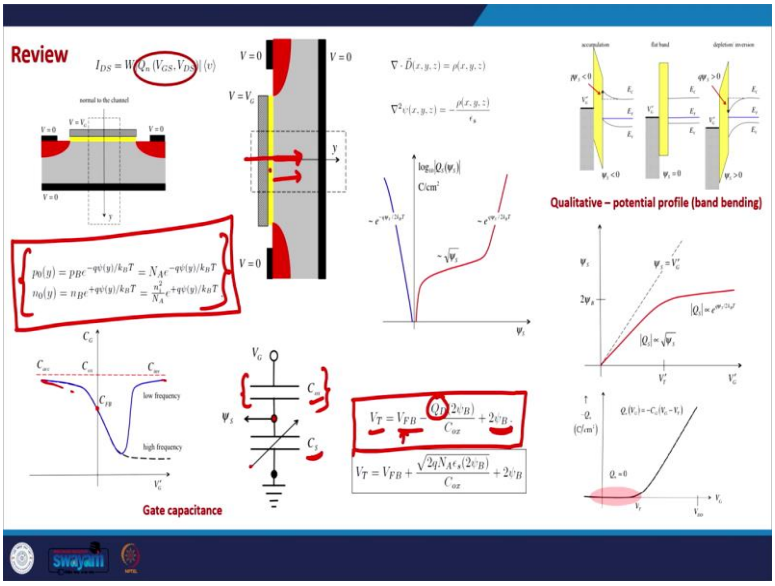

So, after that we saw the notion of gate capacitance and which is the capacitance as seen from the gate terminal and as we know that if we look from the gate terminal we would come across the oxide capacitance, which is a dielectric capacitance and is a constant capacitor constant value capacitor the capacitance will be constant for the oxide.

And then beyond the oxide we have the semiconductor which is a voltage dependent capacitor, because the semiconductor capacitance changes as the gate voltage or the surface voltage Ψ_S is changed. Because when the Ψ_S value is positive in that case first

the depletion region appears, where we where the depletion capacitance comes into picture.

And then the inversion layer comes up where the inversion by considering the inversion capacitance in inversion layer as well we realize that the semiconductor becomes like a metallic plate and in that case the capacitance changes as compared to the depletion capacitance.

So, the semiconductor is a voltage dependent capacitor in a way and in that so that is why we have saw we see here, that this gate capacitance is a series combination of oxide capacitance and a voltage dependent semiconductor capacitance.

And it has a frequency dependent which we discussed last time, at low frequencies in a MOS capacitor this would be the behaviour of C as a function of V_G. At high frequency the capacitance will be low because in a MOS capacitor the inversion layer cannot respond to the applied gate voltage at high frequencies. However, if we are if we talk about the capacitance of a MOSFET in that case the capacitance of a MOSFET will look like the low frequency plot.

Because in MOSFET in the inversion layer, the minority carriers in order to make inversion layer they can come from the contacts. And the mobile charge carrier density inside the semiconductor is given by these relationships which come from the carrier statistics in semiconductors. So, this is all what we have seen so far in the discussion of the conventional electrostatics of MOSFETs.

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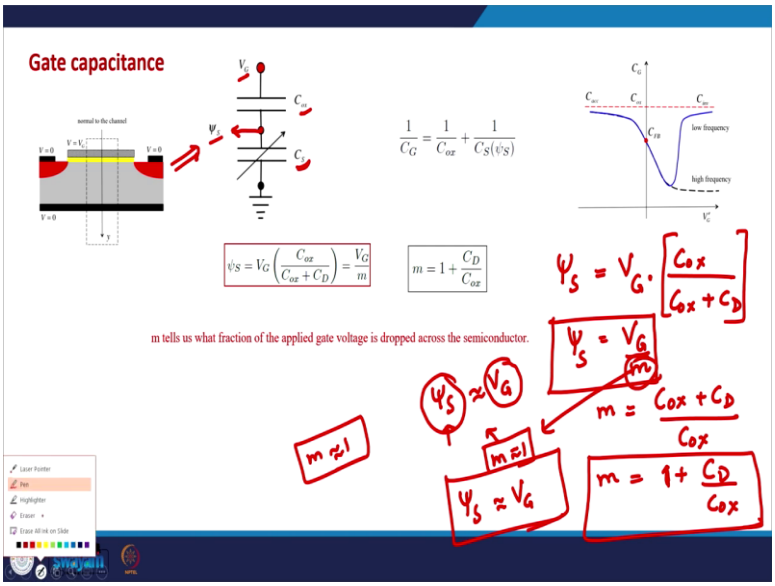

Now, and this is what we saw last time, that the relationship between Ψ_S and V_G can also be written down in terms of the capacitances in terms of the gate oxide capacitance and the semiconductor capacitance. And if we sort of model this MOSFET as a series of two capacitors, in that case we realize that V_G is the voltage at the top of these two capacitors Ψ_S is the voltage in the in between actually in between Cox and C_S.

So, then according to the voltage division rule across capacitors, Ψ_S can be written as V_G times Cox divided by Cox + C_D which means that we can write it down as V_G divided by m, where m is (Cox + C_D)/ Cox which is 1 + C_D/Cox. So, this m as you can see is a number which would be greater than 1 because it is 1 + C_D/Cox and from this relationship Ψ_S equals V_G by m.

We see that if m is larger than 1, m is a large number in that case Ψ_S would be small as compared to V_G. And if m is closer to 1 in that case Ψ_S will be almost equal to V_G. So, this m which is known as the body coefficient of the MOSFET it actually governs how much of the gate voltage will drop across the semiconductor, because the voltage that drop drops across the semiconductor is Ψ_S.

So, if this m approach is 1, in that case Ψ_S will almost be equal to V_G; and what does that mean? It means that if m is almost equal to 1, in that case most of the gate voltage is dropped across the semiconductor. Which means that the external voltage that we are

applying on the gate is totally used to deplete the MOSFET or invert the MOSFET to create the inversion layer in the MOSFET.

So, ideally, we would like and to be as close to 1 as possible always. So, we always try to make sure that m is as close to 1 as possible ok. So, that is a design constraint that we keep in mind that while designing a MOSFET. Generally, the device designers try to make sure that m is not far away from 1 and in order to bring m closer to 1, what needs to be done is that this second factor C_D / Cox this needs to go to 0 actually.

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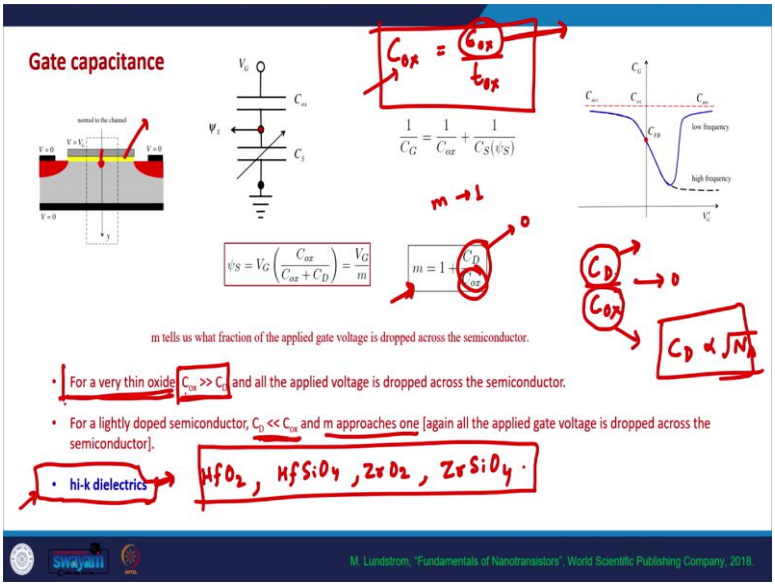

So, we need to make C_D by Cox as small as possible. So, how do we do that? We can do that by 2 ways, one is by having a small C_D by making C_D as small as possible or by having a large Cox, which means we would like to have Cox as large as possible and C_D as low as possible. So, in order to have C_D as low as possible, we need to have a lightly dopped semiconductor. Because as you recall C_D is directly proportional to the doping of the semiconductor.

So, if the doping is less in that case C_D is extremely smaller than Cox and in that case m approach is 1, the second way is if you by taking a very thin oxide. So, if you recall the formula of Cox; Cox is ϵ_{OX}/t_{OX}. So, this is the Cox per unit area, the oxide capacitance per unit area and if t is extremely small in that case Cox becomes larger and in that case C_D/Cox becomes smaller.

So, by making a very thin oxide we could make sure that Cox is extremely large as compared to the depletion capacitance and that way we can bring m closer to 1. But there is there is a trade off in making a very thin oxide because as soon as the oxide thickness goes below two angstroms in that case what happens is that there is a tunnelling of carriers from gate to channel.

So, there the tunnelling current from the gate to the channel starts becoming prominent and we would always like to avoid that. So, we cannot always make a very thin oxide or in fact, making oxide thinner than two angstroms can severely impact the functioning of the MOSFET, because in that case the tunnelling current would increase and this drain current will be disrupted.

So, the other way to increase Cox is we would like to have larger ϵ_{OX}. So, the dielectric constraint of the oxide, if it is larger in that case epsilon ox will be large and we can ensure that m is closer to 1. So, which means that we need to use hi-k dielectrics. So, this hi-k dielectrics is a new area is entirely because generally in MOSFETs silicon dioxide is the oxide which is used as a gate oxide.

And the reason for using silicon dioxide is the ease of fabrication, because we can just oxidize a very thin silicon layer to make silicon dioxide and in that case, we do not need to worry about the matching of the oxide and the silicon. And even the interface charges can also be controlled to a large extent, but if we want to use hi-k dielectrics which means the oxides which have high epsilon ox.

In that case we would need to put another kind of oxide on top of silicon and in that case, we need to keep many things in mind. One is one factor that we need to keep in mind is that the lattice of the silicon and the oxide should match, the bands should also match. So, those kind of constraints when we need to keep in mind.

But generally, the hi-k dielectrics that are used in the MOSFET fabrication are hafnium dioxide, hafnium silicate, zirconium dioxide and zirconium silicate because these dielectrics they are it seems that they can; they have high dielectric constant, as well as they can be fabricated in a much better way as compared to the other oxides ok.

So, we will again come back to this point of hi-k dielectrics apart from having a better body coefficient, we again these hi-k dielectrics are also useful to make smaller or

miniaturized devices, because as we miniaturize the MOSFET in that case the oxide thickness also needs to be made smaller in order to have a better current. And for that and as we just discuss that we cannot make oxide arbitrarily thin.

Because that would lead to increase in the tunnelling current, tunnelling from the gate to the semiconductor. So, the other way is in order to have high oxide capacitance, we use the hi-k materials, hi-k dielectric materials in small in smaller MOSFETs ok. So, we will come back to this point again. But this essentially concludes our discussion of the conventional electrostatics of the MOSFET and a large part of this is also applicable to the nano MOSFETs ok.

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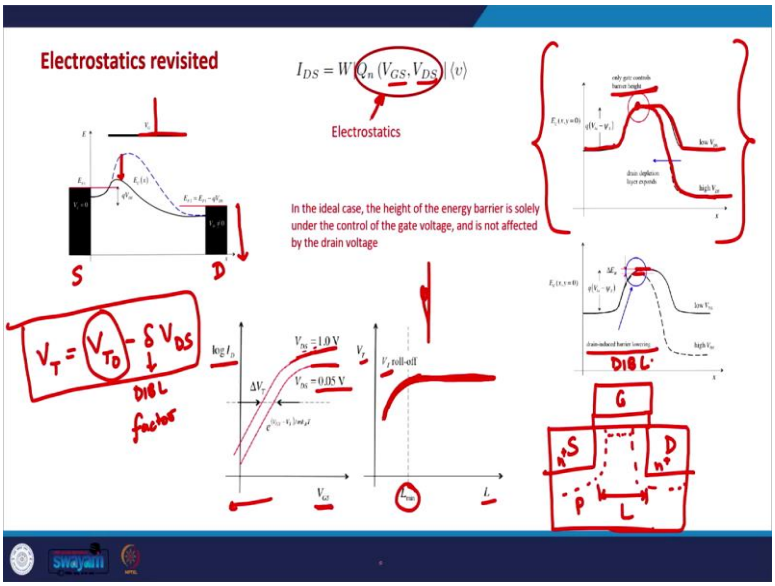

Now, we will see the 2D electrostatics actually, the electrostat; how the electrostatics change in small MOSFETs and again just to quickly review the electrostatics; in electrostatics we are mainly concerned about the charge in the channel which depends on both V_{GS} and V_{DS} and this is the picture of a MOSFET. In this picture as you can see there is a source there is a drain and there is a gate terminal.

And there is a barrier in the channel between the source and the drain and this barrier is controlled by the gate terminal and the drain terminal. So, what does the gate terminal do? The gate terminal essentially lowers the barrier. So, the barrier height depends on the gate terminal.

And what does the drain terminal do? Drain terminal essentially brings down the Fermi level of the drain side or the drain voltage brings down the Fermi level of the drain side, which essentially allows a net flow of electrons from the source to the drain.

So, that way we have a properly well defined tasks or well defined functions of the gate and the drain terminals. By using the gate voltage we can control the barrier height and by using the drain voltage we can control the symmetry of the barrier to allow the electron flow from the source to the drain.

So, this is the ideal scenario in which ideally the barrier height should only depend on the gate voltage and not on the drain voltage. Because if the barrier height depends on the drain voltage, then it creates a kind of non-uniformity across various device because various MOSFETs might be operating at different drain voltages, some might be at 0 drain voltage some might be at 1 drain voltage or high drain voltage.

So, in that case there might be a non uniformity between various MOSFETs. So, ideally this barrier height should only be dependent on the gate voltage and that is again I would say is one of the things that the device designers keep in mind, while designing a good MOSFET, that this barrier height should not depend on the drain voltage.

And we have seen it earlier as well that, especially in smaller MOSFETs what happens is; so this is here we have two figures the top figure actually is the ideal case, in which this barrier in the channel is shown for 2 drain voltages. This is the low V_{DS} and this is high V_{DS} and this barrier height or the peak this top of the barrier the peak on the source side it does not change with V_{DS}. So, this peak is the same for both high V_{DS} and low V_{DS}. So, this is what we try to ensure while designing a MOSFET.

So, only the gate terminal controls the barrier height ok, but generally in smaller MOSFETs, in a in small channel MOSFETs what happens is at high V_{DS} even the barrier height is actually lowered by some value and this is known as the drain induced barrier lowering which we have already seen. And this is best characterized by the sub threshold plot which is the plot of log I_D as a function of V_{GS} for a various V_{DS} voltages.

So, this is the plot for V_{DS} equals to 0.05 volts, a small V_{DS} and this is the plot for high V_{DS}, 1 volts. And as you can see that as the V_{DS} is becoming higher this I_D versus V_G plot is shifting to the left side, which means that the threshold voltage is now lowering.

So, this is this results in the change in the threshold voltage and that is why the threshold voltage most of the times is written as V_T is equal to V_{T0} - δV_{DS}, where δ is the DIBL factor δ. So, V_{T0} is the threshold voltage in ideal case and δ is the DIBL parameter. So, it shows that V_T also changes with V_{DS}, which is what we want to avoid.

Also, more generally in small channel devices there is this kind of phenomena are summed up in a plot of V_T versus L, threshold voltage versus length. So, what it shows is that the threshold voltage is ideally independent of the length for most of the lengths of the MOSFETs, but as soon as the MOSFET length, the device length starts getting smaller than a certain value, then there is a reduction in the threshold voltage.

So, the threshold voltage V_T, becomes dependent on the channel length and this is known as the threshold voltage roll off. One of the reasons of the role off is DIBL, there might be other reasons as well because as soon as the threshold as soon as we make smaller devices the depletion regions. So, let me quickly demonstrate it here this is a typical MOSFET, we have a source we have a drain, we have an oxide, we have the gate terminal.

If this channel length is shrinking in that case what happens is the source and the drain are coming closer to each other and since the source is n-type or n plus type the semiconductor is p-type the drain is also n plus type. So, there is a depletion region because this is a p-n junction and there would be a depletion region around the source and the drain junctions. So, what happens is that in smaller devices these depletion regions can become significant part of the channel.

So, which means that now there is a small smaller charge that or a smaller voltage that is need to deplete the channel, because a large part of the channel is already depleted because of these p-n junctions. The p-n junctions between the source and the and the device and the drain and the body source and the body. So, only this part of the channel needs to be depleted by the gate voltage.

So, that is why we need smaller gate voltage in order to totally deplete the channel region and which means that we need smaller voltage to make an inversion layer and which means that the V_T becomes smaller.

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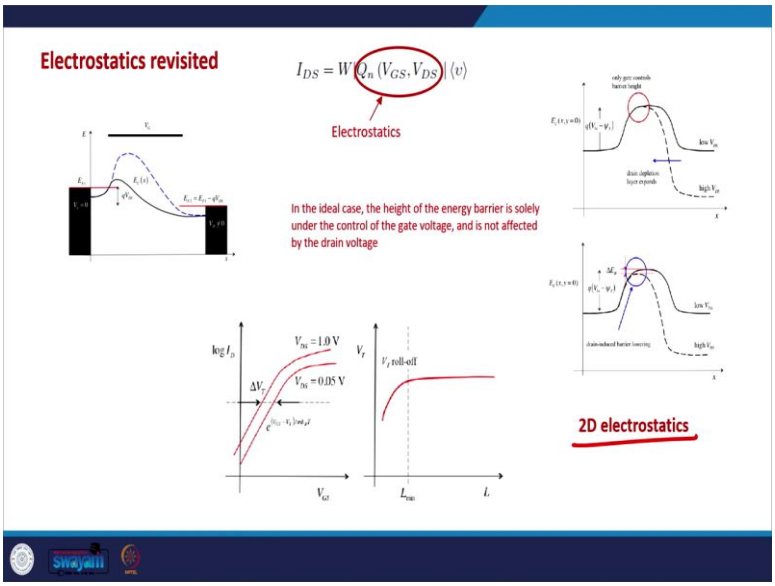

So, generally this is the phenomena this V_T roll off the threshold voltage roll off is observed in smaller MOSFETs and this is a typical small channel effects, this is a consequence of the small channel effects DIBL is one of them.

So, in order to properly characterize and understand all these things, we need to deal with the 2D electrostatics of the MOSFET. So, by understanding the 2D electrostatics, we would be able to understand these phenomenon and we would be hopefully able to solve some of these problems as well.

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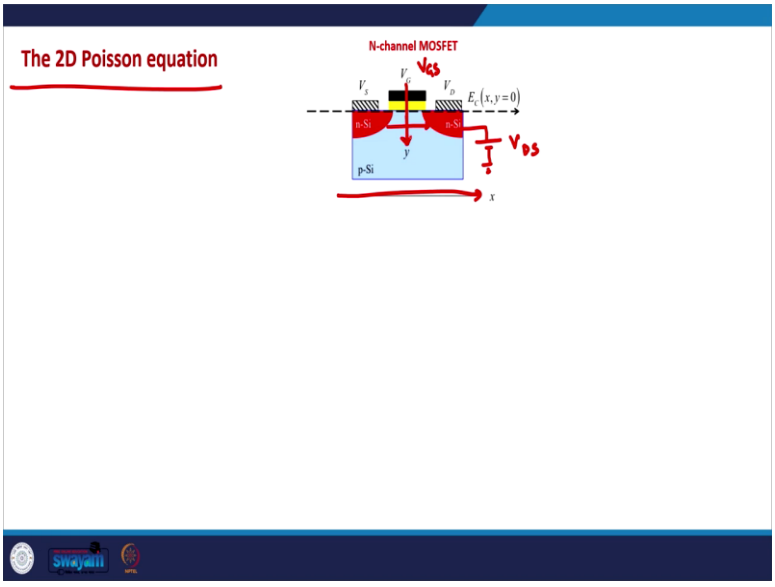

So, that is what we will do now. We will try to see how the 2D Poisson equation looks like in the MOSFET.

So, this is the general picture of our MOSFET, the channel direction is the x direction and the normal to the channel which is from the gate to the body is the y direction in this direction the V_{GS} voltage is applied in x direction we generally apply a V_{DS} voltage ok.

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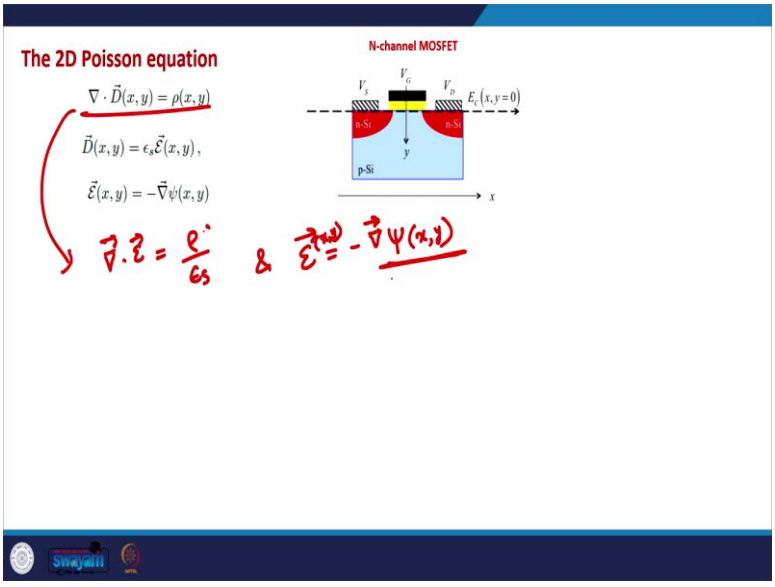

In smaller devices we have already seen that the electric field, both along the channel and perpendicular to the channel are important. And that is why we need to consider the 2D electrostatics or 2D Poisson equation which is we need to write the Poisson equation in both x and by considering the charge distribution both in x and y direction due to the electric field in x and y direction. So, the 2D Poisson equation looks like this. So, general Poisson equation is ▼.D is ρ, ρ is the special charge distribution, D is the displacement electric field vector.

And in 2D in both x and y directions D(x,y) is ϵ_S which is the dielectric constant of the semiconductor times the electric field as a function of x and y. So, now, we are considering both electric field in both directions, both in along the channel x direction and perpendicular to the channel y direction. So, that means, that this Poisson equation ▼.D can be written as ▼.E = ρ/ϵ_S.

And in 2D the electric field is the gradient of the 2D potential in the semiconductor. So, now, this semi conductor potential psi this also becomes a function of two variables both x and y.

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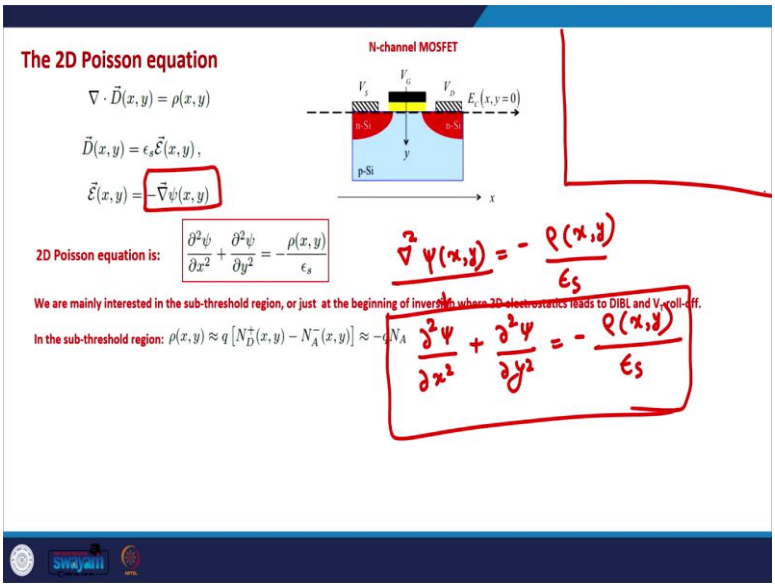

So, the 2D Poisson equation ultimately will look like this if we substitute E is equal to -▼Ψ(x, y) in this equation. So, this equation will be $\blacktriangledown^2\Psi(x,y) = -\rho(x,y)/\epsilon_S$.

So, this left-hand side is essentially $\delta^2\Psi/\delta x^2 + \delta^2\Psi/\delta y^2$, is equal to -ρ which is the charge density in the semiconductor divided by the dielectric constant of the semiconductor. So, this is the 2D Poisson equation in the channel region of the semiconductor and if we quickly recall the 1D Poisson equation, the 1D Poisson equation looks like this.

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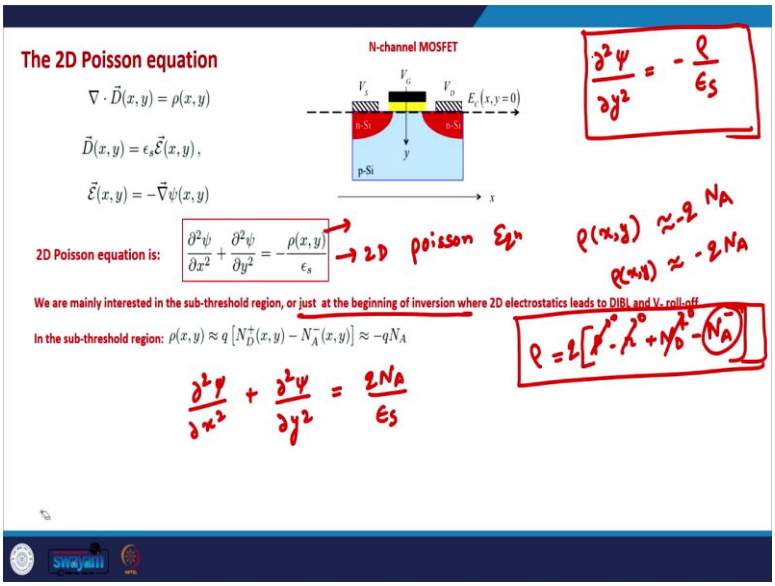

So, this is the 2D Poisson equation, the 1D Poisson equation looks like this and generally the most prominent impact of the 2D electrostatics or most prominent impact of the small channel effects happens in the sub threshold regime, which is just at the beginning of the inversion. Just before the inversion or around the inversion regime that is where we notice the effect of the 2D electrostatics, as is also clear from here.

So, we see that the voltage the threshold voltage rolls off which means that the voltage at which the channel is getting formed the channel is getting inverted is getting smaller and the I_D curve the transconductance curve I_D versus V_{GS} is getting shifted to the left side. And this is visible or this is prominently important around the threshold voltage. So, just at the beginning of the inversion what is the charge in the channel.

Just at the beginning of the inversion we generally assume that the charge due to the electrons the mobile charge is negligible as compared to the depletion charge, which is also true that is what we have also seen earlier. So, this $\rho(x,y)$ just at the beginning of inversion can be written as the charge due to the depletion, just due to the depletion. In general this ρ is actually q this is that charge due to holes minus the charge due to electrons plus the charge due to ionized dopants minus the charge due to ionized acceptors.

So, generally this is the space charge density in the semiconductor, but just at the beginning of the inversion this is 0, this is 0 and we are assuming the p type

semiconductor in that case this is also 0. So, what is left is only this and we assume the total ionization of the acceptor atoms which means that this $\rho(x,y)$ is equal to $-qN_A$, because this qN_A^- is equal to qN_A.

So, the right hand side becomes $\delta^2\Psi/\delta x^2 + \delta^2\Psi/\delta y^2$ is equal to qN_A/ϵ_S and we will also do a parallel analysis of the 1D electrostatics, just to see the difference that arises due to the 2D electrostatics.

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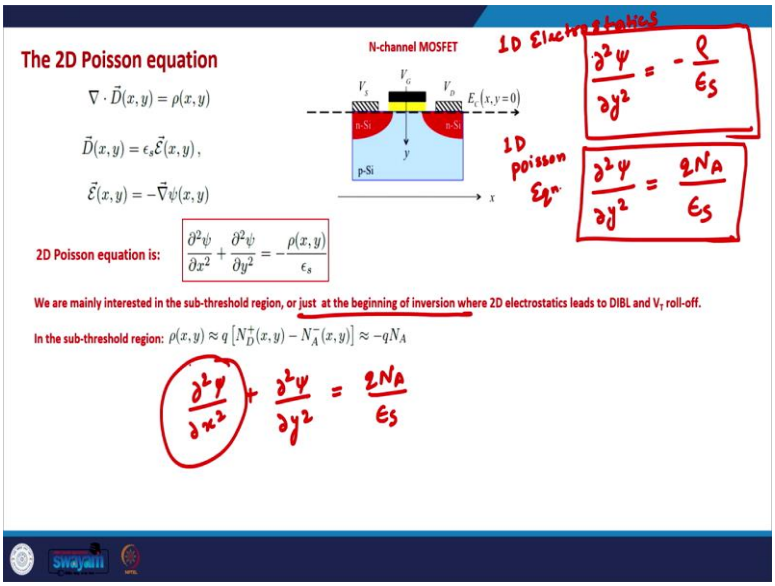

So, in similarly in the 1D electrostatics just at the onset of the inversion this Poisson equation will look like this.

$\delta^2\Psi/\delta y^2$ is equal to qN_A/ϵ_S. So, this is the 1D electrostatics or 1D Poisson equation and this is the 2D Poisson equation. Now, as you can see that the right hand side is the same in both cases, there is a change in the left hand side in 2D Poisson equation in addition to $\delta^2\Psi/\delta y^2$ we also need to consider $\delta^2\Psi/\delta x^2$.

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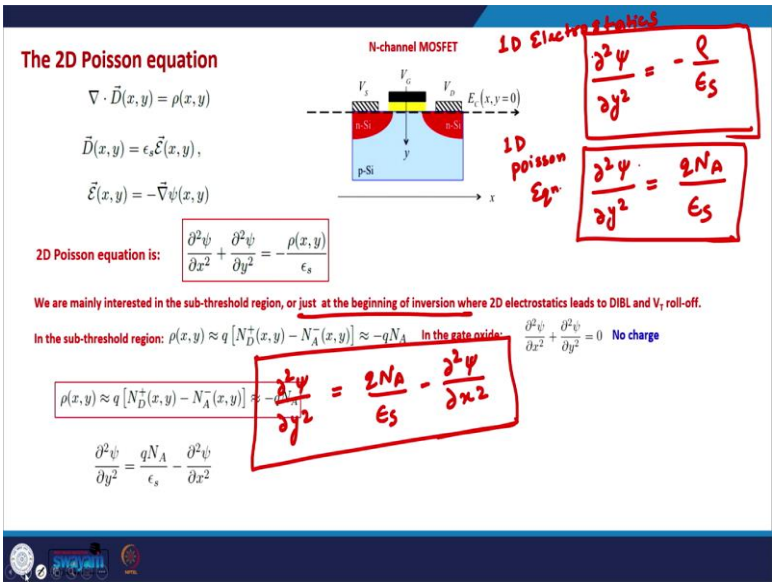

So, what that amounts to is that we can take this term to the right side, $\delta^2\Psi/\delta x^2$ and the left-hand side of this equation is exactly same as the left-hand side of the 1D Poisson equation. So, this 1D analysis is the analysis that we have already done so far in our discussion of electrostatics.

And if we consider the 2D electrostatics because of the small channel in that case this Poisson equation can be written as $\delta^2\Psi/\delta y^2$ is equal to qN_A/ϵ_S - $\delta^2\Psi/\delta x^2$. So, there is a small difference between this 1D Poisson treatment and this 2D Poisson equation ok.

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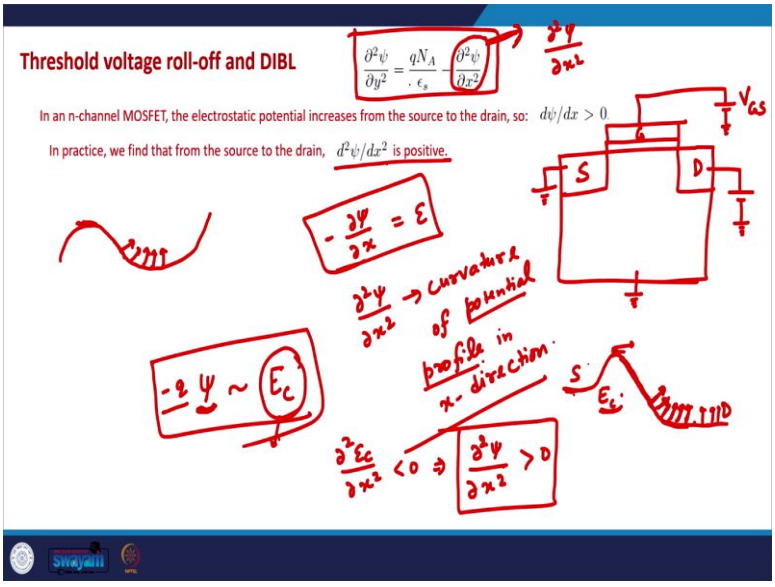

So, ultimately this is the equation that we have in 2D Poisson equation. And so, now, what is this term; let us try to sort of make sense of this term, $\delta^2\Psi/\ \delta x^2$.

Let us draw a picture of the MOSFET, this is how the MOSFET looks like and since we are considering the 2D electrostatics in that case we are assuming that we have applied a voltage on the drain terminal, in addition to a voltage on the gate terminal. The source is assumed to be grounded, the body is also assumed to be grounded psi is the electrostatic potential in the semiconductor.

The first derivative of the Ψ, $\delta\Psi/\delta x$ and negative of that is the electric field and $\delta^2\Psi/\ \delta x^2$ is the curvature of the potential profile in x direction in x direction. So, we need to see what is the curvature of the potential profile in x direction in order to understand this term and please also remember that the Ψ electrostatic potential is also closely related to the conduction band edges and it has a negative relationship.

Because the conduction band edge or the valence band edge or the bands in the semiconductor they essentially represent the potential energy of the electrons and the potential energy is equal to minus q times the electrostatic potential. So, this E_C and Ψ has a negative relationship ok. So, in order to understand the curvature of the potential profile, we will see the curvature of the bands in the semiconductor.

So, and we are familiar with the bands because the bands we have seen many times now. So, this is how the barrier actually looks like in the semiconductor when we apply a certain drain voltage. So, this is the top of the barrier, this is where actually we think that the source is located. So, this is also known as the virtual source point of the device, because this is the point where the gradient of the band is 0 which means that the electric field is 0.

So, the velocity at this point is extremely important we have already seen that is known as the unidirectional thermal velocity, also the known as the injection velocity. So, after this point what we see is that the curvature here is the curvature of this plot is 0 here, but the curvature is becomes negative here. If you see the curvature at these points are negative and here again it is 0.

So, along the channel the curvature is either 0 or negative and this is the curvature of the conduction band edge because in order to understand the barrier generally we plot the

conduction band edge in the device from the source to the drain side. So, it means that the curvature of the conduction band is negative if you are not familiar with the notion of the curvature generally what happens is if this there is a plot like this the curvature is positive.

Because the say if we do the second derivative it turns out to be a positive value and you know this kind of relationship the curvature at these points is negative. In the channel actually the things are assumed to be starting or the electron injection is assumed to be starting from this point and this point onwards the curvature is negative for this conduction band edge. So, the curvature of E_C which means $\delta^2 E_C / \delta x^2$ is a negative number.

Which means $\delta^2 \Psi / \delta x^2$ will be a positive number because they are negatively related to each other. So, that is the key point here, that in a MOSFET $\delta^2 \Psi / \delta x^2$ is a positive quantity and the 2D Poisson equation which looks like this.

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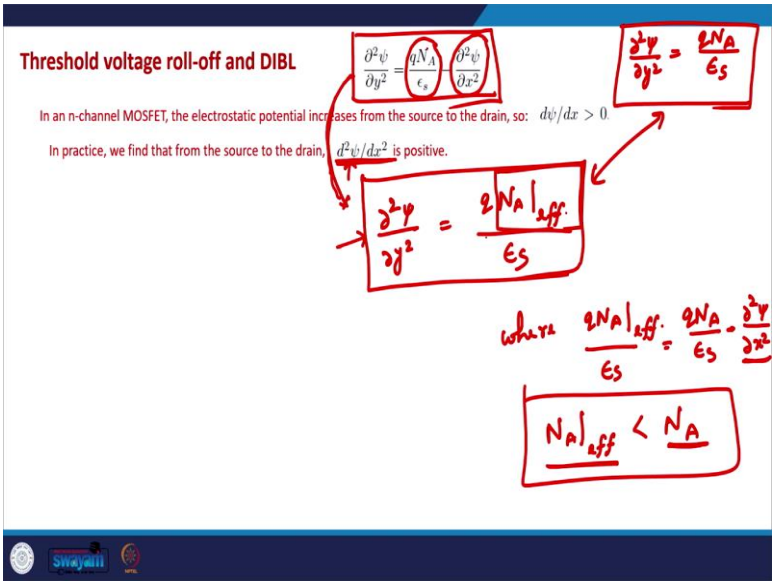

Now, if we compare this to the 1D Poisson equation, $\delta^2 \Psi / \delta y^2$ which is qN_A / ϵ_S.

In addition to so in the 2D electrostatics in addition to this factor of qN_A / ϵ_S we also have a positive quantity $\delta^2 \Psi / \delta x^2$. So, which means that now we or what we can do is we can write this down as $qN_{A\text{-effective}} / \epsilon_S$, where $qN_{A\text{-effective}} / \epsilon_S$ is equal to qN_A / ϵ_S this value $-\delta^2 \Psi / \delta x^2$ and what we have just seen is that this is a positive quantity.

So, this $N_{A\text{-effective}}$ is actually less than N_A. So, this $N_{A\text{-effective}}$ is the effective doping of the semiconductor when we consider the 2D electrostatics ok. So, what it means is, what we can say is if this term is dominant $\delta^2\Psi/\ \delta x^2$ in that case we can write down the 2D Poisson equation just like a 1D Poisson equation. And hence, all the things that we derived for 1D Poisson equation can be used here as well.

But now instead of N_A, we need to consider $N_{A\text{-effective}}$ which is a smaller number than N_A. So, what it means is that the 2D electrostatics effectively reduces the doping of the semiconductor. So, what it means is that now in all the expressions that we have seen for semiconductor for the threshold voltage for the depletion width we need to replace N_A by $N_{A\text{-effective}}$. So, that is the impact of the 2D electrostatics ok.

And now this $N_{A\text{-effective}}$ is smaller than N_A. So, I will give you this small sort of homework assignment to look how various parameters will change while considering the 2D electrostatics. So, how the depletion width will change, how the depletion charge will change how the threshold voltage will change while we consider the 2D electrostatics or this term $\delta^2\Psi/\ \delta x^2$ is significant.

When this is significant how does all those things change, because what we have seen is that the 2D Poisson equation can be converted to just like or converted to a 1D Poisson equation like this. What we just need to do is we need to replace N_A by $N_{A\text{-effective}}$ in all the expressions, that we derived for the 1D Poisson equation. So, just please go back and look into how things change and that is what we will discuss in the coming class. So, thank you for attending this lecture see you in the next class.

Thank you.