

**Physics of Nanoscale Devices**  
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**Lecture - 52**  
**MOSFET Electrostatics, Threshold Voltage**

Hello everyone. Today we will continue the discussion on MOSFET Electrostatics and we will come across a new idea or we will formally discuss the idea of Threshold Voltage, which is I guess most of us know about threshold voltage, but this is not yet mathematically discussed. So, let us quickly review what we have seen.

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**Review**

$I_{DS} = W |Q_n(V_{GS}, V_{DS})| (v)$

$\nabla \cdot \vec{D}(x, y, z) = \rho(x, y, z)$

$\nabla^2 \psi(x, y, z) = -\frac{\rho(x, y, z)}{\epsilon_s}$

**Depletion Region**

**Inversion Region**

**Qualitative - potential profile (band bending)**

$Q_D \propto \sqrt{\psi_S}$ ,  $Q_n \propto \sqrt{\psi_S}^{1.5}$

$\psi_S = \frac{1}{2} \epsilon_s W_D^2$

$Q_D \approx -\sqrt{2qN_A \epsilon_s \psi_S}$

$W_D = \sqrt{\frac{2\epsilon_s \psi_S}{qN_A}}$

$Q_S = Q_D + Q_n$

$Q_n = -q \int_0^{\infty} n(y) dy = -q n(0) t_{inv}$

$n(0) = \frac{n_i^2}{N_A} e^{q\psi_S/k_B T}$

$t_{inv} = \frac{k_B T/q}{\epsilon_{ox}}$

$Q_n(\psi_S) = -q \left[ \frac{n_i^2}{N_A} e^{q\psi_S/k_B T} \right] \left[ \frac{k_B T/q}{\epsilon_{ox}} \right]$

$Q_p = q / N_A \dots$

In the MOSFET electrostatics, in generally in conventional MOSFETs we only do electrostatics in one direction which is the y direction along the direction from the gate to the body, gate to the substrate. Because in the long channel MOSFETs generally the electric field in along the direction of the channel is low and the electric field in the perpendicular direction which is the direction from the gate to the body is generally high.

So, generally that is how that is why this is the typical typically only 1D electrostatics suffice for conventional MOSFETs, but as you will see in coming classes that in the short MOSFETs the electric field in the other direction is not so low and that is why we also need to consider the electric field in the source-drain direction and we need to deal with the 2D electrostatics in the short MOSFETs.

But that is for the later on. And these are the key points of the electrostatics discussion and I hope these things are clear to all of you. This is the way the bands are visualized in when we apply various kind of gate voltages and when the gate voltage is a positive value it leads to the depletion in the P type semiconductor, it leads to the depletion of holes in the semiconductor.

And if this becomes even more positive, the gate voltage becomes even more positive in that case it leads to inversion. So, in the depletion region, which means that there is a positive gate voltage, but still the inversion is not there, the inversion charge is not there in that case, the this  $\Psi_S$  which is the surface potential of the semiconductor is related to the depletion width and the electric field at the surface. The charge is given by this expression, and the depletion width is given by this expression.

And in the last class we saw that, in the inversion region in addition to the depletion charge there is also this mobile charge or also what is known as the inversion charge, and the inversion charge is calculated by integrating the electron density in the semiconductor along y direction, the electron density comes from the fundamental carrier statistics of the semiconductor from this relationship.

And finally, what we see is that this inversion charge can be represented in this expression or it can in short be written like this. Now, there are there is an important observation that we need to make here. The observation is that the depletion charge is related to  $\Psi_S$  in this way. So, the  $Q_D$  charge is directly proportional to the square root of  $\Psi_S$ , but the inversion charge is exponentially related to the  $\Psi_S$  which is the surface potential.

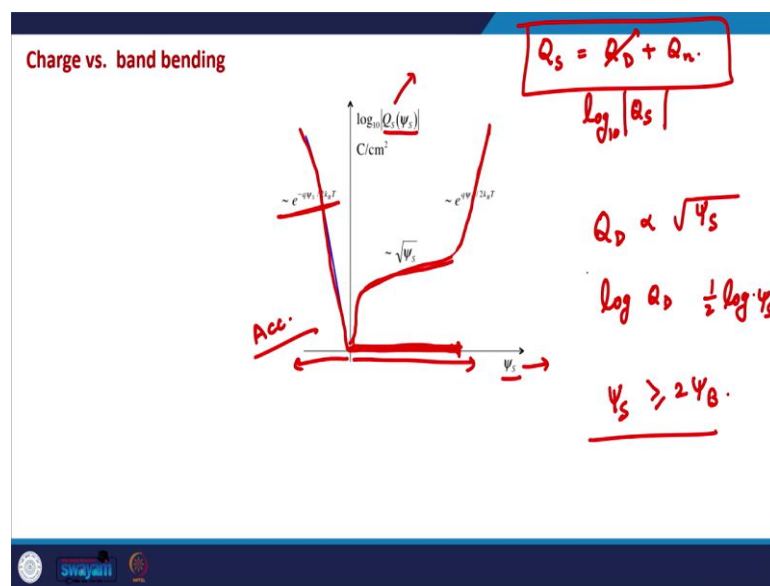
So, this  $Q_n$  is exponentially related to the surface potential and there is there are other factors as well here, and that is the key difference here. So, what it means is that, for the low positive gate voltages when the inversion has not yet happened and the only the depletion charge is there in that case the charge will vary according to this relationship.

But as soon as there is strong inversion in the semiconductor the this the inversion charge or the charge in the semiconductor increases exponentially. Now, you might think what would be the charge in the accumulation region and just to quickly remind you the accumulation region is the region, when a negative gate voltage is applied which means

that now the holes are accumulated in the semiconductor and essentially that is given by this relationship.

So, the accumulation charge which will be a positive charge is given by  $q$  times  $\int N_A \exp(-q\Psi(y)/kT)dy$  and this  $\Psi$  is negative because a negative gate voltage is there which results in a negative surface potential. So, this  $\Psi(y)$  will be negative and this integration needs to be done in  $y$  direction. So, even this accumulation charge is also exponentially related.

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So, just to summarize all these various regimes, we can what we can do is we can plot a relationship between the semiconductor charge and the surface potential. So, the semiconductor charge  $Q_s$  is if you recall is the summation of depletion charge plus inversion charge, and in order to properly understand this we plot the log of the log 10 of  $Q_s$  take a mod as well we generally take a mod.

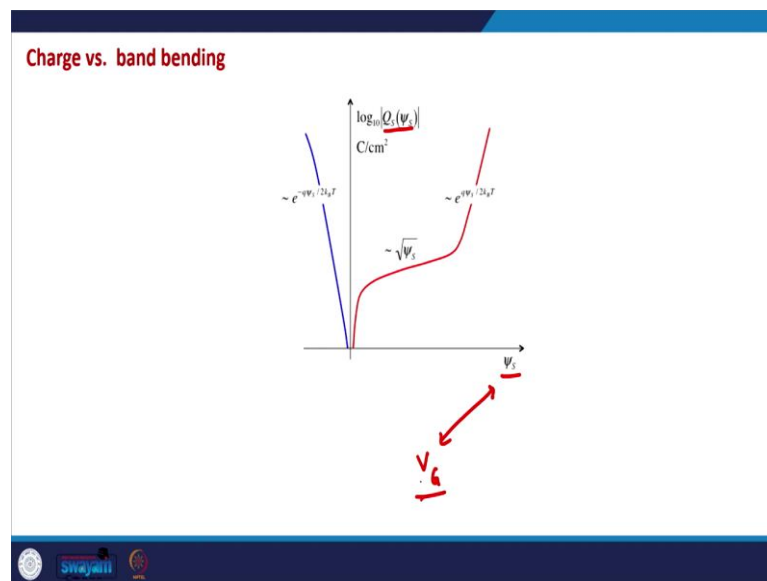
Because this  $Q_s$  is negative sometimes, but to try to understand how the semiconductor charge depends on the surface potential, we generally take we generally plot the log of mod of  $Q_s$  versus  $\Psi_s$  and this region when  $\Psi_s$  is negative is the accumulation region because the negative gate voltage is there which is resulting in the negative surface potential.

And in that region this  $Q_S$  will be only this depletion charge will be 0 and the only charge that will be there will be the mobile charge, and that will be exponentially related to the surface potential. So, that is why we see as exponential dependence of  $Q_S$  in the accumulation. In this in the positive half when  $\Psi_S$  is positive initially there is the depletion of holes and the inversion charge is very less and in that case this  $Q_n$  is negligible as compared to  $Q_D$  and the only charge that is there is just the  $Q_D$  charge.

And the  $Q_D$  charge as all of us know, the  $Q_D$  charge is related to  $\Psi_S$  in this way ok. So, which means that this log of  $Q_D$  will be  $1/2 \log \Psi_S$ . So, that is why there is this slow dependence of the semiconductor charge as a function on  $\Psi_S$  in the for the low values of  $\Psi_S$ , but as soon as the inversion starts which means that now the  $\Psi_S$  is greater than or equal to  $2 \Psi_B$ , in that case, this charge which is the mobile charge, this  $Q_n$  charge starts dominating and it starts becoming more than the  $Q_D$  charge.

So, this  $Q_D$  becomes negligible as compared to  $Q_n$  and again this  $Q_n$  has exponential dependence on  $\Psi_S$ . So, again this plot of  $Q_S$  versus  $\Psi_S$  follows the exponential path. So, this is I would say, in MOSFET electrostatics this is an important observation; how the MOSFET charge or how the semiconductor charge which is essentially the charge in the channel region of the semiconductor varies as a function of  $\Psi_S$ .

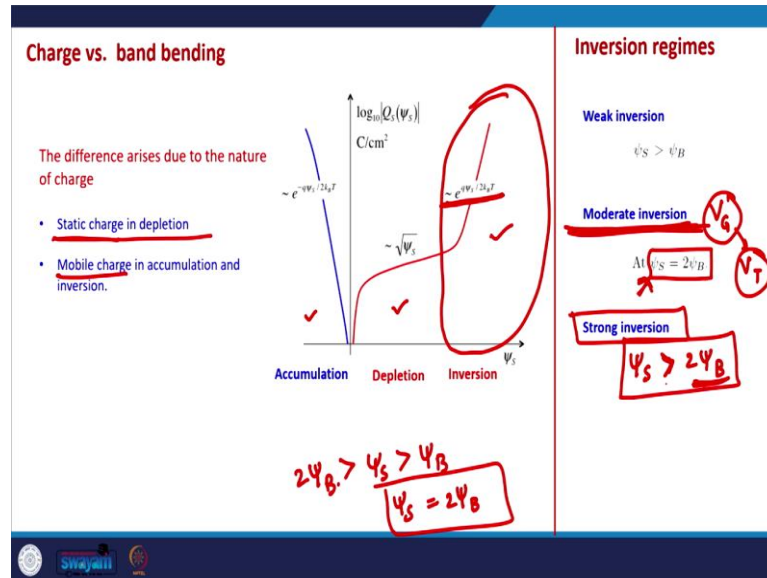
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So, now we have seen the dependence between  $Q_S$  and  $\Psi_S$ , but actually the free variable in our hands is  $V_G$ .  $V_G$  means, the gate voltage that is what we can change externally. So,

we would also like to see a relationship between  $V_G$  and  $\Psi_S$  because that way we will properly understand the relationship between  $Q_S$  and  $V_G$ . So, that will be our next discussion, and from there this idea of threshold voltage will come about.

(Refer Slide Time: 09:37)



But before going into that discussion, let us have a quick sort of review or let us quickly recall what happens in various regimes. So, these are the various regimes and so, this is the accumulation, this is depletion and this is the inversion regime. And as we know that in the depletion region, the charge the major charge is the static charge, in the accumulation and the inversion region we have the mobile charge dominating the semiconductor charge.

And so, this is an important point here, because even in there is a difference in the nature of charges various charges and if we just focus on the inversion regime, because that is the most important regime for operation of the MOSFETs. There is this weak inversion, weak inversion is when the semiconductor is slightly n type at the interface which means that  $\Psi_S$  is greater than  $\Psi_B$ , but it is less than  $2\Psi_B$ .

So, in this regime, even in the weak regime, the mobile charges is very less and the total charge in the semiconductor is dominated by the depletion charge or the static charge. The moderate inversion is the inversion, or it happens when  $\Psi_S$  is equal to twice of  $\Psi_B$ . So, this is known as the moderate inversion and this is also the defining point for the

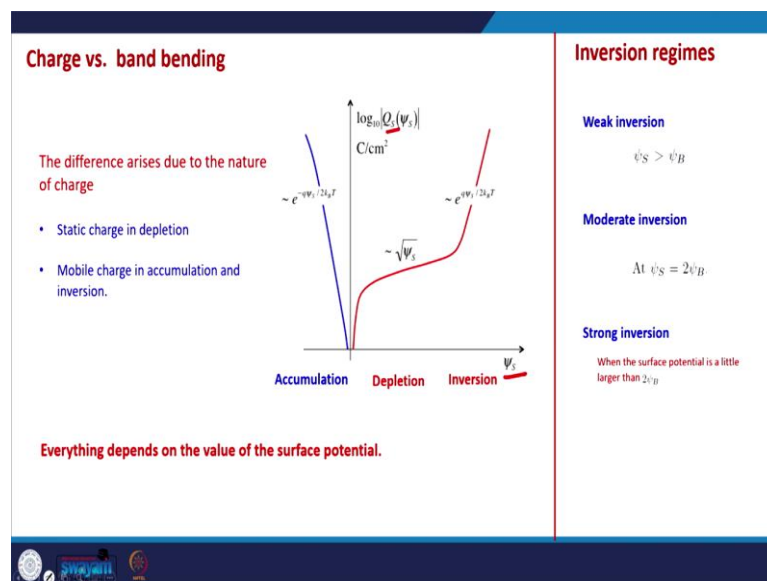
threshold voltage because the voltage at which  $\Psi_S$  becomes  $2 \Psi_B$  is defined as the threshold voltage.

So, the gate voltage at which  $\Psi_S$  becomes equal to  $2 \Psi_B$  is known as the threshold voltage. But even at this point, the mobile charge or the inversion charge is still not too much, it is still it is just comparable to the depletion charge at the interface per unit area. So, that is why it is known as the moderate the inversion, because even at the at this point the depletion charge is quite significant in the semiconductor and at the interface the mobile charge is just equal to the depletion charge per unit area.

And the strong inversion happens when  $\Psi_S$  is slightly more than  $2 \Psi_B$  and at this point if we if you recall this inversion charge increases exponentially, and so it suddenly dominates the semiconductor charge. The semiconductor charge can be assumed to be entirely the mobile charge in the strong inversion regime.

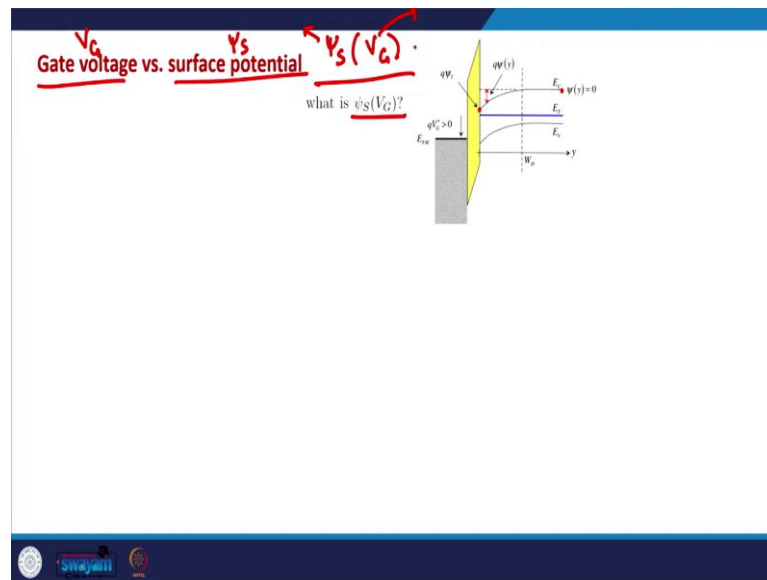
So, generally the MOSFETs are operated not exactly at  $\Psi_S$  is equal to  $2 \Psi_B$ , they are operated slightly above a few  $kT$  values above the  $2\Psi_B$  surface potential and this is known as the strong inversion regime. So, please try to understand these intricacies of the inversion regimes as well. We will not spend too much of a time here, because this is all part of the conventional electrostatics theory of MOSFETs.

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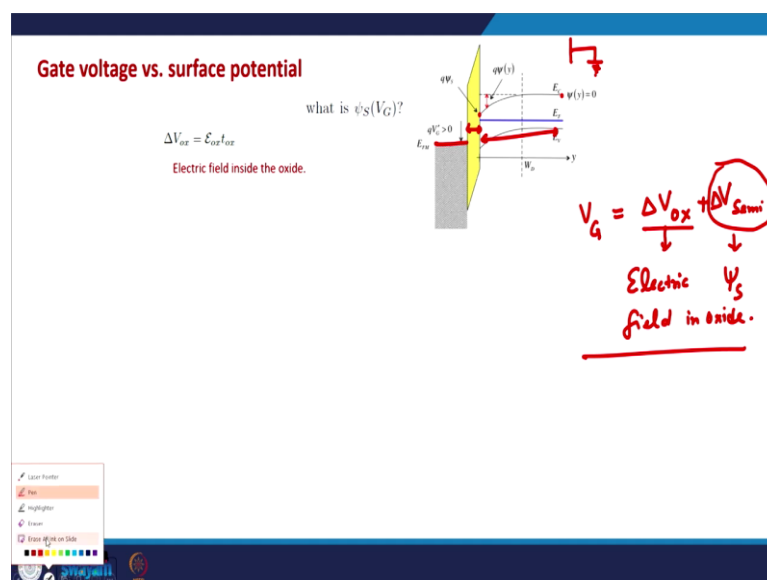
So, now we understand the relationship between  $Q_S$  and  $\Psi_S$ .

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Now onwards we will try to see the relationship between  $\Psi_S$  the surface potential and  $V_G$  because  $V_G$  is the voltage that is in our hands. So, to start with what is that we are trying to find out? We are trying to find out a relationship between  $\Psi_S$  and  $V_G$  or we are trying to see how  $\Psi_S$  is a function of  $V_G$ , because  $V_G$  is the independent variable,  $\Psi_S$  is the dependent variable;  $\Psi_S$  depends on the applied  $V_G$ .

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So, the one way to understand this is that, the voltage that we apply on the gate terminal is dropped in the oxide and in the semiconductor ok. So, the gate; because deep inside

the semiconductor or at the other terminal, then we generally ground the body contact. So, the gate voltage can be written as the voltage drop inside semiconductor and the voltage drop in the oxide. What is the voltage drop in the semiconductor?

The voltage drop in the semiconductor is essentially  $\Psi_s$ . Because  $\Psi_s$  is the electrical potential at the surface and deep inside it is 0. So, the total voltage drop is  $\Psi_s$ . But what is the voltage drop in the oxide? So, that will be given by the electric field in the oxide ok. So, that is an important point again here.

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**Gate voltage vs. surface potential**

what is  $\psi_s(V_G)$ ?

$\Delta V_{ox} = \epsilon_{ox} t_{ox}$   
Electric field inside the oxide.

$\epsilon_{ox} \epsilon_{ox} = -Q_s(\psi_s)$

$\Delta V_{ox} = -\frac{Q_s(\psi_s)}{C_{ox}}$

From Gauss's law:  
 $\oint \mathbf{E} \cdot d\mathbf{A} = \frac{Q}{\epsilon_0}$

$\epsilon_{ox} \cdot \epsilon_{ox} = -Q_s(\psi_s)$

$\epsilon_{ox} = -\frac{Q_s}{\epsilon_{ox}}$

$\Delta V_{ox} = \epsilon_{ox} \cdot t_{ox} = -\frac{Q_s \cdot t_{ox}}{\epsilon_{ox}} = -\frac{Q_s}{C_{ox}}$

$C_{ox} = \frac{\epsilon}{t}$

That in order to understand the relationship between  $V_G$  and  $\Psi_s$  we need to understand what is the voltage drop in the oxide and that depends on the electric field in the oxide. And in order to find out the electric field in the oxide we use the Gauss's Law. And what does the Gauss law says?

The Gauss law says that inside a closed surface, the surface integral of the electric field is given by the total charge enclosed in that surface divided by the permittivity of that medium essentially. So, with this, what we can say that or what we can say is that  $\epsilon_{ox}$  times electric field in the semi in the oxide is  $-Q_s$ , because where  $Q_s$  is the charge in the semiconductor.

Because if we and most of the charge in the semiconductor we assume that it drops very close to the interface, and by using the Gauss's law we can write down this. We are



assuming that there is no interface charge in the semiconductor. So, that is why this is what we can write down. This  $Q_S$  is the charge per unit area and it depends on the surface potential as well.

So,  $E_{OX}$  is essentially  $-Q_S/\epsilon_{OX}$ , where  $\epsilon_{OX}$  is the dielectric constant of the oxide or the permittivity of the oxide, and that is why the voltage drop in the oxide is which is essentially  $E_{OX}$  times  $t_{OX}$  is  $-Q_S$  divided by or  $Q_S$  times  $t_{OX}/\epsilon_{OX}$  or it can be written as  $-Q_S/C_{OX}$  where  $C_{OX}$  is the capacitance of the oxide.

And the capacitance per unit area of any material is given by this, total capacitance is just multiplication of area to this constant, but if we want to find out the capacitance per unit area it is just  $\epsilon/t$  ok. So, this  $\Delta V_{OX}$  finally, is  $-Q_S/C_{OX}$ .

(Refer Slide Time: 17:43)

**Gate voltage vs. surface potential**

what is  $\psi_S(V_G)$ ?

$\Delta V_{ox} = \epsilon_{ox} E_{ox}$

Electric field inside the oxide.

$\epsilon_{ox} E_{ox} = -Q_S(\psi_S)$

From Gauss's law:  $\int E \cdot dA = Q/\epsilon_0$

$\Delta V_{ox} = -\frac{Q_S(\psi_S)}{C_{ox}}$

$V'_G = -\frac{Q_S(\psi_S)}{C_{ox}} + \psi_S$

When Fermi levels are not aligned

$qV_{FB} = (\phi_M - \phi_S) = \phi_{MS}$

$qV_{FB} = \phi_m - \phi_s = \phi_{ms}$

And so, that is why the gate voltage the total gate voltage is  $\Delta V_{OX}$  which is  $-Q_S/C_{OX} + \Psi_S$  which is the voltage that drops inside the semiconductor. And please note it down here that we have written a prime on  $V'_G$ . What does the prime means here?

The prime means that this is this may not be the actual gate voltage, this is a modified gate voltage because in most of the cases the Fermi level of the metal and the Fermi level of the semiconductor they may not be aligned with each other in 0 bias condition. So, there might be a work function difference between the metal and the semiconductor, also

there might be some surface charges, there might be some static charge at the interface between the oxide and the semiconductor.

So, these charges come because of the fabrication, because of the imperfect fabrication and these are in most of the cases unavoidable. So, this is in a way this  $V_G'$  prime is the modified gate voltage which essentially takes into account the effect of the flat band or I would say the work function difference and the surface charges.

Let me sort of quickly do that here as well. So, when in no bias condition when there is a work function difference between the metal between the gate and the semiconductor which means. So, in this example we have shown that  $\phi$  those work function of the metal is less than the work function of the semiconductor. So, in that case what happens is when this MOS structure is formed in that case, there will be a band bending even at 0 gate voltage. So, this will be the case when these will be joined.

Because at 0  $V_G$  value, the Fermi levels need to be aligned and in order to align the Fermi levels, the conduction band and the valence band extremas will bend. So, this is the case with no applied voltage on the gate terminal when there is a work function difference. And in order to neutralize this band bending we need to apply  $V_{FB}$  voltage on the gate terminal and this  $V_{FB}$  is given by,  $V_{FB}$  is  $1/q$  times  $(\Phi_M - \Phi_S)$ , or  $\Phi_{MS}$ .

So, when we apply this voltage on the gate terminal, this bend bending is neutralized and in that case the flat bands are achieved. So, that is why this gate voltage is known as the flat band voltage.

(Refer Slide Time: 21:12)

**Gate voltage vs. surface potential**

$V_G = V_G' + V_{FB}$

$\Delta V_{ox} = \epsilon_{ox} t_{ox}$   
Electric field inside the oxide.

$\epsilon_{ox} \mathcal{E}_{ox} = -Q_S(\psi_S)$

$\Delta V_{ox} = -\frac{Q_S(\psi_S)}{C_{ox}}$

$V_G' = \frac{Q_S(\psi_S)}{C_{ox}} + \psi_S$

what is  $\psi_S(V_G)$ ?

From Gauss's law:  $\int \mathbf{E} \cdot d\mathbf{A} = Q/\epsilon_0$

When Fermi levels are not aligned:  $qV_{FB} = (\Phi_M - \Phi_S) = \Phi_{MS}$

When there is a fixed charge at the interface:  $\epsilon_{ox} \mathcal{E}_{ox} = -Q_S(\psi_S) - Q_F$

In case of both:  $V_{FB} = \frac{\Phi_{MS}}{q} - \frac{Q_F}{C_{ox}}$

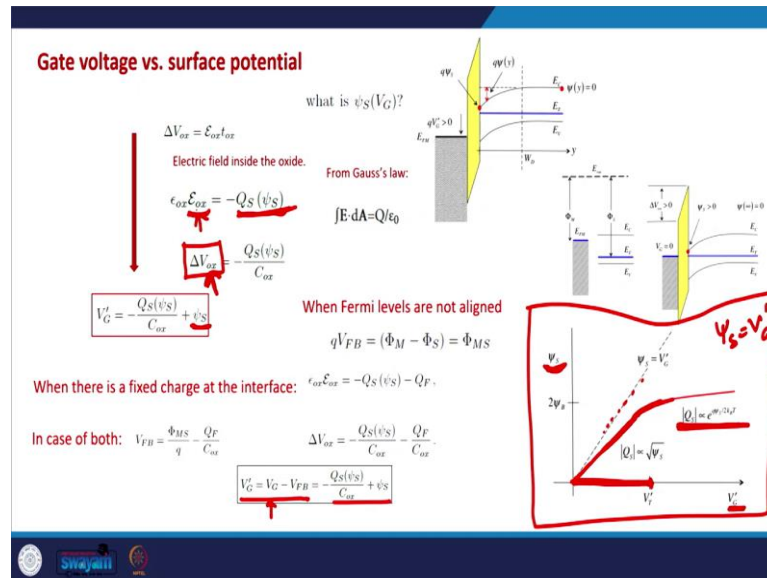
$\Delta V_{ox} = -\frac{Q_S(\psi_S)}{C_{ox}} - \frac{Q_F}{C_{ox}}$

So, in all those materials in which the metal Fermi level and the semiconductor Fermi levels are not aligned in that case we in addition to these voltages the voltage drop in the semiconductor and in the oxide, we also need to account for the flat band voltage. Also if there is a fixed charge at the interface because of the fabrication because of various conditions, we also need to account for  $Q_F$  while calculating the electric field in the oxide and not only  $Q_S$  we also need to account for  $Q_F$  in this calculation.

So, that is why this  $\Delta V_{OX}$  becomes  $-Q_S/C_{OX} - Q_F/C_{OX}$ . So, in total we need to generally this quantity is absorbed in the flat band voltage and this flat band voltage is written as  $\Phi_{MS}/q - Q_F/C_{OX}$ . So, this is the additional voltage that we need to apply on the gate terminal in order to achieve the perfect or ideal conditions that we have been discussing so far.

So, apart from this voltage we need to account for the flat band voltage in the semiconductor and that will. So,  $V_G$  the actual gate voltage will be  $V_G' + V_{FB}$  ok.

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So, or  $V_G'$  is  $V_G - V_{FB}$  and this is given by this value. So, now, this is the relationship between  $\Psi_S$  and  $V_G'$ . So, this is a complex relationship I would say this  $V_G'$  and  $\Psi_S$  they are related to each other. Because this  $Q_S$  which includes the static charge and the depletion charge and the inversion charge this is a complex quantity, and then we have this  $\Psi_S$  term as well.

So, analytically it is not straight forward to do this calculation to exactly figure out a relationship between  $\Psi_S$  and  $V_G'$ , but we can qualitatively understand this relationship from this plot. And what this plot says is that, when the gate voltage is below the threshold voltage or in other words the MOSFET is operating in the depletion region.

So, the most of the charge in the material or most of the charges because of the depletion charge, in that case the  $\Psi_S$  the surface potential or the semiconductor potential almost follows the gate voltage. So, which means that so, this dotted line if you see is the line of  $\Psi_S$  is equal to  $V_G'$ .

And in the sub threshold regime when  $V_G'$  is less than  $V_T'$  in that case, the actual relationship between  $\Psi_S$  and  $V_G'$  is quite close to this line. So, which means that the  $\Psi_S$  value this the semiconductor potential follows closely the gate voltage.

And the reason for that is that the semiconductor charge in this region is less because it is only because of the depletion charge, and that is why this electric field in the oxide is

less because it depends on the semiconductor charge and that is why the voltage drop in the oxide is also less. So, which means that, most of the voltage drops in the semiconductor. So, below threshold most of the voltage drops in the semiconductor and  $\Psi_S$  is closely following the  $V_G'$ .

But as soon as the inversion starts which is exactly at this point when  $V_G'$  is equal to  $V_T'$ , in that case the semiconductor charge is exponentially dependent on  $\Psi_S$ . Which means that the semiconductor charge increases abruptly and that also increases the electric field in the oxide also the voltage drop in the oxide. So, after the inversion has started after the strong inversion, there is a huge charge buildup in the semiconductor that leads to a huge voltage drop in the oxide.

And this  $\Psi_S$  actually deviates this goes away from the this plot this line, which means that after the inversion  $\Psi_S$  does not follow the gate voltage it departs away from the gate voltage. Because even a slight increase in the gate voltage results in a huge increase in the semiconductor charge and as a consequence a huge increase in the voltage drop in the oxide.

So, that is the qualitative I would say picture of the relationship between  $\Psi_S$  and  $V_G'$ . So, in the beginning of this lecture, we have seen a relationship between  $Q_S$  and  $\Psi_S$ , here we have seen a relationship between  $\Psi_S$  and  $V_G'$  and  $V_G'$  is related to  $V_G$  by this relationship  $V_G' = V_G - V_{FB}$ .

So, essentially the same kind of relationship will be there between  $\Psi_S$  and  $V_G$ . So, before inversion and after inversion this changes is noticeable change and this needs to be kept in mind while understanding the surface potential in the semiconductors ok.

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### Gate voltage vs. surface potential

what is  $\psi_S(V_G)$ ?

$\Delta V_{ox} = \epsilon_{ox} E_{ox}$   
Electric field inside the oxide.  
 $\epsilon_{ox} E_{ox} = -Q_S(\psi_S)$   
 $\Delta V_{ox} = -\frac{Q_S(\psi_S)}{C_{ox}}$

From Gauss's law:  
 $\int \mathbf{E} \cdot d\mathbf{A} = Q/\epsilon_0$

When Fermi levels are not aligned  
 $qV_{FB} = (\Phi_M - \Phi_S) = \Phi_{MS}$

When there is a fixed charge at the interface:  
 $\epsilon_{ox} E_{ox} = -Q_S(\psi_S) - Q_F$

In case of both:  $V_{FB} = \frac{\Phi_{MS}}{q} - \frac{Q_F}{C_{ox}}$   
 $\Delta V_{ox} = -\frac{Q_S(\psi_S)}{C_{ox}} - \frac{Q_F}{C_{ox}}$

$V_G = V_G - V_{FB} = -\frac{Q_S(\psi_S)}{C_{ox}} + \psi_S$   
 $\Rightarrow V_G = V_{FB} - \frac{Q_S}{C_{ox}} + \psi_S$

Work functions are the energies required to move an electron from the Fermi level to the vacuum.

Qualitative shape of  $\psi_S$  vs.  $V_G$

M. Lundstrom, "Fundamentals of Nanotransistors", World Scientific Publishing Company, 2018

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### Threshold voltage

Gate voltage needed to bend the bands so that:  $\psi_S = 2\psi_B$

$Q_S(2\psi_B) \approx Q_D(2\psi_B)$

$V_T = V_{FB} - \frac{Q_D(2\psi_B)}{C_{ox}} + 2\psi_B$       $V_T = V_{FB} - \frac{Q_S(2\psi_B)}{C_{ox}} + 2\psi_B$

$V_T = V_{FB} + \frac{\sqrt{2qN_A \epsilon_s} (2\psi_B)}{C_{ox}} + 2\psi_B$

$Q_D = -\sqrt{2qN_A \epsilon_s} \psi_S$

Swajati

So, now let us move on to see, what happens or what is the threshold voltage. So, as we know that the threshold voltage is the gate voltage needed to bend the bands so that  $\Psi_S$  is equal to  $2\Psi_B$ . This definition now we have seen multiple times, we just need a mathematical form to this definition. And from this expression on the last slide this expression which is essentially  $V_G$  is equal to  $V_{FB} - Q_S/C_{OX} + \Psi_S$ , using this definition we will replace  $V_G$  by  $V_T$  when  $\Psi_S$  is  $2\Psi_B$ .

So, in this case what happens is  $V_T$  is equal to  $V_{FB} - Q_S(@ \Psi^S = 2\Psi^B) / C_{OX} + 2\Psi_B$ . So, we have replaced  $\Psi_S$  by  $2\Psi_B$ . And this is as I told you that this is the moderate inversion and even in this inversion, what we can assume is that the semiconductor charge is almost equal to the depletion charge the inversion charge is still not. So, significant.

So, this  $Q_S$  formula can be replaced by  $Q_D$  and this  $Q_D$  is related to  $\Psi_S$  if you recall  $Q_D$  is  $\sqrt{(2qN_A\epsilon_S\Psi_S)}$ . So, in this expression we need to replace  $\Psi_S$  by  $2\Psi_B$ . So, that way we will find out the expression for the threshold voltage. So, the threshold voltage is the flat band voltage plus  $\sqrt{(2qN_A\epsilon_S \cdot 2\Psi_B)} / C_{OX} + 2\Psi_B$ .

So, this is the, this is one of the most frequently used expressions in the MOSFET electrostatics because this gives us the threshold voltage of a given MOSFET.

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**Threshold voltage**

Gate voltage needed to bend the bands so that:  $\psi_s = 2\psi_B$

$Q_S(2\psi_B) \approx Q_D(2\psi_B)$       $V_T = V_{FB} - \frac{Q_D(2\psi_B)}{C_{ox}} + 2\psi_B$       $V_T = V_{FB} - \frac{Q_S(2\psi_B)}{C_{ox}} + 2\psi_B$

$V_T = V_{FB} + \frac{\sqrt{2qN_A\epsilon_S(2\psi_B)}}{C_{ox}} + 2\psi_B$

**Gate capacitance**

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_S}$

$C_G(inv) \approx C_{ox}$

$C_G(acc) \approx C_{ox}$

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_S}$  → Semi conductive capacitance

$C_S = \frac{d(Q_S)}{d\psi_S} = \frac{d(Q_D)}{d\psi_S}$  → Exponential

The slide includes a diagram of a MOSFET cross-section with gate (G), source (S), and drain (D) terminals, and a diagram of a capacitor model with plates A and B, dielectric  $\epsilon_{ox}$ , and semiconductor  $\epsilon_s$ .

Let us quickly try to understand another important topic that is the gate capacitance. The gate capacitance is, essentially the capacitance of as seen from the gate terminal, and as we know that a MOSFET is also has a capacitive element. So, this is the gate terminal, this is the oxide and this is the semiconductor.

In the semiconductor what we have seen is that the charge changes as a function of the applied voltage. So, which means that the semiconductor also has some capacitance in it because whenever the charge is a function of the voltage, then it shows a capacitive

behavior and in that case. So, as seen from the gate terminal we will see the oxide capacitance and the semiconductor capacitance.

So, these are the 2 capacitive elements I would say, one is because of the this oxide which is an insulator and this is like a parallel plate capacitor, and then we have a semiconductor capacitance, but this is a function of the voltage. This capacitance is constant because this is like a parallel plate capacitor and the capacitance just depends on the thickness here.

So, this is the picture here and the total capacitance or this becomes a series of 2 capacitors and the total gate capacitance will be  $1/C_{OX} + 1/C_S$  which is the semiconductor capacitance ok. So, just to give you couple of pointers here in the inversion region, and this what is this  $C_S$ ?  $C_S$  is  $dQ/dV$ . So, always this is how the capacitance is defined the change in charge as a function of the voltage.

And  $C_S$  will be the change in semiconductor charge as a function of the voltage applied which is the semiconductor voltage. So, it instead of  $dV$  it should be  $d\Psi_S$  or  $dV$  let us just write is  $dV_S$  the voltage across the semiconductor which is also the  $\Psi_S$  voltage. And in the accumulation and the inversion regimes as all of us know that this  $Q_S$  is an exponential quantity as a function of  $\Psi_S$ .

So, this is also  $dQ_S$  divided by  $d\Psi_S$ , and  $Q_S$  is exponentially related to  $\Psi_S$ . So, this is also an exponential  $C_S$  is also exponential quantity which means that for a large enough accumulation and in strong inversion this is a huge quantity  $C_S$  the semiconductor capacitance is a huge capacitance and when we have two series capacitance is the total capacitance is actually limited by the smaller capacitance.

Because if  $C_S$  is extremely large then,  $1/C_S$  will be a small number can be all approximately 0 and in that case  $C_G$  will just be equal to  $C_{OX}$ . So, what we can say is that in accumulation and in strong inversion the total gate capacitance is almost equal to the oxide capacitance. However, in the depletion region the semiconductor capacitance is not very large and in that case we need to account for this.



(Refer Slide Time: 33:48)

**Threshold voltage**

Gate voltage needed to bend the bands so that:  $\psi_S = 2\psi_B$

$Q_S(2\psi_B) \approx Q_D(2\psi_B)$       $V_T = V_{FB} - \frac{Q_D(2\psi_B)}{C_{ox}} + 2\psi_B$       $V_T = V_{FB} - \frac{Q_S(2\psi_B)}{C_{ox}} + 2\psi_B$

$V_T = V_{FB} + \frac{\sqrt{2qN_A\epsilon_s(2\psi_B)}}{C_{ox}} + 2\psi_B$

**Gate capacitance**

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_S(\psi_S)}$

$C_G(inv) \approx C_{ox}$

$C_G(acc) \approx C_{ox}$

$\frac{1}{C_G(depl)} = \frac{1}{C_{ox}} + \frac{1}{C_D}$  F/m<sup>2</sup>

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_D}$

So, for that we need to understand that, that in the depletion region the gate capacitance will be derived from this formula, because still we have the two capacitors in series, and the gate capacitance will be dependent on the depletion capacitance of the semiconductor.

(Refer Slide Time: 34:06)

**Threshold voltage**

Gate voltage needed to bend the bands so that:  $\psi_S = 2\psi_B$

$Q_S(2\psi_B) \approx Q_D(2\psi_B)$       $V_T = V_{FB} - \frac{Q_D(2\psi_B)}{C_{ox}} + 2\psi_B$       $V_T = V_{FB} - \frac{Q_S(2\psi_B)}{C_{ox}} + 2\psi_B$

$V_T = V_{FB} + \frac{\sqrt{2qN_A\epsilon_s(2\psi_B)}}{C_{ox}} + 2\psi_B$

**Gate capacitance**

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_S(\psi_S)}$

$C_G(inv) \approx C_{ox}$

$C_G(acc) \approx C_{ox}$

$\frac{1}{C_G(depl)} = \frac{1}{C_{ox}} + \frac{1}{C_D}$  F/m<sup>2</sup>

In depletion regime:  $C_s \approx C_D = \frac{\epsilon_s}{W_D(\psi_S)} = \frac{\epsilon_s}{\sqrt{2\epsilon_s\psi_S/qN_A}} = \frac{\epsilon_s}{\sqrt{2\epsilon_s\psi_S} \sqrt{qN_A}}$

$C_s \approx C_D = \frac{\epsilon_s}{W_D}$

$C_s \approx C_D = \frac{\epsilon_s}{\sqrt{2\epsilon_s\psi_S} \sqrt{qN_A}}$

So, in the depletion region, generally the width of the depletion. So, in the depletion region what we can say that, the capacitance of the semiconductor will just be  $\epsilon_s / W_D$  the depletion width, and the depletion width as a function of  $\Psi_S$  is  $\sqrt{(2\epsilon_s\Psi_S / qN_A)}$ .

So, which means that the depletion capacitance will be  $\sqrt{(\epsilon_{sq}N_A/2\Psi_s)}$ . And in the depletion regime, the mobile charge or the inversion charge is very less. So, the only capacitance that the semiconductor has is the depletion capacitance.

(Refer Slide Time: 35:17)

**Threshold voltage**

Gate voltage needed to bend the bands so that:  $\psi_s = 2\psi_B$

$Q_s(2\psi_B) \approx Q_D(2\psi_B)$       $V_T = V_{FB} - \frac{Q_D(2\psi_B)}{C_{ox}} + 2\psi_B$       $V_T = V_{FB} - \frac{Q_s(2\psi_B)}{C_{ox}} + 2\psi_B$

$V_T = V_{FB} + \frac{\sqrt{2qN_A\epsilon_s(2\psi_B)}}{C_{ox}} + 2\psi_B$

**Gate capacitance**

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_s(\psi_s)}$

$C_G(inv) \approx C_{ox}$

$C_G(acc) \approx C_{ox}$

$\frac{1}{C_G(depl)} = \frac{1}{C_{ox}} + \frac{1}{C_D}$  F/m<sup>2</sup>

**In depletion regime:**

$C_s \approx C_D = \frac{\epsilon_s}{W_D(\psi_s)} = \frac{\epsilon_s}{\sqrt{2\epsilon_s\psi_s/q}N_A}$

The slide also includes a graph of capacitance  $C_G$  versus gate voltage  $V_G'$  showing a peak at threshold voltage, and two cross-sectional diagrams of the MOSFET channel showing charge distribution in accumulation and depletion regimes.

So, the total in that case the total capacitance or the gate capacitance will be just a series combination of the depletion and the oxide capacitance. So, that way we can calculate this  $C_G$  in the depletion region. So, in this way we have seen what is the gate capacitance in various operational regimes of the MOSFET.

Now, in order to understand the relationship of  $C_G$  the gate capacitance on the gate voltage,  $V_G'$  please remember that this is  $V_G'$  because generally this effect of flat band voltage is not considered is not being considered at this point. So, there is a difference in this relationship the relationship between  $C_G$  and  $V_G$  at low frequency and at high frequency.

And what is the difference? At low frequency when we do we apply an ac signal of low frequency what happens is that, in the accumulation nothing changes because if the gate voltage is an ac signal and the semiconductor charge is the holes the majority carriers they can respond to any frequency of the gate voltage, but in the inversion region what happens is that, the gate voltage is a negative voltage.

So, there is a large negative dc voltage and along with this there is a small ac signal as well and in that case what happens is, that if the frequency of the gate voltage is extremely high then the semiconductor charge cannot respond to that frequency. Because the semiconductor charge is made of the minority charge carriers and the minority charge carriers or minority charges the rate of generation is limited by the recombination generation rate.

So, if the frequency is above a few megahertz in that case this inversion charge cannot respond to that frequency and the semiconductor will have only the depletion capacitance and at high frequency as you can see the gate capacitance will be equal to the capacitance in the depletion region.

So, this is the capacitance in the depletion region and this is a cumulative effect of  $C_{OX}$  and  $C_D$ , in the accumulation region the gate capacitance is quite close to the oxide capacitance, but at low frequency when the gate voltage is applied we apply a gate voltage of low frequency in that case the inversion layer can respond to that low frequency and the total gate capacitance is almost again equal to the oxide capacitance.

So, this is a key point here in the gate capacitance, and this needs to be kept in mind while designing various circuits of MOSFETs that at high frequency this charge inversion charge may not respond to the gate voltage. But if we consider the total MOSFET in that case this charge this is the true this is true for MOS device MOS capacitor.

But if we consider the MOSFET in that case what happens is that, this inversion layer charge which is essentially the electrons that can come from the source and the drain region and even at high frequency in the MOSFET we will see this behavior this low frequency behavior will be seen ok.

Because now the electrons need not come from recombination generation process, they can come from the contacts as well they can because they are the majority carriers there. So, this is the frequency this will be the frequency or this will be the CV relationship for all frequencies ok.

(Refer Slide Time: 39:29)

**Threshold voltage**

Gate voltage needed to bend the bands so that:  $\psi_S = 2\psi_B$

$Q_S(2\psi_B) \approx Q_D(2\psi_B)$

$V_T = V_{FB} - \frac{Q_D(2\psi_B)}{C_{ox}} + 2\psi_B$       $V_T = V_{FB} - \frac{Q_S(2\psi_B)}{C_{ox}} + 2\psi_B$

$V_T = V_{FB} + \frac{\sqrt{2qN_A\epsilon_s(2\psi_B)}}{C_{ox}} + 2\psi_B$

**Gate capacitance**

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_S(\psi_S)}$

$C_G(inv) \approx C_{ox}$

$C_G(acc) \approx C_{ox}$

$\frac{1}{C_G(depl)} = \frac{1}{C_{ox}} + \frac{1}{C_D}$  F/m<sup>2</sup>

In depletion regime:  
 $C_S \approx C_D = \frac{\epsilon_s}{W_D(\psi_S)} = \frac{\epsilon_s}{\sqrt{2\epsilon_s\psi_S/qN_A}}$

$\psi_S = V_G \left( \frac{C_{ox}}{C_{ox} + C_D} \right) = \frac{V_G}{m}$       $m = 1 + \frac{C_D}{C_{ox}}$

$\psi_S = V_G \times \frac{C_{ox}}{C_{ox} + C_D}$       $m = \frac{C_{ox} + C_D}{C_{ox}} = 1 + \frac{C_D}{C_{ox}}$

Now, the last point in today's discussion is the relationship between  $V_G$  and  $\Psi_S$  in terms of various capacitances. We have already seen a relationship between  $V_G$  and  $\Psi_S$  in terms of charge, but a more intuitive picture is the relationship between  $\Psi_S$  and  $V_G$  as a function of various capacitances.

So, as you can see that this entire MOSFET can be sort of summarized in this way where this is the gate terminal then we have an oxide this is the interface between the oxide and the semiconductor and then we have the variable semiconductor capacitance and the voltage at the semiconductor surface is  $\Psi_S$  ok.

So, if we this is a series of capacitances, and if we try to find this  $\Psi_S$  in terms of  $V_G$  we just need to apply the voltage division rule in a series of capacitors and that rule says, what does that rule say is that  $\Psi_S$  is  $V_G$  times  $C_{OX}/(C_{OX} + C_D)$  or  $C_S \sim C_D$  is the case we are considering the depletion regime, and in total what we can do is we can define this to be  $V_G$  divided by  $m$ .

So,  $\Psi_S$  is  $V_G/m$ , where  $m$  is  $(C_{OX} + C_D)/C_{OX}$  or  $1 + C_D/C_{OX}$ . So, this  $m$  is known as the body coefficient and this is always a number larger than 1, but now we have a very intuitive expression between  $\Psi_S$  and  $V_G$ .

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**Threshold voltage**

Gate voltage needed to bend the bands so that:  $\psi_S = 2\psi_B$

$Q_S(2\psi_B) \approx Q_D(2\psi_B)$       $V_T = V_{FB} - \frac{Q_D(2\psi_B)}{C_{ox}} + 2\psi_B$       $V_T = V_{FB} - \frac{Q_S(2\psi_B)}{C_{ox}} + 2\psi_B$

$V_T = V_{FB} + \frac{\sqrt{2qN_A\epsilon_s(2\psi_B)}}{C_{ox}} + 2\psi_B$

**Gate capacitance**

$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_S(\psi_S)}$

$C_G(inv) \approx C_{ox}$

$C_G(acc) \approx C_{ox}$

**In depletion regime:**

$C_S \approx C_D = \frac{\epsilon_s}{W_D(\psi_S)} = \frac{\epsilon_s}{\sqrt{2\epsilon_s\psi_S/qN_A}}$

$\frac{1}{C_G(depl)} = \frac{1}{C_{ox}} + \frac{1}{C_D}$  F/m<sup>2</sup>

$\psi_S = V_G \left( \frac{C_{ox}}{C_{ox} + C_D} \right) = \frac{V_G}{m}$

$m = 1 + \frac{C_D}{C_{ox}}$

The slide contains several diagrams: a cross-section of a MOSFET gate stack showing oxide thickness  $t_{ox}$  and semiconductor thickness  $t_s$ ; a band diagram showing the bending of energy bands at the surface; a graph of gate capacitance  $C_G$  versus gate voltage  $V_G$  showing a step-like increase at threshold voltage  $V_T$ ; and a circuit diagram of a MOSFET gate stack with capacitances  $C_{ox}$  and  $C_S$  in series.

And that is  $\Psi_S$  is  $V_G$  divided by  $m$ . So, this  $m$  actually governs how much of the gate voltage drops across the semiconductor because if this  $m$  is close to 1 in that case  $\Psi_S$  will be almost equal to  $V_G$ . So, what we can say is that almost all the voltage drops across the semiconductor.

So, in an in our ideal or in order to make the MOSFET better and better what we try to do is, we try to make  $m$  as close to 1 as possible ok. So, we will stop here. I will recommend all of you to think more about the body coefficient this coefficient  $m$ , and we will start from this point, and we will see various ways in which  $m$  is brought closer to 1.

So, thank you and see you in the next class.