Physics of Nanoscale Devices
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Lecture - 41
MOSFET IV Characteristics - III

Hello everyone. Today in this lecture we will continue our discussion on the MOSFET IV Characteristics which we started in last lecture. And before going forward let us quickly review what we have seen so far.

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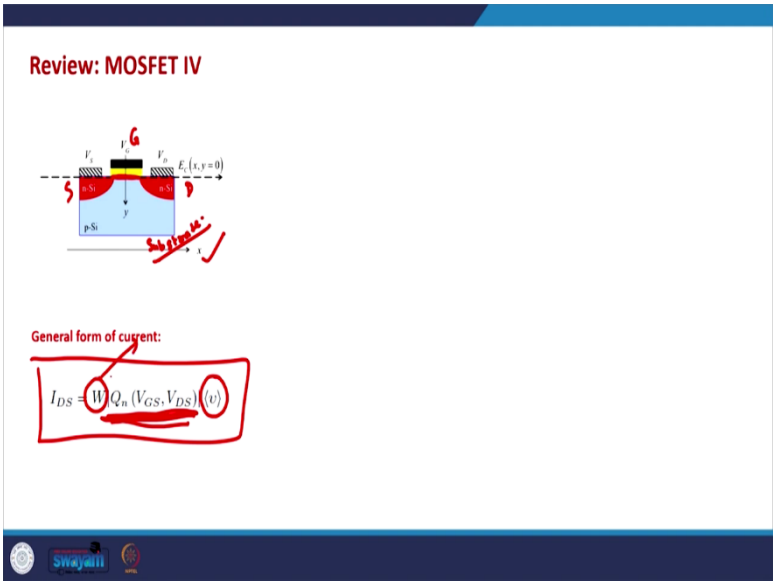

So, this is a typical structure typical geometry of the MOSFET, it has a source, a drain, a gate; mainly a three terminal device also has a body terminal or a substrate terminal does not play significant role, but one of the important roles of substrate is that the channel is formed in the substrate very close to the interface between the substrate and the oxide.

So, in this we have seen that the general form of the current in this structure in the MOSFET can be written as like this I_{DS} the current from drain to source is essentially dependent on two factors; one is the charge in the channel Q and V_{GS} V_{DS} this Q_n charge depends both on V_{GS} and V_{DS} and it depends on the velocity at which this charge is moved across the channel ok. Which is quite which is I would say a quite intuitive definition of the current and also in addition to these things it depends on the geometry it depends on the width of the transistor.

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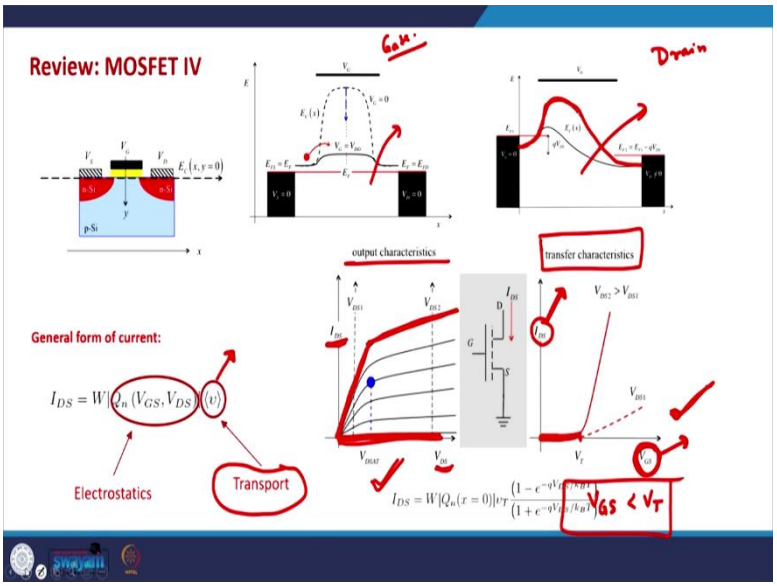

So, this is what we have also discussed in the previous lectures that the charge in order to analyze the charge in the channel we need to see the electrostatics of the MOSFET we need to see what is the effect of the gate voltage and the electric field due to the gate voltage on the channel region, also the electric field due to the drain voltage that is also what we need to closely see.

Second is the velocity of electrons in order to analyze the velocity of electrons we need to understand the transport theory of electrons in the nanostructures in the nano devices. Specially for the short channel MOSFETs that we use nowadays because the transport as we have seen in the previous part of this course that this has modified a lot in modern devices.

So, with this we saw that on application of a gate voltage this is how the barrier in the channel is changed and on application of the drain voltage this is how the barrier in the channel in the MOSFET looks like. So, this barrier in the channel is due to the structure of the MOSFET because we have n type contacts and p type substrate. So, if we draw the band diagram of this device this barrier appears naturally, but this barrier can be manipulated by applying a gate voltage and drain voltage.

And that is how we can manipulate things in the MOSFET and that is how we can induce current in the MOSFET ok. So, after this we saw that the IV characteristics of the MOSFET is generally divided in two types of characteristics; one is the output

characteristics which is essentially the relationship between the output current which is the drain source current and the input voltage which is the drain source voltage. I_{DS} versus V_{DS} is the output characteristics of the MOSFET and I_{DS} versus V_{GS} is the transfer characteristics of the MOSFET.

So, this characteristics is actually quite interesting because this is a very useful characteristic the output characteristics is very useful characteristics generally in circuits, but even this characteristics I_{DS} versus V_{GS}, this is also quite interesting because the voltage that we are considering is the gate voltage and the current that we are considering is the drain current.

So, this current is not flowing from the gate terminal. So, the terminals on which we are seeing or we are applying the voltage in this plot and the terminals across which the current is flowing is different. And that is why this is known as the transfer characteristics and generally it is used to understand the control of the gate voltage on the channel ok.

And in the output characteristics we also saw that there are three regimes one is the linear regime where the V_{DS} is very small and I_{DS} increases linearly with V_{DS}. Second is the saturation regime where the current does not change significantly with the drain voltage and third regime which is not properly visible in these plots is the sub threshold regime.

The sub threshold regime is also there in the transfer characteristics and this is the relationship between I_{DS} and V_{GS} when V_{GS} is less than the threshold voltage. So, that is why it is known as the sub threshold regime.

And the current characteristics in the sub threshold regime is known as the sub threshold characteristics. So, this is what we have seen so far. We have discussed fairly about the linear regime and the saturation regime and we started discussing the sub threshold regime. So, as you can see in on both of these plots that in the sub threshold regime the amplitude of the current is extremely low and this is not properly visible in these plots in the both of these plots; output characteristics and the transfer characteristics.

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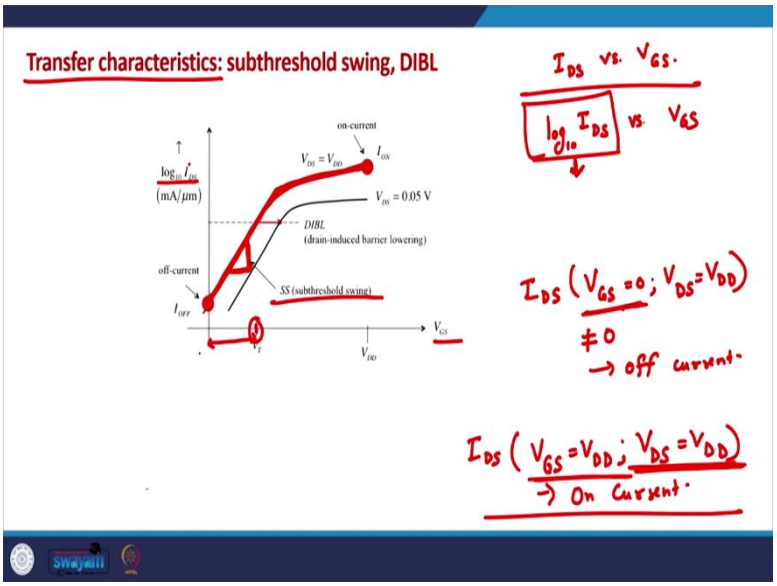

So, generally what is done is in order to properly understand the sub threshold regime instead of plotting I_{DS} versus V_{GS}, instead of doing that log of I_{DS} versus V_{GS} is plotted. So, this by taking log as you know that it gives us better resolution when the quantity is not changing very fast in that case the log plot gives us better resolution. So, if we analyze the lV characteristics and especially the transfer characteristics on a log scale of the current which means if we plot $\log_{10}(I_{DS})$ versus V_{GS} very close to the and see very close to the threshold voltage.

When V_{GS} is quite close to the threshold voltage this is kind of plot that we see. So, there is a linear relationship between $\log_{10}(I_{DS})$ versus V_{GS} when V_{GS} is less than V_T. In this regime the relationship between $\log_{10} I_{DS}$ and V_{GS} is almost linear. Which means that actually I_{DS} is exponentially varying as a function of V_{GS} in this regime.

So, that is why this log of I_{DS} is varying linearly with V_{GS} ok. And there is an important parameter here which is the I_{DS} when V_{GS} is 0 and V_{DS} is maximum. So, the value of I_{DS} when V_{GS} is 0 and V_{DS} is maximum; this is a non-zero number as you can see here this is the intersection of this line on this current axis and this is known as the off current.

Because when V_{GS} is 0 when gate voltage is 0 we expect that the device should be off because there should not be any channel we presume that there is no channel if V_{GS} is below V_T if V_{GS} is less than the threshold voltage, but in this case if we have a decent amount of drain voltage applied it means that there will be a finite current because there

is a non-zero probability of electrons crossing from the source side to the drain side and similarly from drain side to the source side.

But if we apply a high drain voltage the probability for the electrons to cross from the drain side diminishes and there is a finite probability that the electrons sitting on the source side will cross to the drain side and they will give us certain current even if V_{GS} is 0 and this is known as the off current.

Similarly when V_{GS} is maximum and V_{DS} is also maximum in that case this current is known as the on current. Because when V_{GS} is V_{DD} which it means that the channel is now properly there in the device and if we apply the maximum drain voltage this is sort of the maximum on current that would be there in the device ok.

And these two points are indicated on this plot as you can see in this sub threshold characteristics particularly the slope of this characteristics very close to the threshold voltage is an extremely important parameter which is known as the sub threshold swing. It is also known as the sub threshold slope.

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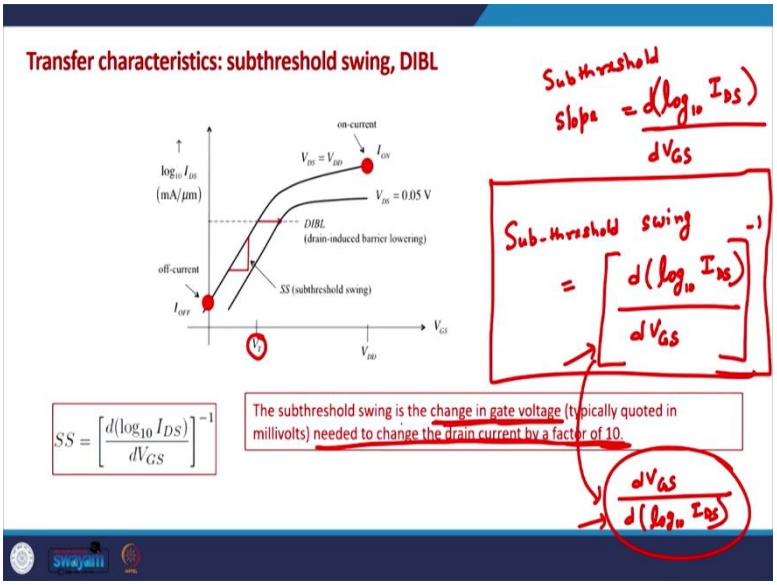

So, as you can see as you have already understood by now this sub threshold slope should be change in this divided by dV_{GS} ok this should be the slope. And the sub threshold swing is defined as inverse of this is defined as $\left(\frac{d \log_{10} I_{DS}}{dV_{GS}}\right)^{-1}$.

And the way it is defined is that it is the change in the gate voltage that is needed to change the drain current by a factor of 10 ok. So, ideally this sub threshold swing will be $\frac{dV_{GS}}{dI_{DS}}$, but this is not the way to understand it because V_{GS} is the independent parameter I_{DS} is the dependent parameter.

So, we write it in this way we do not write it in this way ok and this is defined as the amount or the change in the gate voltage below threshold voltage in the sub threshold regime it is the change in the gate voltage that is required to change the drain current by a factor of 10 ok.

That is defined as the sub threshold swing and this is an important parameter especially in the devices that are operating very close to the threshold voltage. And in some in many modern day applications especially in neuromorphic applications nowadays the devices need to be operated very close to the threshold voltage and in that case the sub threshold characteristics become extremely relevant right ok.

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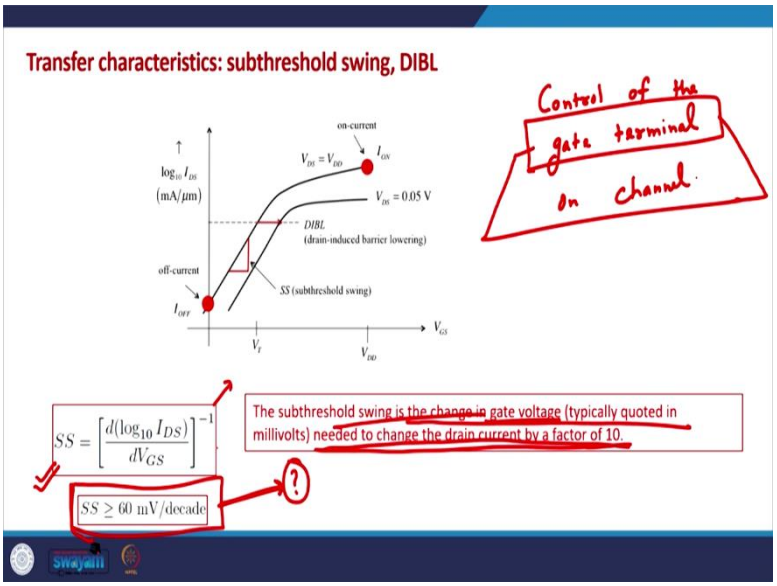

So, apart from this apart from just defining the threshold swing, it tells us about the control of the gate terminal on channel ok. So, if we need less gate voltage if we need less gate voltage to change the drain current by a factor of 10, it means that only a small change in the gate voltage is changing the current in the channel abruptly and it means that the gate terminal has better control on the channel ok.

And if we need a large voltage change on the gate terminal in order to change the drain current by a factor of 10, it means that now the control of the gate terminal on the channel is less ok. And since as all of us know that ideally this gate terminal is the control terminal and generally it is better to have the sub threshold swing as less as possible which means we want to have the control of gate terminal as maximum as possible ok.

So, we would always like to minimize the sub threshold swing parameter in the MOSFETs. And there is a fundamental limit up to which this can be minimized. So, for a MOSFET the sub threshold swing is always greater than equal to 60 milli volt per decade. 60 milli volt it means that at least 60 milli volt change in the gate voltage is required in order to change the drain current by a factor of 10 in the sub threshold regime of the transistor.

I would recommend all of you to go back and look into this limit where does this limit come from and this 60 milli volt per decade is the minima of this sub threshold swing. So, I would recommend you to go back and look into this; this is an interesting physics you will like it ok.

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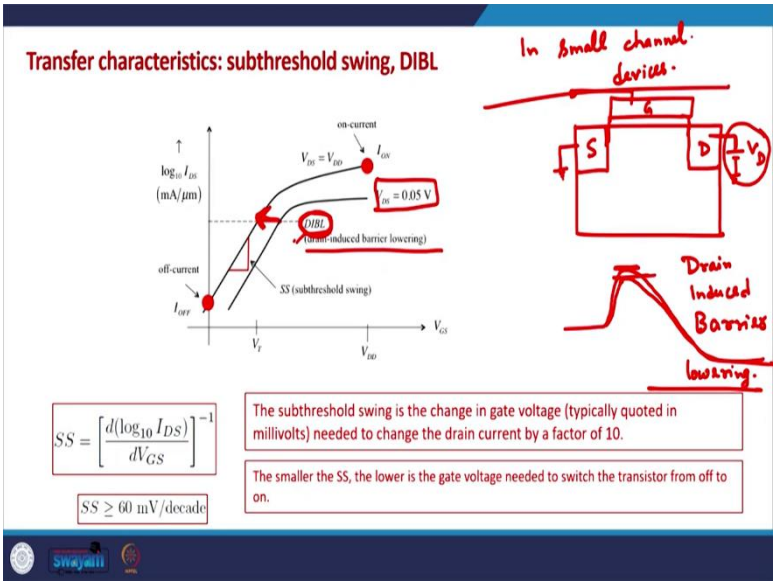

So, that was the main point here. Apart from this we have also seen that nowadays in small channel devices which means that the channel length is less than a micrometer or so or few tens of nanometers in that case the drain voltage is having an impact on the threshold voltage.

So, this is the source, this is the drain, this is a typical geometry of the MOSFET ok. In the long channel MOSFETs it used to happen when the channel length was in micrometers if we apply any voltage on the drain terminal if we apply a drain voltage here and the source voltage is let us say 0 sources most of the cases grounded in most of the cases it is grounded.

The voltage at the source side is always 0, the voltage at the drain side is V_D, the maximum and in between in the channel there is an electric field because of this voltage applied on the drain terminal. So, generally it used to happen that and this is how the barrier actually looks like in this device. So, it used to happen in long channel devices that this barrier height was shielded from the voltage that was applied on the drain terminal in long channel MOSFETs.

So, this barrier height is shielded in long channel devices ok. But nowadays in short channel devices because of the drain voltage even this barrier is changed this is no longer shielded and this is how it looks like in short channel devices and this phenomenon is known as the drain induced barrier lowering DIBL ok.

This we have already discussed and this is a typical small channel effect and on in the sub threshold characteristics because of DIBL effect because of drain induced barrier lowering this transfer characteristics are shifted to the right side.

So, if the drain voltage is less, it is on the right side. If the drain voltage is applied it reduces the threshold voltage it means that for high drain voltages the characteristics is on the left side, for low drain voltages the characteristics is on the right side in this plot.

Because drain is now helping the gate to create a channel. Generally prima facie it would seem that this is a good effect we are now having less threshold voltage the channel is appearing fast, but that is not the case because it is interfering with the role of the gate terminal and it is actually giving uncertainties in the device ok.

So, that it may reduce reliability of the device because in a chip there may be the drains terminal of various transistors may be at different voltages which means that it will create a variation in the threshold voltage and that might create error in the or that might create variation in the current or in the charge in the channel ok.

So, this DIBL effect is actually undesirable effect this generally we do not want this to appear in the channel, but because of the DIBL at high drain voltages the IV characteristics the transfer iv characteristics is on the left side and at low drain voltages it is on the right side ok. So, this on the log scale this is also properly visible this DIBL is also properly visible in the sub threshold characteristics ok.

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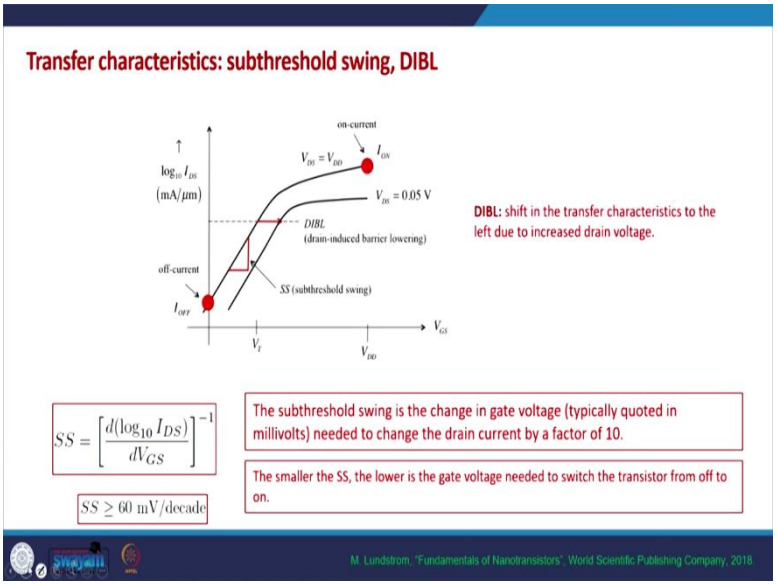

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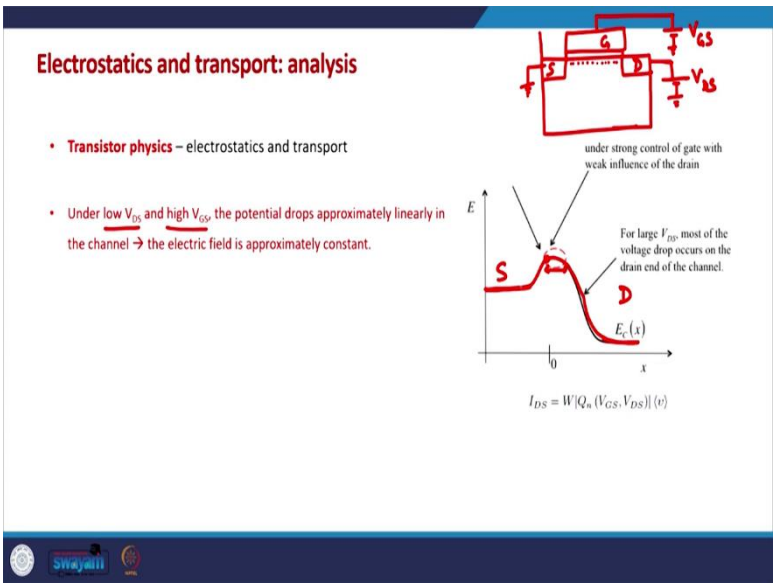

So, this is about the sub threshold characteristics and DIBL discussion and now there are a certain points that we need to I would say the qualitative points that we need to keep in

mind; this is how the barrier in the channel looks like in a typical MOSFET. This is the source side, this is the drain side.

This small region is very important region in a MOSFET because this is creating a barrier for the electrons sitting on the source side and this is actually controlling the current in the device ok. Now there are few points that we need to keep in mind one is that under low V_{DS} when V_{DS} the drain voltage is low and V_{GS} is high it means that because of the high V_{GS} the channel is there in the device there is a layer of electrons in the device.

So, if this is the MOSFET, this is source, this is drain, this is oxide, this is gate. So, because of the gate voltage ok because of the gate voltage the channel is there is if we consider NMOS there is a channel of electrons just below the gate terminal, but the V_{DS} voltage is very low this barrier the shape of this barrier will be almost linear from the height of the barrier to the drain side.

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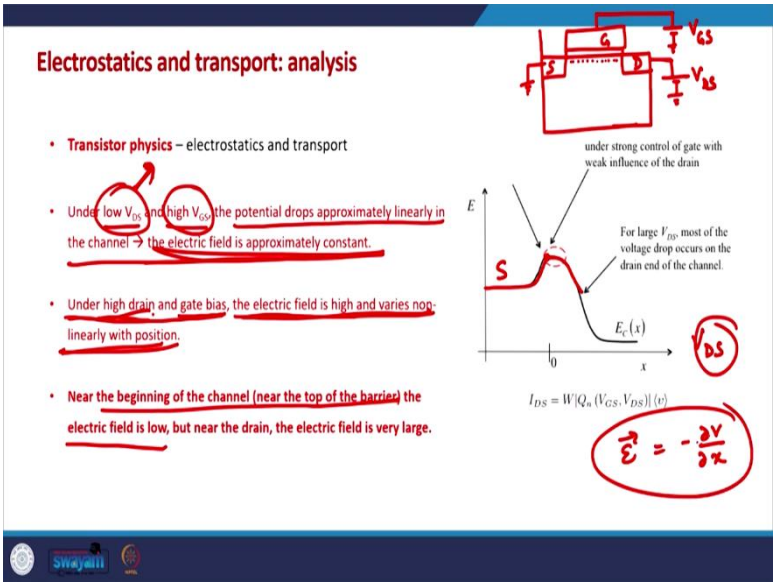

So, this barrier will be this will change very smoothly almost linearly ok. So, it means that high V_{GS} and low V_{DS} the potential drops approximately linearly in the channel and the electric field is almost constant in the channel ok. So, this is the case with when we have low V_{DS} which is the linear regime of IV characteristics of the or the output characteristics ok.

And this is also quite I would say also qualitatively understandable when a high drain voltage is applied and the gate voltage is already high. So, under high gate and drain bias the electric field is also high and it varies non-linearly in the channel. So, if V_{DS} is high if we are applying high voltage on the drain terminal the electric field in the channel will also be changing nonlinearly.

This is actually a subject matter of a MOSFET electrostatics which we will study in coming classes, but just to sort of qualitatively have an understanding of things when in the linear regime of output characteristics when V_{DS} is low in that case the electric field is approximately constant in the channel with high drain bias the electric field varies nonlinearly in the channel and at the beginning of the channel which is at the top of the barrier the electric field is very low.

As you can see that the voltage is directly proportional to the voltage is actually directly related to the potential energy and potential energy is directly related to the band edge. So, the electric field which is essentially $-\frac{\partial V}{\partial x}$ it is or to write it more generally because in short channel devices it needs to be written.

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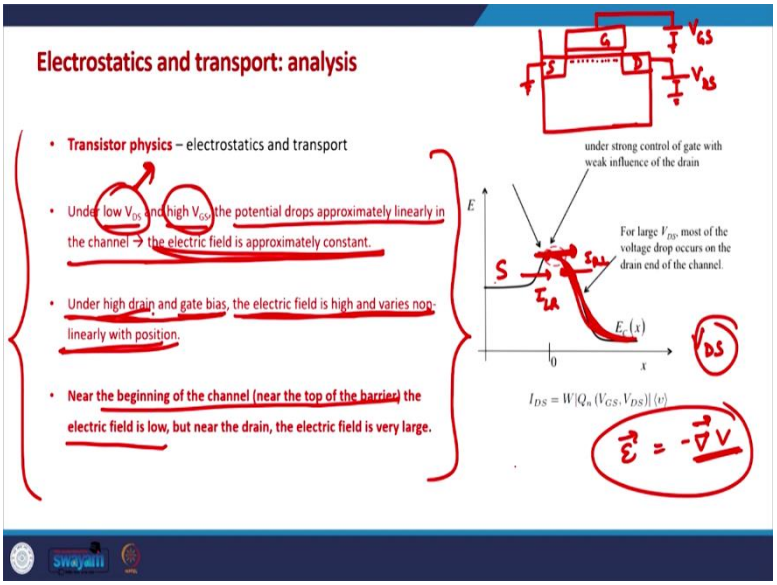

Properly it is the gradient of this band edge will give us the electric field in the channel ok. So, the gradient of the band at the top of the barrier is almost 0 or extremely low just at the top of the barrier the gradient is 0. So, the electric field is almost 0 at the top of the barrier, but on this side, on the drain side the bands change abruptly as you can see and that is why

the gradient will also have large value ok and that is why the electric field will also be large on the drain side ok.

So, these are few things that we need to keep in mind although these points will be discussed in more detail and more precisely in electrostatics part, but even qualitatively these things I these things make sense and this is what we always need to keep in mind. So, now comes the interesting part here.

So, the electric field at the top of the barrier is 0 ok; it means that just at the top of the barrier the force the electric force is also insignificant its almost 0 and in most of the cases the thermal velocity of the electrons play an extremely important role here just at the top of the barrier. Because the velocity due to the force is not there it is just the thermal velocity with which these electrons enter.

And when we take the average velocity in the barrier this thermal velocity plays an important part which we will see in the coming class ok.

Thermal velocity means that is the velocity that is due to just due to the thermal motion of the carriers ok. So, let me take a take a moment and summarize what we have seen. We have seen that MOSFET is a barrier control device, we have seen various IV characteristics of the MOSFET, we have seen and we have also derived in a way very qualitatively I would say or we have seen a glimpse of how IV characteristics of the MOSFET looks like.

In which we considered that the current going from the source to the drain side is I_{LR} left to right and the current from drain to source side is I_{RL} and by relating the current to the barrier height we have also seen how this current is dependent on the charge in the channel and the velocity of the electrons with which they cross the barrier ok.

We have also seen the sub threshold characteristics we have seen the DIBL effect. In coming classes we will see the transport theory or the transport theory that we or the model of we will apply the transport model that we derived in our previous classes in the first half of this course in the and we will apply that on the MOSFET device.

Before going into that detail let me quickly sort of take a detour and just for the sake of completion let us see how the traditional iv characteristics of the MOSFET look like. How traditionally the iv characteristics of the MOSFET is derived ok.

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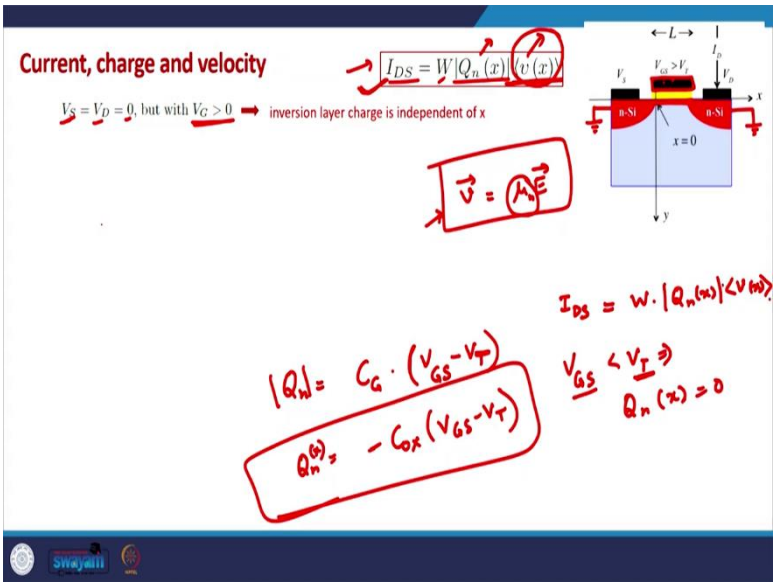

So, we will do that we will try to be quick in that because I suppose most of you might have already seen that and if not I would recommend you to go to the basic books of MOSFET any basic UG books of books on MOSFET and you can see how this IV characteristics is derived.

The book by Streetman and Banerjee is a good one if you want to if you want a recommendation or a book by Robert Pierre is also a good one ok. So, let us quickly try to see how traditionally the MOSFET IV characteristics is derived. The starting point we will take this starting point which is a fairly general form of current in a MOSFET I_{DS} the drain current depends on the charge in the channel and the velocity at which this charge moves multiplied by the width.

So, ultimately what we need to do is we need to find out how much charge is there in the channel and the velocity at which this charge moves. In the traditional theory this velocity of electrons is generally related to the electric field in this way, the velocity of a charge carrier is given by the electric field times the mobility of the charge carrier.

So, in case of electrons it is the velocity of electrons is the mobility of electrons times the electric field in the device ok and this is true in the case of long channel MOSFETs, but as we have seen in our previous discussions that the notion of mobility breaks down for ballistic transport or for the mesoscopic devices and that is why we need to do things in a

bottom up approach which we have already seen, but let us try to quickly see how the iv characteristics in a traditional MOSFET looks like.

So, this is the starting point I_{DS} is W times $Q_n(x)$ times the average velocity with which this charge moves in. So, let us take the case in where the source terminal is grounded and the drain terminal is also grounded; which means the V_S and the V_D is equal to 0 and V_G is greater than 0.

So, we have started applying a voltage on the gate terminal which will create a channel in the device which will create a layer of negative charges just below the oxide that will act as a channel in the MOSFET. And generally it is presumed that for V_{GS} less than V_T the charge is 0 charge in the channel is 0.

And the charge starts appearing when the gate voltage is slightly higher as soon as the gate voltage is slightly higher than the threshold voltage it appears at the higher voltages than the threshold voltage ok. So, in our classical treatment of MOSFET as I have already pointed out in one of the classes that this structure of the gate and the channel this is a capacitance like structure we have a conducting gate contact we have a conducting channel and in between we have a dielectric or an insulator.

So, the charge in the channel will depend on the capacitance of this capacitor and times the voltage applied. So, the charge in the channel will be the capacitance which is generally the gate capacitance times the voltage applied and as we have seen that if V_{GS} is less than V_T then there is no charge.

So, effectively the charge starts appearing as soon as V_{GS} is greater than V_T. So, the difference between V_{GS} and V_T is the voltage that will create charge on the capacitor plates ok. And with some approximations generally this gate capacitance is considered to be the oxide capacitance and this charge is negative.

So, this channel charge is negative. So, the charge in the channel is $-C_{ox}$ $(V_{GS} - V_T)$. So, this is the case when the source voltage is zero and the drain voltage is also 0 ok. So, this is the starting point for doing the traditional MOSFET electrostatics ok.

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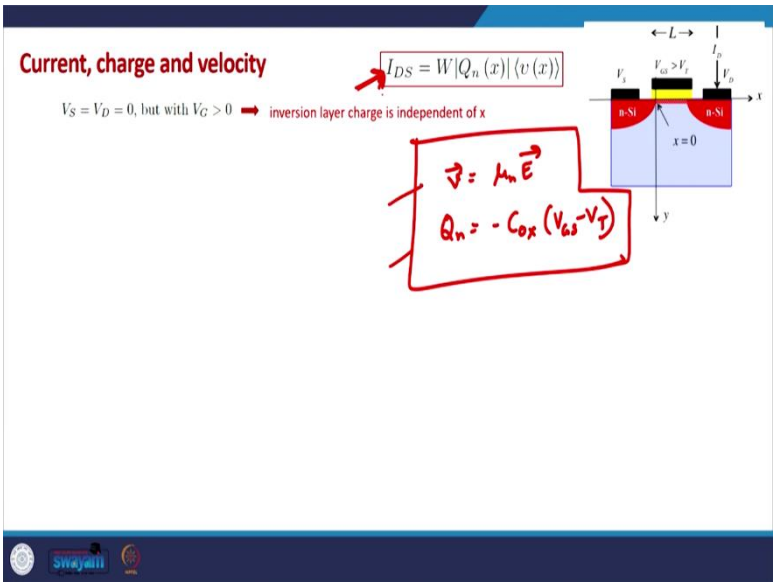

So, I will let you think more about it, I have told you how the velocity is treated the velocity is generally taken to be like this in traditional approach and the charge is taken this ok. Now, I think it must be straight forward for all of you to derive the IV characteristics using the traditional approach.

So, I would recommend that all of you give try this try putting these values in this expression and see how the IV characteristics look like. And in the coming class we will do the detailed analysis of IV characteristics using traditional approach ok. So, I thank you for your attention see you in the next class.

Thank you.