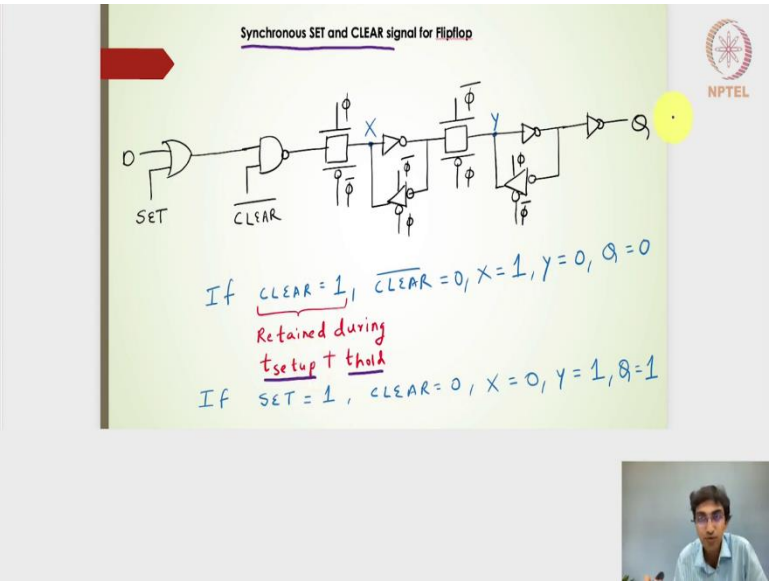
Design and Analysis of VLSI Subsystems
Dr. Madhav Rao
Department of Electronics and Communication Engineering
International Institute of Information Technology, Bangalore

Lecture - 84
SET and CLEAR enabled Latch and Flipflop Design

Hello students welcome to this lecture, in this particular lecture we will quickly go about understanding the asynchronous part of the SET and CLEAR Signals. Especially for the Latch and the Flipflop Designs.

Asynchronous in the sense that whenever we press the SET and CLEAR irrespective of the clock level being high or irrespective of during the edge transition, wherever we press the SET and CLEAR signal we should get the output to be 0 or 1 as we press the CLEAR or the SET signals. Hope this with that particular understanding let us move ahead.

(Refer Slide Time: 00:51)

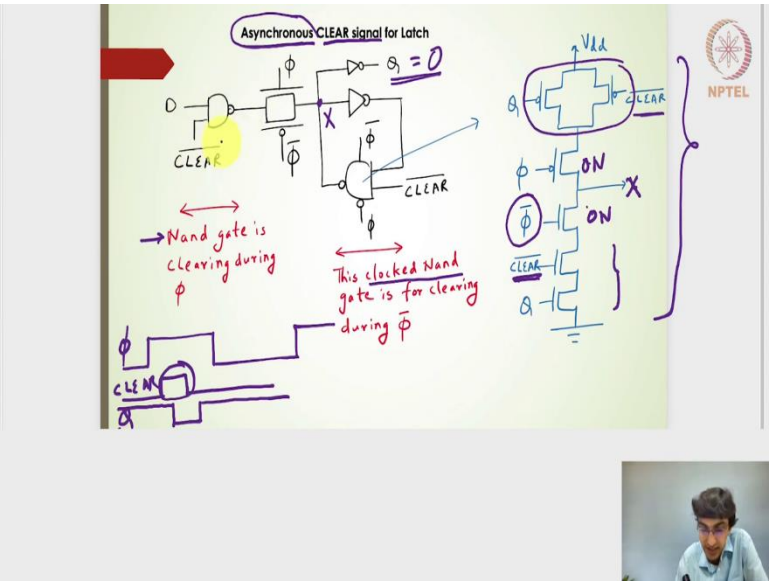


Let me also pick my pointer, this is what we had seen in the last lecture where it was a synchronous SET and CLEAR signal for the Flipflop. That is what the synchronous represents that only when the $\phi = 1$ the level high and if we press the SET or CLEAR signal we will get the output to be 1 or 0.

What it really means is that during the clock level to be high we have to maintain the SET and CLEAR signal at least before the t set up and it should be retained after the clock edge and then till the t hold time.

It should be the CLEAR signal or the SET signal should be retained for this entire duration of the set up and the whole time with respect to the negative edge of the clock, because this is a negative edge triggered the Flipflop, that is when I will get the proper output.

(Refer Slide Time: 01:46)



Let us have a look at the asynchronous part and let us try to understand with the latch design first and let us take only the CLEAR control signal for the latch design. This is something we had already seen except this particular portion. Just to summarize this if I apply the CLEAR if I press the CLEAR here I will get an output of 1, this output will be passed through the transmission gate during the high level of the clock and then the output will be 0. Whenever I press the CLEAR signal during the clock level to be high I will get the output to be 0.

Then this is the CLEAR and then the D signal path are provided to the D input NAND gate. Here is a statement saying that the NAND gate is clearing the output during whenever the transmission gate is passing the signal, that is when the clock is high.

But because I want an asynchronous portion that means, that even when the clock is low and if I press the CLEAR signal I need the output to be 0. To accommodate that there is a

tri-state 2-input NAND gate its called as a 2-input NAND gate, but there is a clocked NAND gate or rather I will call it as the clocked NAND gate or the clocked tri-state NAND gate and this is there to CLEAR the signal CLEAR the output during the clock level being low.

During the opaque mode of the latch. Now, let us have a look at this the 2-input NAND gate. It is nothing but at the transistor level it will be nothing but the NAND gate. If I consider these two transistors and the pull upside and then these two transistors in the pull downside and then these two transistors in the pull upside, that becomes like a 2-input NAND gate. But because it is a tri-state or a clocked NAND gate. We will have two transistors here 1 on the pull upside and then 1 on the pull downside and that those are provided or those are fed by the clock signals. This behaves like this completes the clocked NAND gate schematic.

What really happens is when the clock is low here, both these transistors will be ON, ON for the NMOS transistors and then the clock being low. The $\overline{clock}$ will be high and clock will be low, this PMOS will also be ON. Both these transistors are ON here, the output here which is provided to this particular X node. This particular X node here depends on what is the Q signal or what is the CLEAR signal. In this particular case because it is a 2-input NAND gate whenever the CLEAR is pressed. I will get the $\overline{CLEAR}$ to be 0. I will get the X to be 1 here and then this will throw the output to be 0.

This particular output being comes to 0 through when the clock is low comes to this particular tri-state or the clocked the NAND gate and when the clock is high and if I press the CLEAR the output of 0 is passed to this particular 2-input NAND gate.

We have used 2-input NAND gates here one is that the regular 2-input NAND gate another one is a tri-state or a clocked 2-input NAND gates, to get the cleared output. Both this NAND gates will pass the output or will make the output to be 0 during the different levels of the clock, that is why we call it as an asynchronous CLEAR signal.

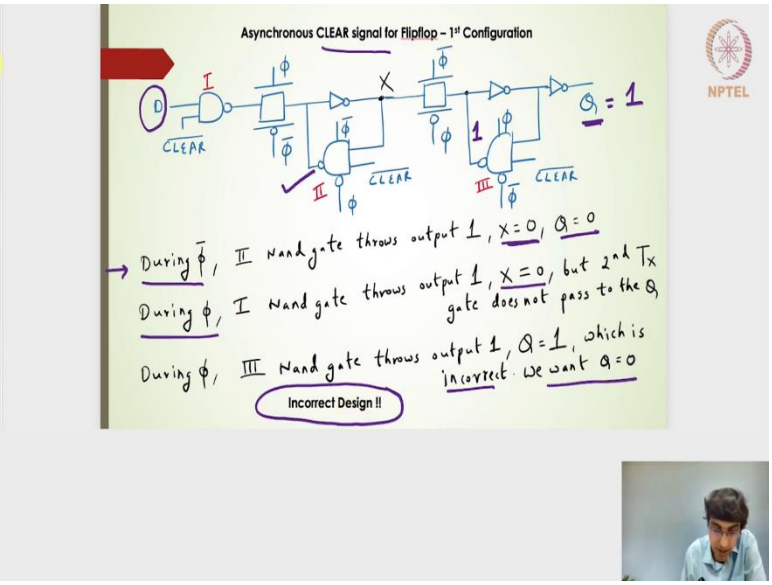
Remember that even when the clock is high here. Let us say if I have a this is the clock high and if I make the CLEAR press it for some time and then depress it. During this particular portion, let me write this as CLEAR and then I will also have an output of Q.

During this particular portion. The output let us say it is high and then during this particular portion it will go low and it will stay low because the CLEAR is pressed and then when the CLEAR depresses, then it may come back high depending on the D output signal or the D input signal.

It clears within this particular clock cycle and then comes back if the S is 1. Then it will come back to the to the D input. Whereas, in the $\overline{\text{clock}}$ signal whenever it is get it gets cleared here the Q will be retained to 0, because the D is not allowed in the clock whenever the clock is low because this particular transmission gate does not allow when the clock is low here, the transmission gate will be off, the D does not pass.

In the low level of the clock if the CLEAR is pressed then the Q will be 0 it will be retained. Whereas, in the high level whenever it is the CLEAR is pressed and if it is depressed it will get back that D value alright, that is an added information here.

(Refer Slide Time: 06:54)



Now, let us have a look at the asynchronous CLEAR signal for the Flipflop designs and if we can understand this then I think we can easily go or incorporate the preset or the SET signals and then finally, we will have a look into the latch design accommodating both CLEAR and the preset signal, asynchronous CLEAR signal for the Flipflops.

Now what it really means it means that whenever the clock is high if I press the CLEAR signal then I should get the output to be 0 and if the clock is low if I press the CLEAR

signal the output should be 0 alright and the output should get the updated value of the D only during the next clock edge. In this particular design this, the first latch is the positive level of the of the latch and then the second latch is this negative level of the latch. This particular Flipflop output or the Flipflop design is considered to be a negative edge triggered flip flop.

With this particular understanding, what we really need is if I press the CLEAR signal during the high level or during the low level, I need to have the Q to be made to be 0 and Q should wait for the next clock edge for the next negative edge or the falling edge of the clock, so as to get the updated D value.

Let us say that I have written three conditions here. Let us look at it one by one. During the $\overline{\Phi}$ that means, during the clock being low let us say that this is the design I have. Just a disclaimer here that it is an incorrect design. I have added the clocked 2-input NAND gate here I have added that clocked 2-input NAND gate here, because this clocked two input here was when we inserted that then we got the CLEAR signal as this the asynchronous CLEAR signal for the latch and with that understanding I have put both the clock 2-input NAND gate in both the latch designs.

To get the asynchronous CLEAR signal for the Flipflop. But again, I am just mentioning reiterating again that it is an incorrect design. Let us see why it is an incorrect design. Let us take the first case during the $\overline{\Phi}$. During the $\overline{\Phi}$ and I have annotated this first NAND gate, second NAND gate and then the third NAND gate.

The second and third NAND gates are the clocked NAND gates or the tri-state based NAND gates. During $\overline{\Phi}$ what we are saying is if the CLEAR is pressed then the clock level is low. The tri-state will pass this whenever the CLEAR is pressed I will get the output to be 0 here.

This 0 will make the X or rather this the output whenever the CLEAR is pressed the $\overline{CLEAR}$ will be 0. This output of the tri-state or the clocked 2-input NAND gate will be 1. This X will be 0, that is what it is mentioning here and this X will be 0 because the clock level is low here this is going to pass the 0 here and then the output will be 0. This seems to work well when the clock is low and if I press the CLEAR signal the Q output turns out to be 0

which is good. Let us say during the high level of the clock high level of the clock the first NAND gate is going to pass CLEAR is press.

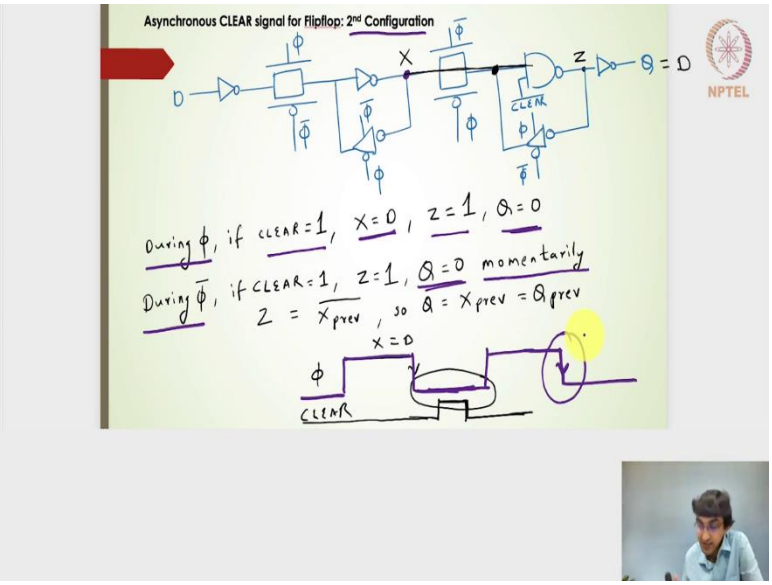
This will be 1 here, this will be 1 here, X will be a 0 here and X will be 0 here. But the $\overline{\phi}$ it is not going to pass because the clock is high here. I got an X value of 0, but the second transmission gate is not going to pass this X = 0 to the other side, because the clock is high.

In that sense the second transmission gate does not the passed output it does not give the output to be 0 it has to wait till the next, next the negative edge comes. Which is not what we are expecting we expect the moment the CLEAR is press I will get an output of 0. The high level of the clock this particular design does not achieve.

Let us say what happens with this particular 2-input NAND gate. This 2-input NAND gate is we wanted it to be giving the Q = 0 when the ϕ = 1 when the clock is high level, but this is not giving that this is giving the output when the ϕ is low let us talk about this third the clocked NAND gate or the third NAND gate.

The third NAND gate when the ϕ is high that means, this ϕ is high that means, this the two input or the tri-state or the clocked NAND gate will give me the output. If the CLEAR is pressed here when the ϕ is high. I will get an output of CLEAR pressed, $\overline{\text{CLEAR}}$ will be 0, this will be 1. The output here will be 1, but this is incorrect because we want the Q to be 0, that is why we say that it is an incorrect design right proceeding further.

(Refer Slide Time: 12:11)



What should be the design. Let us try another configuration second configuration here. In fact, if we look into this Flipflop designs I have removed the NAND gates from here I have removed the 2-input NAND gates from here I have removed the 2-input NAND gates from here.

I have just pressed taken this 2-input NAND gates here, this particular NAND gate is not clocked at all say if it is not clocked at all the moment if I press the CLEAR signal I will get the Z to be 1 and Q to be 0. The irrespective of the clock here and here if I make this 2-input NAND gate very close to the output and if it is not a clocked 1. The irrespective of the clock and irrespective of the D input if I press the CLEAR signal, I will get the output to be 0.

Seems to be very satisfying, but there are some problems here as well. Let me go over that let me go over these two cases. During the ϕ during the high level of the clock if the CLEAR is pressed 1 then I will get based on the D signal this X will be D whatever is the D value this X will achieve D that is what I have written here. But the Z is 1 here because CLEAR is pressed and then $\overline{\text{CLEAR}}$ will be 0 and Z will be 1 and then the Q will be 0.

The irrespective of the D signal, I will get the Q to be 0. During the low level of the clock during the low level of the clock if the CLEAR is 1, Z will be 1 and Q Z will be 0. Again, during the low level of the clock irrespective of all this transmission gates. The transmission gate tri-state inverter tri-state clocked inverter the output will be 0, seems to be satisfying. But the problem here is it is actually momentarily 0 and why I am saying that it is momentarily 0. The moment if I depress this CLEAR signal if I depress this CLEAR signal.

Whatever was the X previous, let us say that I have a clock here and during the low level of the clock. That is what we are considering at this particular low level of the clock. Let us say I have an input from D, which is gone and this X will contain in the D value based on the high level of the clock, because this transmission gate will be ON.

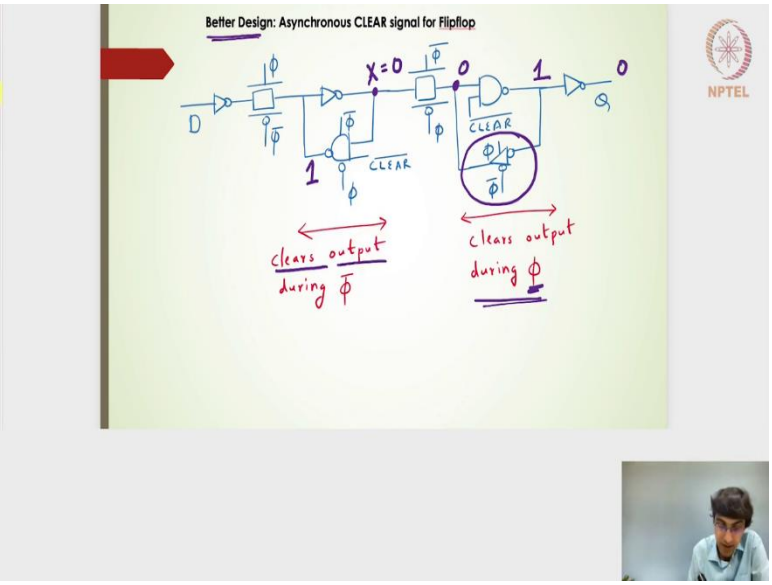
During the previous high level of the clock right I will have an X = D here alright and this updated D value is waiting here, but because when it goes to the clock goes to the low level that is when during the during the falling edge or the negative edge of the transition. This X is going to be passed here because of this particular transmission gate is now on,

but what really happens is because the CLEAR is pressed here somewhere here. I am going to have the CLEAR signal. Let us say that the CLEAR signal is here this is my clock and then the CLEAR is somewhere it is pressed here and it is depressed here, because the CLEAR is pressed here I will get an output of 0 during this particular portion of the CLEAR signal, but then after that once it goes down this X = D is there this X = D will be passed here. The D signal will be passed here although I will have this whenever this particular value is Z = 1 and Q = 0.

The moment CLEAR is depressed here it will take this particular signal and then I will get the Q to be nothing but D. The moment the CLEAR is depressed Q will become D and which is not what we want what we really want is from the circuit design what we need to I mean the way we need to accommodate the CLEAR control signal and the SET signal is the moment we press the CLEAR signal or the SET signal the Q should be 0 or 1 and should stay to 0 or 1 till the next negative edge will come.

Till the next negative edge means I will have to wait for this particular edge and it should not change anything during this level of the clock. Either during the positive level or during the negative level it should change only in the next subsequent edge falling edge in this particular case. In that sense this is a wrong design, Q will get updated with the previous value of X the moment the CLEAR is depressed again which is not a good design.

(Refer Slide Time: 17:05)



The better design is what I have drawn here, this is the third configuration design. What we need to do is this particular portion which was creating a problem because the D was passed here. This particular X value if it had retained the D value during the positive level of the clock and it was waiting for this CLEAR to be depressed and the moment is the CLEAR signal is depressed this X will be passed to the output.

Whenever the CLEAR is pressed we need to ensure that this CLEAR this X signal is also cleared and for doing that now in this particular better design there is a clocked NAND gate. This clock NAND gate will ensure that when during the $\overline{\phi}$ here the transmission gate, when it is likely to pass the X signal on the other side during the $\overline{\phi}$ this X signal should be cleared.

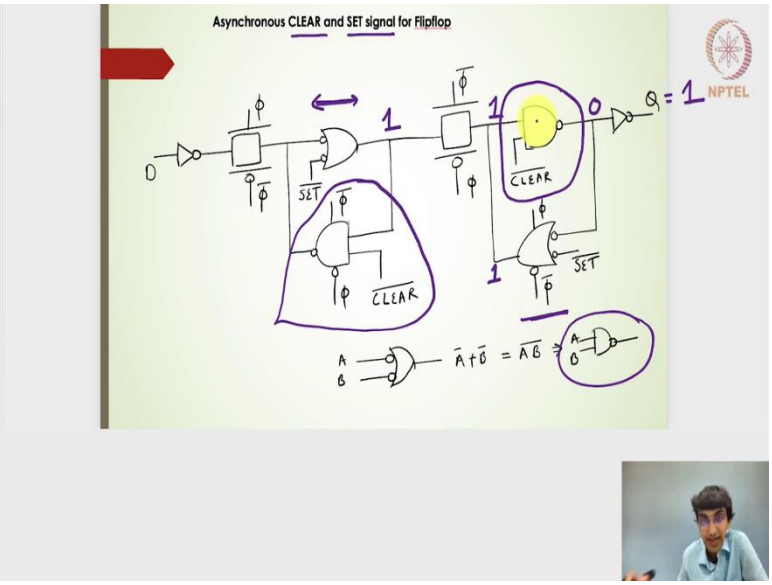
If I have this CLEAR signal pressed I know that the output here will be 1 and this will be 0, but at the same time this will be 1 here and then X will be 0. No matter what is the D here given during the $\overline{\phi}$.

This will be off, this transmission gate will be off and then it will X will take the value or it will take the precedence of this particular tri-state 2-input NAND gate which is driven by this CLEAR logic. The X will be 0 and then this 0 will be passed or will be maintained even if the CLEAR is depressed this 0 is going here and then will be retained, the Q will be 0 alright.

Hope this is clear. What we have accommodated this two NAND gates 1 this particular NAND gate ensures that the CLEAR output is 0, during the ϕ level of the clock and then during the ϕ level of the clock it is actually maintaining this particular path because this tri-state inverter is our it maintains this 1 and then makes this 0.

This node is statisticized and this statisticize node ensures that it does not dominates this particular part dominates and then makes keeps this value to be 0. During the ϕ phase during the clock level high whereas, this 1 this particular clocked 2-input NAND gate will ensure that during the ϕ is low during the $\overline{\text{clock}}$ or the ϕ being low this clears the output hope this is clear.

(Refer Slide Time: 19:53)



Let us try to accommodate the CLEAR and SET signal both for the Flipflop and we already know that this particular NAND gate will ensure that during the ϕ is high the output will be 0. This particular clocked NAND gate will ensure that when the clock is low the output will be clear.

How do we accommodate the SET signal as well, to accommodate the SET signal we have this particular portion and then we have this particular portion. Here the bubbled or gate is used the bubbled or gate is nothing but a NAND gate here.

This bubbled or gate 1 is the tri-state bubble or gate which is nothing but the bubble or rather the tri-state NAND gate and here it is not a tri-state it is just a forward passing a bubbled or gate. It will be nothing but a 2-input NAND gate.

One of the input is the SET signal. A $\overline{SET}$ is given to the bubbled one. What it really means is the SET is high. I will get the output of this or gate to be 1. Similarly, here if the SET is high and if the clock is whatever is the clock that has been given. If it is the clock is high here. During the high level of the clock, I will get if the SET is 1, I will get the output to be 1 here alright.

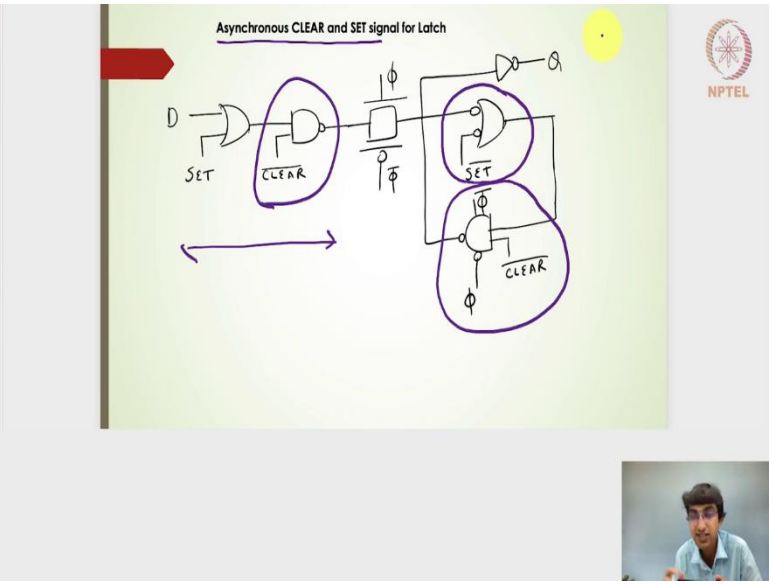
The way this works is if the SET is 1 during the negative level of the clock during the negative level of the clock if the SET is 1. I will have this output to be 1. During the negative level of the clock this transmission gate will pass the 1 here and then this 1

particularly will give the 0 here assuming that the CLEAR is not at all pressed. Again the condition is if the SET is pressed the CLEAR will be depressed and if the CLEAR is pressed the SET will be depressed.

This 0 will be passed and then the output will be 1. During the negative level or the low level of the clock this particular bubbled or gate is going to maintain the Q = 1 and then during the high level of the clock if this is SET is 1. I will get the value 1 here and then this will be 1 here and then 0 and then 1 here.

The clock whenever the clock is high this particular bubbled or gate will ensure that the Q is 1 and when the clock is low level this particular bubbled or gate is ensuring the output to be 1. Similarly, we have anyway seen the CLEAR control signals that have been accommodated or incorporated by this 2-input NAND gates. Hope this is clear. We have seen the asynchronous SET and CLEAR signal for the Flipflop.

(Refer Slide Time: 22:34)



The last one is asynchronous CLEAR and SET signal for the latch designs. For the latch designs what we are seeing was an asynchronous CLEAR signal which was accommodated by this particular 2-input NAND gates and this particular two input tri-state or the clocked NAND gates. But if I want to accommodate the SET signal pretty simple the synchronous CLEAR and SET signal, however we have designed we had this the 2-input OR gate and then that is been followed by the 2-input NAND gate for the

synchronous CLEAR and SET signal. The same designs will come here in the forward part and in this particular instead of an inverter here, we have used the bubbled or gate.

Then in this particular or gate we will apply the SET signal. Here it is the $\overline{SET}$ and here it is a set. This particular forward path will ensure that when the clock is high if it is either SET or CLEAR signal that has been pressed we will get the output, if it is either SET if it the output will be 1 if it is CLEAR the output will be 0.

When the clock is slow, this particular clocked 2-input NAND gate or this particular bubble or gate will ensure that the output is 0 or 1 during the ϕ being low. This clears or this completes the asynchronous control signals for the latch designs as well as the Flipflop designs. In this particular lecture we actually looked into the incorporating the asynchronous the control signal such as the CLEAR and SET signals for our latch and then the Flipflop designs.