Design and Analysis of VLSI Subsystems
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Lecture - 81
Static Timing Analysis - Part 4

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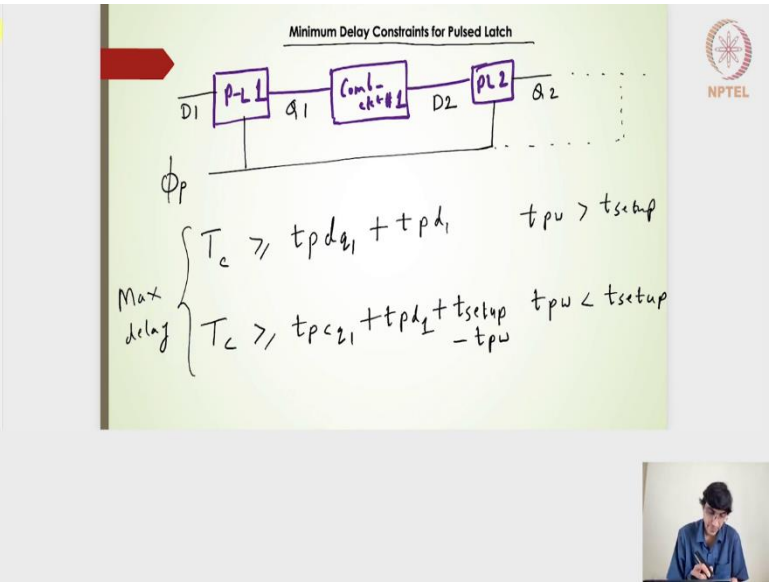

Let me draw the block diagrams stating the pulse latch and then the combinatorial circuit involved in it. What we want is the pulse latch here, the pulse latch number 1 and then we will have the combinatorial circuit. I am going to write a combinatorial circuit number 1 and then we will have the pulse latch number 2, this is my pulse latch number 2. Let us say that the clock here is given by the pulse signal, which is anyways generated by the original clock signal.

Let us say this is the D1 signal and then this is the Q1 signal that goes through the combinatorial circuit number 1 and generates the D2 signal and then the Q2 signal and then so on. This also I can say that it is going to be the next pulse latch number 3 and then so on. What we have arrived was the maximum delay constraints and just to reiterate the maximum delay constraint was that clock time period, we wanted to be greater than or equal to for the pulse latch design, we said that could be two expressions one is the t_{pdq1} where, if the t_{pw} the pulse width is greater than the setup time. In that case we will consider

it to be some kind of a latch design and in that sense it is t_{pdq1} plus the propagation delay of the combinatorial circuits.

$$T_c \geq t_{pdq1} + t_{pd1}$$

The other expression is especially valid if the t_{pw} is actually smaller than the t_{setup}, then we will have,

$$T_c \geq t_{pcq1} + t_{pd1} + t_{setup} - t_{pw}$$

This is what we have the two expressions for the maximum delay constraints and although the title says that is a minimum delay constraint what I wanted to showcase to all of you is it is nothing but the block diagrams and then in the next slide we will look into the minimum delta constraints. This establishes the maximum delay constraints and now we will go to the minimum delay constraints.

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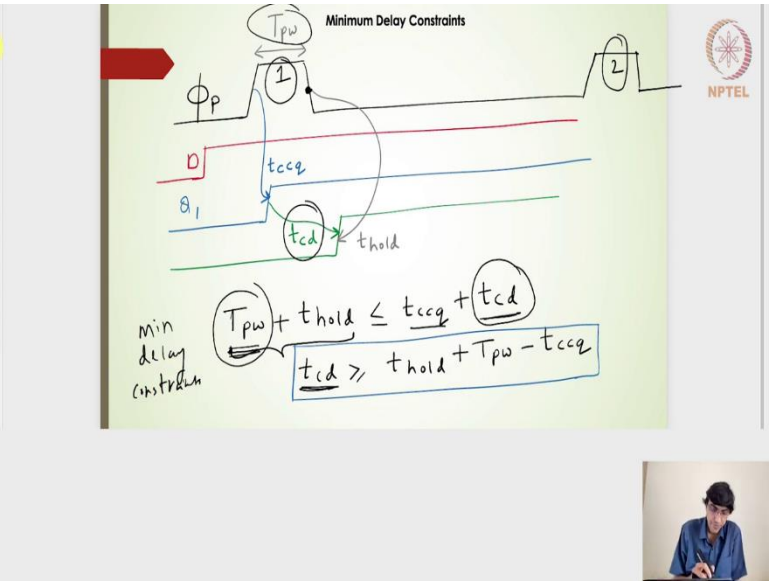

Having the same block diagrams where we have the pulse latch and then followed by the combinatorial circuits and then followed by the pulse latch number 2. Let us say this is the signal which we have the pulse signal which we have and then this is the first pulse signal. The pulse latch number 1s output will be generated in this particular pulse signal and then we will have the combinatorial circuit throwing the output. Then we are expecting the

combinatorial circuit number 2 or the pulse latch which is seeing the combinatorial circuit number 2 to get captured in the second pulse.

But, let us say that now due to the contamination output that has been generated by the pulse latch number 1. Let us say that the d is there much earlier than the t_{setup} is always with respect to the for the latch design especially it will be with respect to the due the falling output. If the latch the pulse latch or a regular latch is defined for a positive level of the clock or the pulse.

In that sense the t_{setup} is with respect to the negative edge and in that sense what we will say that D is arrived much earlier than the t_{setup} and the output of the pulse latch because the D has arrived earlier then it is with respect to the clock or the pulse going high.

We will have because it is a contaminated output which we are trying to see and trying to establish the minimum delay constraints or the hold time failures then we will take the contaminated output here and it will be with respect to the clock. It is a contaminated clock to Q delay, once we have the Q1 which is given to the combinatorial circuit, the combinatorial circuit will provide the contaminated output after the contamination delay.

Let us say that the contamination delay is here and with respect to the hold time for a latch design it is always with respect to the even if the latch is for the positive level the hold time is always with respect to the negative edge of the clock or in this case it is a pulse signal.

$$T_{pw} + t_{hold} \leq t_{ccq} + t_{cd}$$

Instead of capturing at the second clock cycle instead of the capturing at the second pulse levels for the pulse latch number 2. The pulse latch number 2 will actually get captured in the first pulse signal itself. now, that is a problem, what we need to do is we need to ensure that this $t_{ccq} + t_{cd}$ should arrive after this t_{hold} from the negative edge.

What it really means is should have

$$t_{cd} \geq t_{hold} + T_{pw} - t_{ccq}$$

We have to ensure that the buffer or rather the combinatorial circuit that has been designed should have a t_{cd} value which will extend beyond the t_{hold} and the T_{pw} for the first pulse.

So, that if it extends then it will not be captured in the first pulse rather it has to wait for the second pulse.

That is what the minimum delay constraints it says, this is the minimum delay constraints and if I look closely into this, it looks very very similar to that of the flop designs. The flop designs we have always had with respect to the rising edge. Here for the pulse latch it is only with respect to the falling edge. It has an additional parameter here of T_{pw} otherwise everything remains the same alright.

Now, because of this additional pulse width because of the pulse latch designs, the effective t hold time is actually a more than that of the flop designs. We have to be very very careful in designing the combinatorial circuit, because here in the flop designs it has to be only the $t_{cd} + t_{ccq} > t_{hold}$ whereas, in the pulse latch it has to be much much greater because the T_{pw} is getting added on to the left hand side. Efectively the minimum delay constraint or the minimum delay that the combinatorial circuit should be having is $t_{hold} + T_{pw} - t_{ccq}$, this that is why it is called as the minimum delay constraints.

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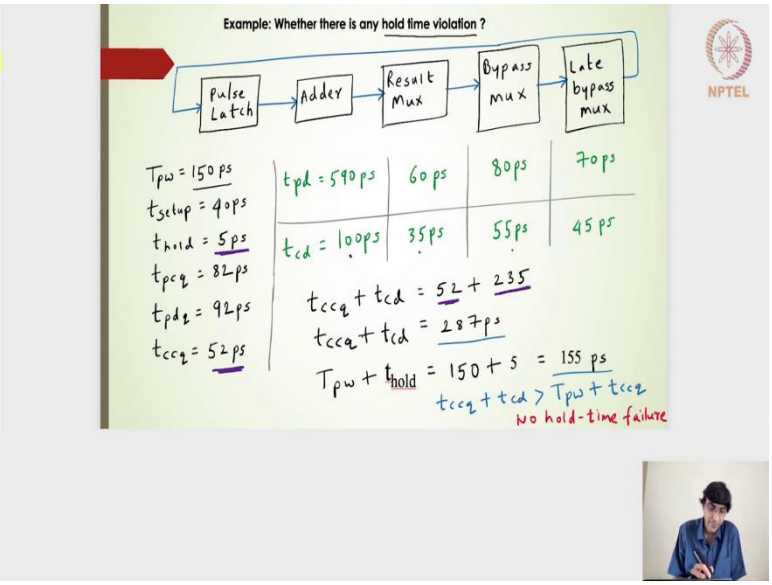

Now moving further let us take an example here and then let us see whether there is any minimum delay constraint is getting violated or in other terms whether the hold time is getting violated. We have a pulse latch here and then we have the 4 combinatorial circuits blocks here. The output of that is fed back to the pulse latch here, the pulse width is 150ps,

t_{setup} for the pulse latch which has been characterized as 40ps, hold time is 5ps, t_{pcq} has 82ps, t_{pdq} has 92ps and t_{ccq} has the 52ps. The propagation delay of all the combinatorial blocks are also provided here and then the t_{cd} the contamination delay of all the 4 combinatorial blocks are also provided here.

Now to find out whether it is a hold time failure it is very simple we need to find out the contamination delay of all the 4 blocks plus the t_{ccq} which is 52ps. The contamination delay of all the blocks it is nothing 100ps + 35 + 55 = 190 + 45 = 235ps + t_{ccq} of 52ps we will get 287ps.

We have to see whether 287 is much greater than we have the T_{pw} and the t_{hold} which is 5. The 155 on one side and 287 on the other side. The $t_{ccq} + t_{cd} > T_{pw} + t_{ccq}$. We can comfortably say that there will not be any hold time failures, hope this is clear. This is directly taken from the expression which we derived in the last slide.

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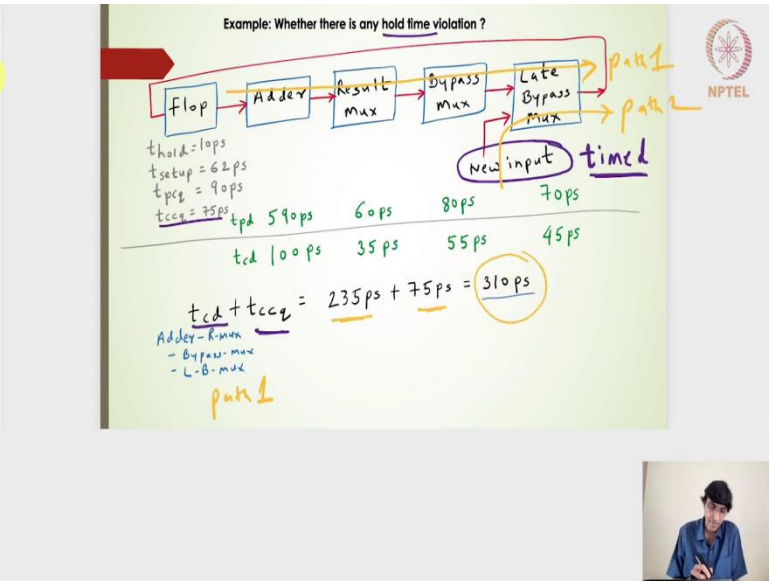

Moving ahead, this is a flop design now and then we will come back to the pulse latch design again, but we have the same kind of a circuit designs here. The adder block the MUX block the bypass MUX the late bypass MUX given back to the flop.

Then the flop is actually characterized by this particular parameters t_{ccq} is 75ps t_{pcq} is 90 seconds, setup is 62 and hold time is 10ps and the t_{pd} and t_{cd} of the adder MUXes three

MUXes are given here. The only condition now is the new input has been added here alright.

The new input they said what it means is basically one particular subsystem design, there is one critical path one path is this which passes through the flop adder result MUX, bypass MUX, late bypass MUX and it goes back to the flop. The other data part in this particular subsystem design is this new path. It may be coming from some any other I know any other circuit and we can say that we cannot just have it as a because it is a sequential circuit, we cannot have this as a random signal that has been generated, it has to be a timed new input.

We will say that this is a basically a timed input. What it means is we can say that it is actually coming from another flop or any other sequential element, it is a timed 1. We can at this particular point we can consider it to be a an input that is coming from the flop design. In that sense, we wanted to see whether there is will be any hold time violation. If it is coming from any other the flop inputs or the flop designs, this input will have the minimum path the other path will have the maximum delay. This path will have the minimum delay. If I am trying to find out the hold time violation. I need to find out which of this path has the minimum delay path and then try to establish or satisfy the hold time for that minimum delay path.

Now if I look into this particular blocks of adder result MUX bypass late bypass MUX. If I calculate the t_{cd} of that particular path plus the t_{ccq} plus this particular t_{cd} value for the flop design, that has to be greater than the t_{hold}. For this particular path the path number 1, let me write it in a different color, this will be path number 1 and I will say that this will be path number 2. For path 1 here I am trying to calculate,

$$t_{cd} + t_{ccq} = 235\text{ps} + 75\text{ps} = 310\text{ps}$$

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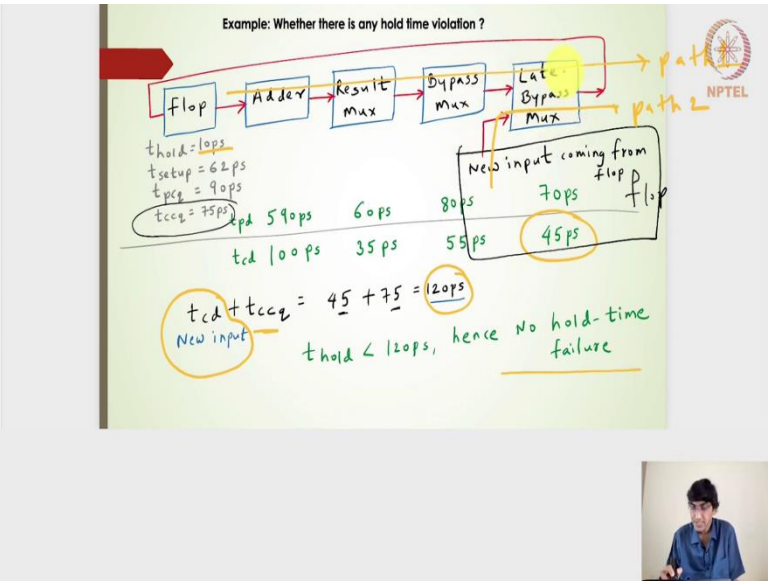

For the second path, this is path number 2, for the second path here coming from the new input plus the t_{ccq}. This particular path sees a 45ps of the contamination delay of the late bypass MUX plus I will say that because that is coming from another flip flop. Somewhere here we have a flip flop design is there. That particular flops t_{ccq} that I need to take into account and let us say that all the flop designs are kind of homogeneous.

We will have the same t_{ccq} here of 75ps. I am going to take that,

$$t_{cd} + t_{ccq} = 45 + 75 = 120\text{ps}$$

Which was the path 1 here, the path 1 was this particular path 1 alright. Path 1 if I look into the path 1 delay it was 310ps and path 2 it is 120ps. The 120ps we have to see because it is a minimum delay or the less delay than the path 1 then we will have to see whether it is violating any hold time failures.

The hold time is nothing but 10ps. I will say that 10ps is much much less than 120ps hence there is no hold time failure even for this particular design where there is a another path, which is joining the late bypass MUX.

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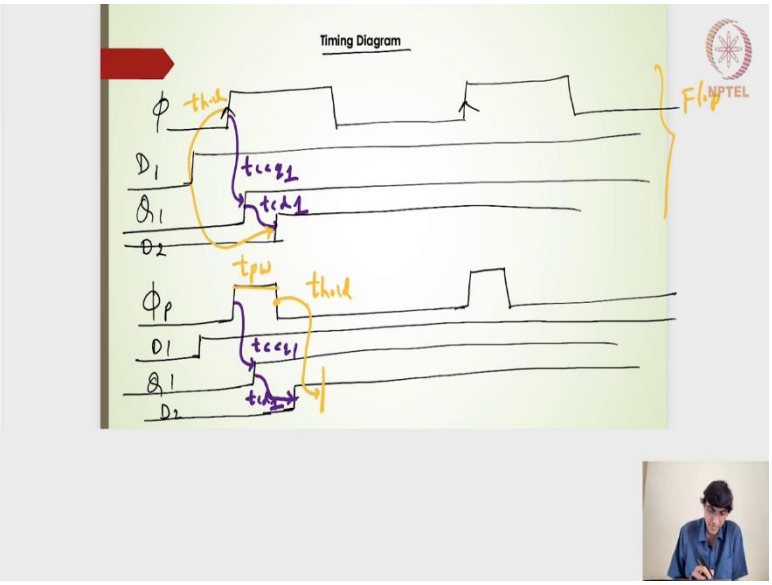

To look into the timing diagram here that means, I need to draw the timing diagram. I am going to draw the timing diagram both the flops and the pulse latch just to substantiate the difference of the hold time failures here. Let me draw the clock designs for the flop and I will have the clock design for the flop here, this is a positive edge triggered flop.

This is the clock here and let us say that the input to the flop of number 1 is arriving much much earlier and then the output here because it is a contaminated output that is what we are worried about, this will be my contaminated signal. This will be t_{ccq} for the flop number 1 and we will have the combinatorial circuit number output which goes to the second one.

Let us say this is my output that has been generated. I will say that this is my t_{cd} of the combinatorial circuit 1 and both put together it should be a better than the t hold of the clock that has been applied to the flip flop designs. These three are the flop designs and now I am going to draw that for the pulse latch designs alright. In this case what I am going to draw is a short duration here because it is a pulse signal.

Having the same clock frequency, a short duration and then the pulse. I am going to write this as speed ϕ p and then we are having the D1 signal let us say that D1 signal has arrived very similar to that of the flop design.

The D1 and then the Q1 output it produces the Q1 output and then let us say that again this Q1 is for the contamination delay. I will say that this is t_{ccq} for the pulse latch number 1. Now, this diagram is for the pulse latch instead of the flop designs and the next one it goes to the combinatorial circuits output the contaminated output is getting generated.

Let us say I have it here, this is I should have drawn this using the blue ink. This will be my t_{cd1} of the common utilities circuit, but here the t hold time is not with respect to the to the rising edge for the pulse latch

For the pulse latch it is actually with respect to this and if the t hold time comes somewhere here and I am going to write it as t hold here then although I have the same t_{ccq} and t_{cd} for the flop designs as well as for the pulse latch then even if the flop designs does not have a hold time failure. Here there is a possibility of a hold down failure because of this t_{pw} which is getting added into our timing constraints. With the same t_{ccq} and the same t_{cd} which has been used for the pulse latch I will still get a hold time failure, that is a possibility.

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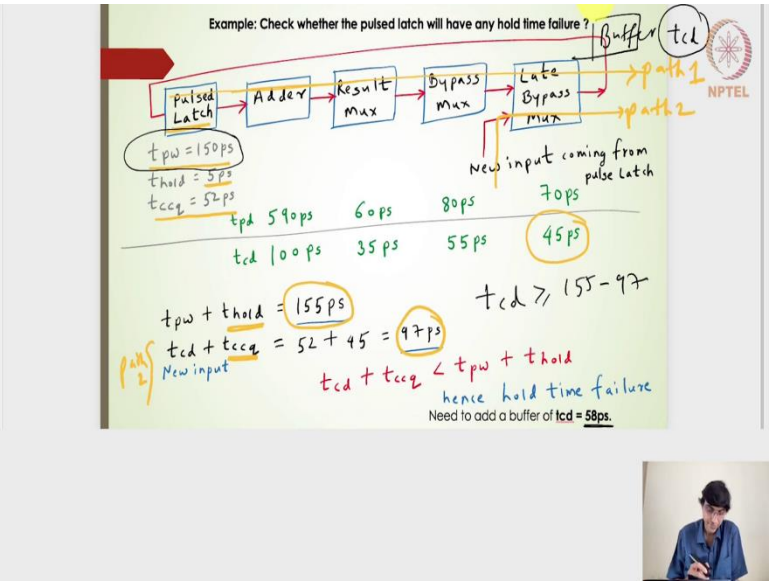

If I actually change this particular example of instead of a flop designs if I change it to the pulse latch and have the same combinational circuits having the same new input coming from the pulse latch, what we have to do is we have to make sure that it does not have any

hold time failure and if it does we will have to design a buffer. Let us say that the pulse latch the t_{pw} is 150ps the hold time is 5ps the t_{ccq} is 52ps.

Now similar to how we defined the paths there are two paths here. One path is this path, path 1 find out the delay for the path 1 and then the other path is this particular path the path coming from the new input coming from the pulse latch or the flop designs whatever it is.

We know that if I do the contamination delay addition of all these four blocks that will be more than that of a single late bypass MUX path. The t_{cd} for the new path or the path 2 here is going to be less than that of the path 1 and that is what we had seen in the flop designs.

The t_{cd} coming from the new input plus t_{ccq} coming from we can consider it to be a pulse latch of homogeneous design similar to the flop or the pulse latch here. If this is a pulse latch I was also say that because it is a timed circuit the new input is actually timed and we have the coming it from the pulse latch alright.

I will use the same t_{ccq} which has been given here for this particular pulsed latch, it will be 52 + 45 = 97ps and my t_{pw} + t_{hold} = 155ps, not only the t_{hold} of 5ps, but the t_{pw} is getting added and makes it 155 instead of 5ps.

The 97ps coming from this path 2 will have a hold time failure because of this 155ps. This is not surpassing 155 seconds. In fact, it is coming much much earlier than 155ps. We will have an output whatever is the contaminated output that is passing through this particular path will be sneaked in into the pulse latch. In fact, it will be sneaked in into an earlier pulse signal instead of waiting for the next pulse signal and that is a problem.

To overcome that problem we will have to add a buffer. We need to add a buffer somewhere here, in somewhere in this particular path of the late bypass MUX and not earlier than that. I need to add some kind of a buffer here, after the late bypass MUX and that particular buffers the contamination delay has to be a design such that it avoids the hold time failures.

Even for the new input coming from this pulse latch another pulse latch here and then the bypass MUX and then the buffer and then goes to the pulse latch. It will be it should be

able to easily avoid the hold time with respect to the first pulse signal and then it should be easily be able to capture in the second pulse.

What should be that particular buffer t_{cd} time, the t_{cd} time should be it should make sure that it surpasses this 155ps and to surpass that the t_{cd} will be nothing but should be at least be greater than 155 - 97ps = 58ps. The buffer design should be at least should be having a t_{cd} of 58ps to avoid the hold time failure.

Currently without the buffer we will have a hold time failure. Now, the other important thing is here the buffer I said that it has to be placed after the late bypass MUX because if it is placed before the late bypass MUX in any of this in between any of these combinational circuits.

That is going to not help this particular path 2, the buffer designs has to be added in this particular path 2 in the path of the path 2. Even if the new input comes, new input which is a timed input if it comes it has to propagate through the late bypass MUX it has to pass through the buffer which is a new buffer design and then it has to go to the pulse latch thereby.

Even if there is a contaminated output it will avoid the hold time or it will avoid this it will overcome this 155ps and it will not be captured in the in the previous pulse signal.

The buffer design has to be put before, if it is put somewhere here then the new input will not be able to see the buffered buffer t_{cd} value and even if we have designed a buffer somewhere here it will have only the late bypass MUX and then it should be able, there will be again be an hold time failure and the output the contaminated output coming from the new input here passes the late bypass MUX and then will be captured in the earlier pulse signals, hope this is clear.

We had seen two designs the flop designs and then the pulse latch and then in the pulse stats because of this T_{pw} value especially for the hold time failure, we will have to carefully design our combinatorial circuits or add a buffer design, that we avoid the hold time failures.

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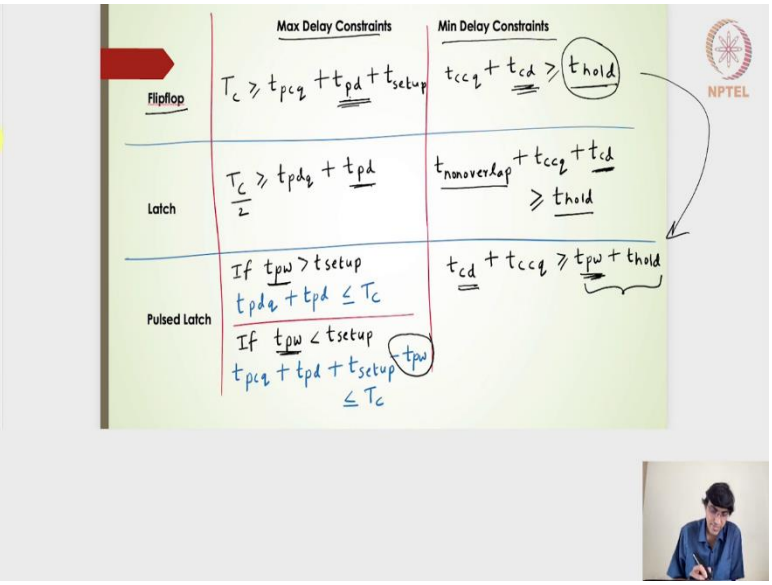

Just to summarize we have the maximum and minimum delay constraints. For the flop we have the minimum clock time period which is nothing but $t_{pcq} + t_{pd} + t_{setup}$ for the pulse latch, if the T_{pw} the pulse width is small it is very very similar here. The $T_c \geq t_{pcq} + t_{pd} + t_{setup} - T_{pw}$, that is the additional parameter here in the pulse latch.

The minimum delay constraints for the flop is nothing but the t hold should be smaller or rather the $t_{cd} + t_{ccq} \geq t_{hold}$, which usually gets satisfied in the flop design, because the t_{hold} is characterized for around 5ps or 10ps and normally we will have the t_{cd} values to be much much higher.

We are much in a better position if we have the flop designs, but if I consider the pulse latch designs for the hold time the T_{pw} gets added here and effectively the hold time put together it will much much larger. We should be careful in designing the combinatorial circuits t_{cd} value the contamination delay value and it should be greater than that of the $T_{pw} + t_{hold}$ of course, the $t_{cd} + t_{ccq} \geq T_{pw} + t_{hold}$.

On the other side the pulse design if the $T_{pw} > t_{setup}$ then we will say that the $T_c \geq t_{pdq} + t_{pd}$ which is very similar to that of the latch designs. In a latch if I want to determine or design a clock time period if I consider a transparent pair of the phase latches then it is nothing but $t_{pdq1} + t_{pdq2} + t_{pd1}$ of the combinatorial circuit number 1 + t_{pd} or 2 of the combinatorial circuit number 2.

The summation of all the four parameters and T_c should be greater than those of the summation of the four parameters, but if I am considering only the half the clock cycle then I can consider it to be one pair of the latch design and one pair or rather one of the latch design and the subsequent one combinatorial circuit. The $\frac{T_c}{2} \geq t_{pdq1} + t_{pd.}$

For the satisfying the hold time success in the sense there should not be any hold time violations, in that sense we will have to ensure that the

$$t_{non-overalp} + t_{ccq} + t_{cd} \geq t_{hold}$$

With this I think we have covered to most of the extents of the static timing analysis for the three sequential elements and you know especially we want to target the propagation delay and the contamination delay of the combinatorial circuit designs. To satisfy the maximum delay and the minimum delay constraints, there should not be any setup time violations there should not be any hold time violations.

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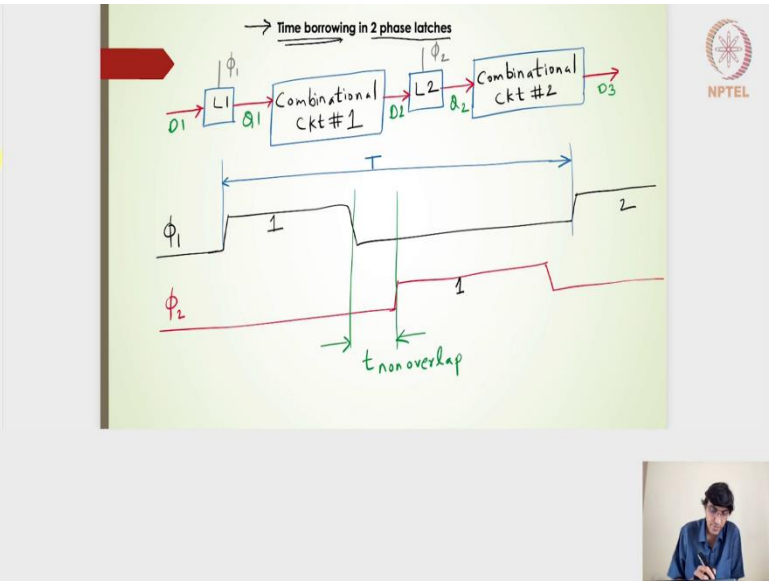

Let us move on to the last topic of this particular lecture, where it is about the time borrowing especially in the phase latches. When we are talking about the phase latches we will have a pair of latches we will have a pair of combinatorial circuits.

The latch number 1 latch number 2 and then the pair of combinatorial circuit number 1 circuit number 2. If I have a clock here ϕ 1 clock and then the ϕ 2 clock which is 180

degrees phase shifted. The ϕ 2 will be high during most part of the ϕ 1 being low and we will have a positive let us say we will have a positive non overlapping time.

The time borrowing concept says that how much of the time the combinatorial circuit number 1 or circuit number 2 can actually borrow from the other clock. Just to repeat and make you understand what we are expecting is the combinatorial circuit number 1 should get operated in the in the first level of the clock and then make the output available in the in the first clock of the high level of the ϕ 2 clock.

What we are expecting is combinatorial circuit number 1 to operate in this first high level of the ϕ 1 and combinatorial circuit number 3 should operate in the second clock level high of the ϕ 1 clock and a combinational circuit number 2 should operate in the first clock level high of the ϕ 2 clock.

Similarly, the combinatorial circuit number 4 should operate in the second clock level high of the ϕ 2 clock. That is what our expectation is, but even if it is combinational circuit if it extends the propagation delay extends beyond, it is trying to borrow some of the time from this ϕ 2 clock whenever it is level high. In that sense how much of time it can actually borrow without having any problems for the combination circuit number 2 or rather the combinatorial even if it borrows some of the time from here how far it can borrow. So, that the latch 2 will be able to capture the output of the combinatorial circuit number 1 the output of the combinatorial circuit number 1 even in the first level of the ϕ 2 clock.

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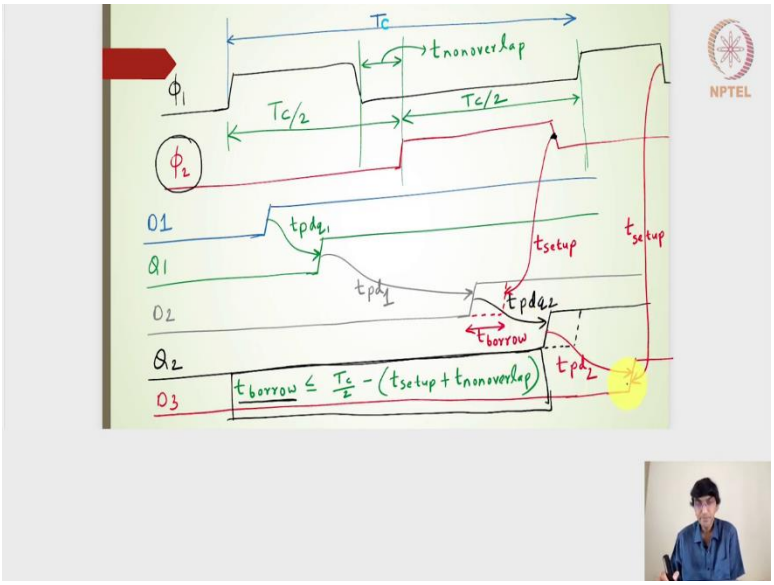

On that particular node let me try to explain this particular timing diagram. Let us say I have the clock 1 here which is given to the latch number 1 clock 2 which is 180 degree phase shifted and also it has non zero overlapping time a positive non overlapping time. Whenever the ϕ 1 is low that is when the ϕ 2 will go high for the most part of the ϕ 1 being low.

In all other cases it is actually the ϕ 2 is actually low. Now let us say that the D1 arrives somewhere in between this particular clock level high and Q1 which is nothing but the output of the latch 1, with respect to because clock 1 and D1 whichever arrives later. In this case D1 has arrived later. The Q1 the output of the latch 1 and the delay is with respect to the later signals in this case the D1 signal.

The output of the Q1 is drawn with respect to the propagation of D2q, that is where we have and this particular Q1 signal is given to the a combinatorial circuit number 1 and that is where it generates the D2 signal. Generally, it should be able to have a propagation delay of 1 and then it should be made available during the clock level high of the ϕ2 signal.

That the latch number 2 will be able to capture it during this particular level and then the d and then Q2 of the latch number 2 should be able to generate and then it passes to the combinatorial circuit number 3. Now if the combinatorial circuit number 1, which is actually operating in this particular level high and then making it available.

The output making it available during this particular level or during this particular level high. The question is how far it can make the output of the combinatorial circuit number 1 the output should be made available such that it will be captured in the latch number 2 and the answer is very simple it is nothing but it should be made available at least before the tsetup of for the latch number 2. The t setup time if I want to draw it will be with respect to the latch number 2, latch number 2 is also a clock level high with respect to the clock 2.

The clock level high, the latch at the t_{setup} is defined with respect to the transition going the clock transition going low. The combinatorial circuit can actually process for some more time can actually borrows for some more time here instead of this it can borrow up till this extent alright, then also the latch 2 is going to capture the output and then it will be made available to the combinatorial circuit number 2 and then the combinatorial circuit number 2 will be will show the output.

Then will be captured by the latch number 3 in the second clock level high off of ϕ1 signal. Even if it borrows till the tsetup, even if it borrows some amount of time till the t setup time for this particular latch number 2 there is no problem.

The question is how much of time the combinatorial circuit number 1 can actually borrow from the second clock. Actually, it turns out that the t_{borrow} the maximum t_{borrow} that can happen is $T_c/2$. In fact, if I write it this way

$$t_{borrow} \leq \frac{T_c}{2} - (t_{setup} + t_{non-overlap})$$

Even if I have a combinatorial circuit in the circuit number 1 if it is throwing the output somewhere here or here in this case it can still extend it can still borrow up till this t_{setup} and that is why the maximum t_{borrow} for the combinatorial circuit number 1 borrowing from the ϕ2 clock, especially during the clock level high is nothing but the maximum it can do is make sure that the signal reaches at least before the t_{setup} for the clock 2 of the level high.

That is why this is the expression that will be useful for designing the combinatorial circuit number 1 and having also no problem, because having no problems in the sense the D2 signal will be captured here and then the D2 for the latch 2 it will be anyways be captured because if the signal arrives before the setup time we will get the Q2 signal and then the D3 signal will also be made available.